

TOSHIBA

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MOS MEMORY PRODUCTS


**DATA BOOK
'85-9**

TOSHIBA CORPORATION

TOSHIBA

MOS MEMORY PRODUCTS

DATA BOOK

 quantum electronics

Box 391262

Bramley,

2018

TOHETA

STANDARD VOLUME 80M

DATA BOOK

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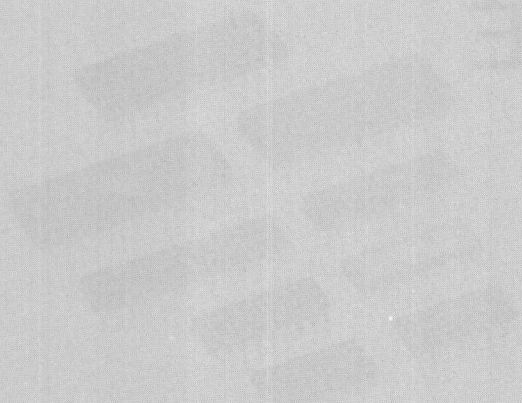
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MEMORY PRODUCT GUIDE



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1. NMOS Dynamic RAM

| Capacity | Type No. | Organi- zation | Access Time, Max(ns) | | Cycle Time Min (ns) | Power Supply (V) | Power Dissipation, Max(mW) | | Pins | Alternate Source |
|----------|------------------|-------------------|----------------------|------------------|------------------------|---------------------|----------------------------|---------|------|---------------------|
| | | | t _{RAC} | t _{CAC} | | | Active | Standby | | |
| 64K Bit | TMM4164AP-12 | 65,536×1 | 120 | 60 | 220 | +5 | 275 | 22 | 16 | — |
| | TMM4164AP-15 | | 150 | 75 | 260 | | | | | |
| | TMM4164AP-20 | | 200 | 100 | 330 | | | | | |
| 256K Bit | TMM41256C-12 | 262,144×1 | 120 | 60 | 220 | +5 | 330 | 28 | 16 | UPD41256 |
| | TMM41256C-15 | | 150 | 75 | 260 | | 275 | | | |
| | TMM41256C-20 | | 200 | 100 | 330 | | | | | |
| | TMM41256P-12 | 262,144×1 | 120 | 60 | 220 | +5 | 330 | 28 | 16 | UPD41256 |
| | TMM41256P-15 | | 150 | 75 | 260 | | 275 | | | |
| | □TMM41257P-12 | 262,144×1 | 120 | 60 | 220 | +5 | 385 | 28 | 16 | UPD41257 |
| | □TMM41257P-15 | | 150 | 75 | 260 | | 330 | | | |
| | TMM41464P-12 | 65,536×4 | 120 | 60 | 220 | +5 | 385 | 28 | 18 | UPD41464 |
| | TMM41464P-15 | | 150 | 75 | 260 | | 330 | | | |
| 1M Bit | * TMM411000C-10 | 1,048,576×1 | 100 | 50 | 190 | +5 | 385 | 22 | 18 | — |
| | * TMM411000C-12 | | 120 | 60 | 220 | | 330 | | | |
| | * □TMM411001C-10 | 1,048,576×1 | 100 | 50 | 190 | +5 | 385 | 22 | 18 | — |
| | * □TMM411001C-12 | | 120 | 60 | 220 | | 330 | | | |

Note: Package material P: Plastic C: Ceramic, □: Nibble mode parts

*: Preliminary.....These are target specifications and are subject to change without notice.

2. CMOS Dynamic RAM

| Capacity | Type No. | Organi- zation | Access Time, Max(ns) | | Cycle Time Min (ns) | Power Supply (V) | Power Dissipation, Max(mW) | | Pins | Alternate Source |
|----------|----------------|-------------------|----------------------|-----------------|------------------------|---------------------|----------------------------|---------|------|---------------------|
| | | | t _{RAC} | t _{AA} | | | Active | Standby | | |
| 1M Bit | *△TC511000C-10 | 1,048,576×1 | 100 | 55 | 190 | +5 | 330 | 5.5 | 18 | — |
| | *△TC511000C-12 | | 120 | 65 | 220 | | 275 | | | |
| | *○TC511001C-10 | 1,048,576×1 | 100 | 50 | 190 | +5 | 330 | 5.5 | 18 | — |
| | *○TC511001C-12 | | 120 | 60 | 220 | | 275 | | | |

Note: Package material C: Ceramic, △: Fast page mode parts ○: Static Column parts

*: Preliminary.....These are target specifications and are subject to change without notice.

3. NMOS Static RAM

| Capacity | Type No. | Organi- zation | Access Time Max (ns) | Cycle Time Min. (ns) | Power Supply (V) | Power Dissipation Max (mW) | | Pins | Package Width (inch) | Alternate Source |
|----------|--------------|-------------------|-------------------------|-------------------------|---------------------|----------------------------|---------|------|-------------------------|---------------------|
| | | | | | | Active | Standby | | | |
| 16K Bit | TMM2015AP-90 | 2,048×8 | 90 | 90 | +5 | 440 | 38.5 | 24 | 0.3 | (HM6116AS) |
| | TMM2015AP-10 | | 100 | 100 | | | | | | |
| | TMM2015AP-12 | | 120 | 120 | | | | | | |
| | TMM2015AP-15 | | 150 | 150 | | | | | | |
| | TMM2015BP-90 | 2,048×8 | 90 | 90 | +5 | 275 | 27.5 | 24 | 0.3 | (HM6116AS) |
| | TMM2015BP-10 | | 100 | 100 | | | | | | |
| | TMM2015BP-12 | | 120 | 120 | | | | | | |
| | TMM2015BP-15 | | 150 | 150 | | | | | | |
| | TMM2016AP-90 | 2,048×8 | 90 | 90 | +5 | 440 | 38.5 | 24 | 0.6 | (HM6116) |
| | TMM2016AP-10 | | 100 | 100 | | | | | | |
| | TMM2016AP-12 | | 120 | 120 | | | | | | |
| | TMM2016AP-15 | | 150 | 150 | | | | | | |
| | TMM2016BP-90 | 2,048×8 | 90 | 90 | +5 | 275 | 27.5 | 24 | 0.6 | (HM6116) |
| | TMM2016BP-10 | | 100 | 100 | | | | | | |
| | TMM2016BP-12 | | 120 | 120 | | | | | | |
| | TMM2016BP-15 | | 150 | 150 | | | | | | |
| | TMM2018D-35 | 2,048×8 | 35 | 35 | +5 | 825 | 110 | 24 | 0.3 | — |
| | TMM2018D-45 | | 45 | 45 | | | | | | |
| | TMM2018D-55 | | 55 | 55 | | | | | | |
| | TMM2068D-35 | 4,096×4 | 35 | 35 | +5 | 825 | 110 | 20 | 0.3 | IMS1420 |
| | TMM2068D-45 | | 45 | 45 | | 660 | | | | |
| | TMM2068D-55 | | 55 | 55 | | | | | | |
| | *TMM2078D-35 | 4,096×4 | 35 | 35 | +5 | 825 | 110 | 22 | 0.3 | — |
| | *TMM2078D-45 | | 45 | 45 | | 660 | | | | |
| | *TMM2078D-55 | | 55 | 55 | | | | | | |
| 64K Bit | TMM2063P-10 | 8,192×8 | 100 | 100 | +5 | 440 | 55 | 28 | 0.3 | — |
| | TMM2063P-12 | | 120 | 120 | | | | | | |
| | TMM2063P-15 | | 150 | 150 | | | | | | |
| | TMM2064P-10 | 8,192×8 | 100 | 100 | +5 | 440 | 55 | 28 | 0.6 | (HM6264) |
| | TMM2064P-12 | | 120 | 120 | | | | | | |
| | TMM2064P-15 | | 150 | 150 | | | | | | |

Note: Package material P: Plastic D: Cerdip

*: Preliminary.....These are target specifications and are subject to change without notice.

4. CMOS Static RAM

| Capacity | Type No. | Organi- zation | Access Time Max. (ns) | Cycle Time Min. (ns) | Power Supply (V) | Power Dissipation Max. (mW) | | Pins | Alternate Source |
|-------------|-------------------|-------------------|--------------------------|-------------------------|---------------------|-----------------------------|---------|----------|---------------------|
| | | | | | | Active | Standby | | |
| 4K Bit | TC5513AP-20 | 1,024×4 | 200 | 200 | +5 | 27.5 | 0.11 | 18 | HM6514 |
| | TC5513APL-20 | | 200 | 200 | | | 0.005 | | |
| | TC5514AP-2 | 1,024×4 | 200 | 200 | +5 | 27.5 | 0.11 | 18 | HM6514 |
| | TC5514AP-3 | | 300 | 300 | | | 0.005 | | |
| | TC5514APL-2 | | 200 | 200 | | | | | |
| | TC5514APL-3 | | 300 | 300 | | | | | |
| 16K Bit | TC5516AP/AF-2 | 2,048×8 | 200 | 200 | +5 | 302.5 | 0.165 | 24 | — |
| | TC5516AP/AF | | 250 | 250 | | | 0.005 | | |
| | TC5516APL/AFL-2 | | 200 | 200 | | | | | |
| | TC5516APL/AFL | | 250 | 250 | | | | | |
| | TC5517AP/AF-2 | 2,048×8 | 200 | 200 | +5 | 302.5 | 0.165 | 24 | (HM6116L) |
| | TC5517AP/AF | | 250 | 250 | | | 0.005 | | |
| | TC5517APL/AFL-2 | | 200 | 200 | | | | | |
| | TC5517APL/AFL | | 250 | 250 | | | | | |
| | TC5517BP/BF-20 | 2,048×8 | 200 | 200 | +5 | 27.5 | 0.165 | 24 | (HM6116L) |
| | TC5517BP/BF-25 | | 250 | 250 | | | 0.005 | | |
| | TC5517BPL/BFL-20 | | 200 | 200 | | | | | |
| | TC5517BPL/BFL-25 | | 250 | 250 | | | | | |
| | TC5518BP/BF-20 | 2,048×8 | 200 | 200 | +5 | 27.5 | 0.165 | 24 | (HM6117L) |
| | TC5518BP/BF-25 | | 250 | 250 | | | 0.005 | | |
| | TC5518BPL/BFL-20 | | 200 | 200 | | | | | |
| | TC5518BPL/BFL-25 | | 250 | 250 | | | | | |
| | *TC5517CP/CF-15 | 2,048×8 | 150 | 150 | +5 | 27.5 | 0.165 | 24 | (HM6116L) |
| | *TC5517CP/CF-20 | | 200 | 200 | | | 0.005 | | |
| | *TC5517CPL/CFL-15 | | 150 | 150 | | | | | |
| | *TC5517CPL/CFL-20 | | 200 | 200 | | | | | |
| | *TC5518CP/CF-15 | 2,048×8 | 150 | 150 | +5 | 27.5 | 0.165 | 24 | (HM6117L) |
| | *TC5518CP/CF-20 | | 200 | 200 | | | 0.005 | | |
| | *TC5518CPL/CFL-15 | | 150 | 150 | | | | | |
| | *TC5518CPL/CFL-20 | | 200 | 200 | | | | | |
| TC5564PL-15 | 8,192×8 | 150 | 150 | +5 | 27.5 | 0.005 | 28 | μPD4464C | |
| TC5564PL-20 | | 200 | 200 | | | | | | |
| 64K Bit | TC5565PL/FL-12 | 8,192×8 | 120 | 120 | +5 | 27.5 | 0.55 | 28 | HM6264L |
| | TC5565PL/FL-15 | | 150 | 150 | | | 0.165 | | |
| | TC5565PL/FL-12L | | 120 | 120 | | | | | |
| | TC5565PL/FL-15L | | 150 | 150 | | | | | |
| | *TC5561P-55 | 65,536×1 | 55 | 55 | +5 | 550 | 0.55 | 22 | — |
| | *TC5561P-70 | | 70 | 70 | | | | | |
| | *TC5562P-45 | 65,536×1 | 45 | 45 | +5 | 550 | 11 | 22 | HM6287 |
| | *TC5562P-55 | | 55 | 55 | | | | | |
| 256K Bit | *TC55257P-10 | 32,768×8 | 100 | 100 | +5 | 27.5 | 5.5 | 28 | — |
| | *TC55257P-12 | | 120 | 120 | | | | | |
| | *TC55257PL-10 | 32,768×8 | 100 | 100 | +5 | 27.5 | 0.55 | 28 | — |
| | *TC55257PL-12 | | 120 | 120 | | | | | |

Note: Package material P: Plastic F: Flat package

*: Preliminary.....These are target specifications and are subject to change without notice.

5. NMOS EPROM

| Capacity | Type No. | Organi- zation | Access Time Max. (ns) | Cycle Time Min. (ns) | Power Supply (V) | Power Dissipation Max. (mW) | | Pins | Alternate Source |
|----------|---------------|-------------------|--------------------------|-------------------------|---------------------|-----------------------------|---------|------|---------------------|
| | | | | | | Active | Standby | | |
| 64K Bit | TMM2764D-15 | 8,192×8 | 150 | 150 | +5 | 525 | 131 | 28 | i2764 |
| | TMM2764D-2 | | 200 | 200 | | | | | |
| | TMM2764D | | 250 | 250 | | | | | |
| | TMM2764DI-15 | | 150 | 150 | | | | | |
| | TMM2764DI-2 | | 200 | 200 | | | | | |
| | TMM2764DI | | 250 | 250 | | | | | |
| 128K Bit | TMM27128D-15 | 16,384×8 | 150 | 150 | +5 | 525 | 131 | 28 | i27128 |
| | TMM27128D-20 | | 200 | 200 | | | | | |
| | TMM27128D-25 | | 250 | 250 | | | | | |
| | TMM27128DI-15 | | 150 | 150 | | | | | |
| | TMM27128DI-20 | | 200 | 200 | | | | | |
| | TMM27128DI-25 | | 250 | 250 | | | | | |
| 256K Bit | TMM27256D-15 | 32,768×8 | 150 | 150 | +5 | 525 | 131 | 28 | — |
| | TMM27256D-20 | | 200 | 200 | | | | | |
| | TMM27256DI-15 | | 150 | 150 | | | | | |
| | TMM27256DI-20 | | 200 | 200 | | | | | |

Note: Package material D: Cerdip DI type: Operating temperature range = -40°C ~ 85°C

6. CMOS EPROM

| Capacity | Type No. | Organi- zation | Access Time Max. (ns) | Cycle Time Min. (ns) | Power Supply (V) | Power Dissipation Max. (mW) | | Pins | Alternate Source |
|----------|-------------|-------------------|--------------------------|-------------------------|---------------------|-----------------------------|---------|------|---------------------|
| | | | | | | Active | Standby | | |
| 256K Bit | TC57256D-20 | 32,768×8 | 200 | 200 | +5 | 158 | 0.525 | 28 | MBM27C256 |
| | TC57256D-25 | | 250 | 250 | | | | | |

Note: Package material D: Cerdip

7. NMOS Mask ROM

| Capacity | Type No. | Organi- zation | Access Time Max. (ns) | Cycle Time Min. (ns) | Power Supply (V) | Power Dissipation Max. (mW) | | Pins | Alternate Source |
|----------|-----------|-------------------|--------------------------|-------------------------|---------------------|-----------------------------|---------|------|---------------------|
| | | | | | | Active | Standby | | |
| 64K Bit | TMM2365P | 8,192×8 | 200 | 200 | +5 | 550 | 138 | 28 | (i2764) |
| | TMM2366P | | 200 | 200 | | 550 | 138 | 24 | (TMS4764) |
| 128K Bit | TMM23128P | 16,384×8 | 200 | 200 | +5 | 440 | 110 | 28 | (i27128) |
| 256K Bit | TMM23256P | 32,768×8 | 150 | 230 | +5 | 220 | 55 | 28 | (i27256) |

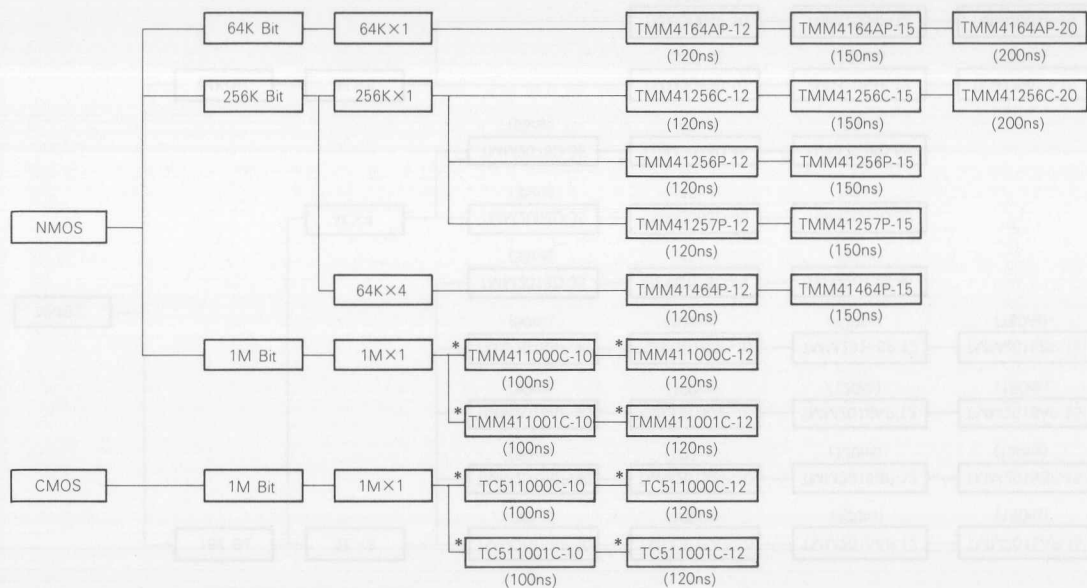
Note: Package material P: Plastic

8. CMOS Mask ROM

| Capacity | Type No. | Organi- zation | AccessTime Max. (ns) | Cycle Time Min. (ns) | Power Supply (V) | Power Dissipation Max. (mW) | | Pins | Alternate Source |
|----------|------------|-------------------|-------------------------|-------------------------|---------------------|-----------------------------|---------|------|---------------------|
| | | | | | | Active | Standby | | |
| 64K Bit | TC5364P | 8,192×8 | 250 | 350 | +5 | 39 | 0.11 | 28 | (MK37000) |
| | TC5365P/F | | | 250 | | | | 24 | (TMS4764) |
| | TC5366P | | | | | | | | |
| 256K Bit | TC53257P/F | 32,768×8 | 200 | 200 | +5 | 39 | 0.11 | 28 | (i27256) |
| 1M Bit | TC531000P | 131,072×8 | 200 | 200 | +5 | 39 | 0.11 | 28 | — |

Note: Package material P: Plastic F: Flat Package

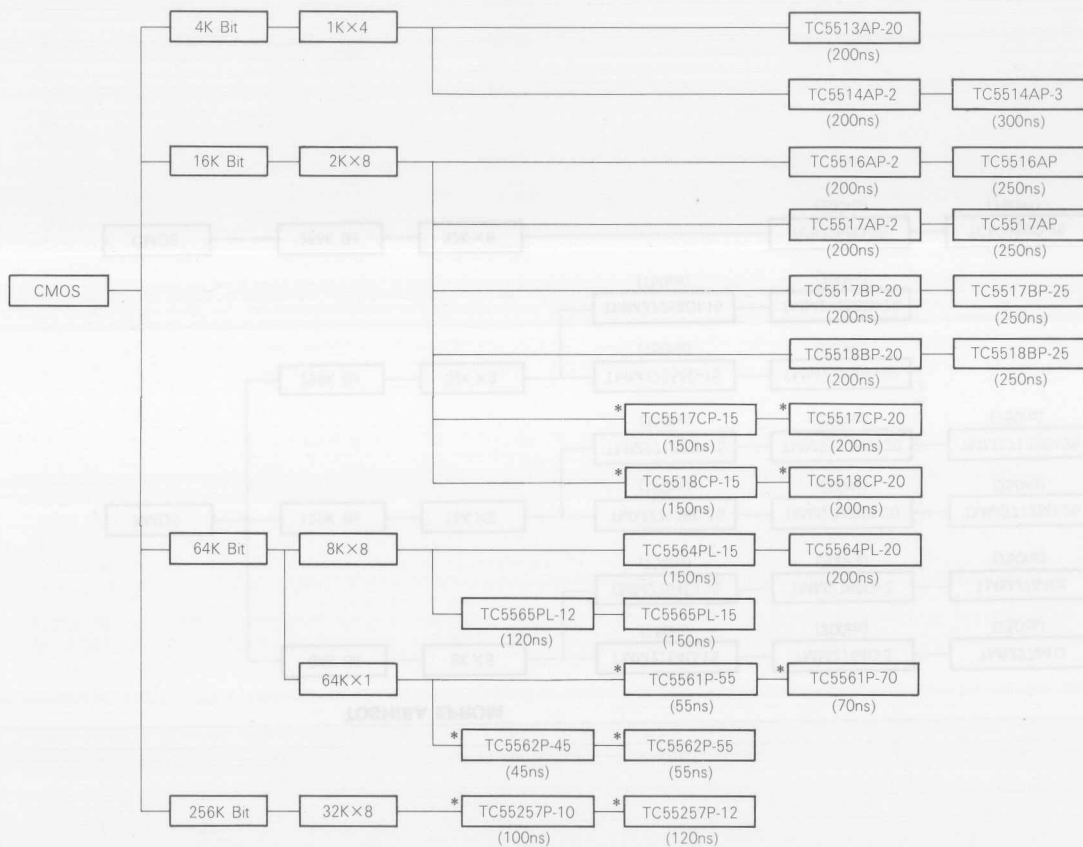
TOSHIBA DYNAMIC RAM



* : Preliminary

TOSHIBA STATIC RAM



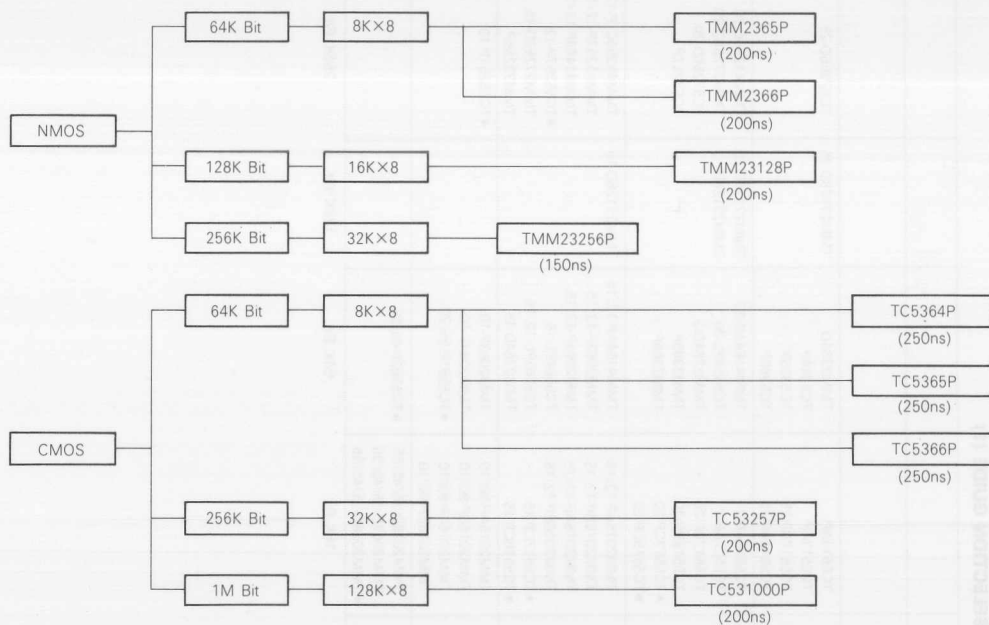


* : Preliminary

TOSHIBA EPROM



TOSHIBA MASK ROM



MEMORY SELECTION GUIDE (1)

* : preliminary

| Access Time (ns) | 4K Bit | 16K Bit | 64K Bit | 128K Bit | 256K Bit | 1M Bit |
|------------------|---------------------------|--|---|---------------------------|--|--|
| 300 | TC5514AP-3 | | | | | |
| 200 | | TC5516AP TC5517AP TC5517BP-25 TC5518BP-25 | TMM2764D TC5364P TC5365P TC5366P | TMM27128D-25 | TC57256D-25 | |
| | TC5513AP-20 TC5514AP-2 | TC5516AP-2 TC5517AP-2 TC5517BP-20 TC5518BP-20 *TC5517CP-20 *TC5518CP-20 | TMM4164AP-20 TC5564PL-20 TMM2764D-2 TMM2365P TMM2366P | TMM27128D-20 TMM23128P | TMM41256C-20 TMM27256D-20 TC57256D-20 TC53257P | TC531000P |
| 100 | | TMM2015AP-12/15 TMM2015BP-12/15 TMM2016AP-12/15 TMM2016BP-12/15 *TC5517CP-15 *TC5518CP-15 | TMM4164AP-12/15 TMM2063P-12/15 TMM2064P-12/15 TC5564PL-15 TC5565PL-12/15 TMM2764D-15 | TMM27128D-15 | TMM41256C/P-12/15 TMM41257P-12/15 TMM41464P-12/15 *TC55257P-12 TMM27256D-15 TMM23256P | *TMM411000C-12 *TMM411001C-12 *TC511000C-12 *TC511001C-12 |
| | | TMM2015AP-90/10 TMM2015BP-90/10 TMM2016AP-90/10 TMM2016BP-90/10 | TMM2063P-10 TMM2064P-10 *TC5561P-55/70 | | *TC55257P-10 | *TMM411000C-10 *TMM411001C-10 *TC511000C-10 *TC511001C-10 |
| | | TMM2018D-35/45/55 TMM2068D-35/45/55 *TMM2078D-35/45/55 | *TC5562P-45/55 | | | |

MEMORY SELECTION GUIDE (2)

* : preliminary

| Memory | Type | Memory Capacity | | | | | |
|--------|------------------|----------------------|--|---|-------------------------|---------------------------------------|----------------------------|
| | | 4K Bit | 16K Bit | 64K Bit | 128K Bit | 256K Bit | 1M Bit |
| RAM | NMOS Dynamic RAM | | | TMM4164AP | | TMM41256C/P TMM41257P TMM41464P | *TMM411000C *TMM411001C |
| | CMOS Dynamic RAM | | | | | | *TC511000C *TC511001C |
| | NMOS Static RAM | | TMM2015AP TMM2015BP TMM2016AP TMM2016BP TMM2018D TMM2068D *TMM2078D | TMM2063P TMM2064P | | | |
| | CMOS Static RAM | TC5513AP TC5514AP | TC5516AP/AF TC5517AP/AF TC5517BP/BF TC5518BP/BF *TC5517CP/CF *TC5518CP/CF | TC5564PL TC5565PL/FL *TC5561P *TC5562P | | *TC55257P | |
| | | | | | | | |
| ROM | NMOS EPROM | | | TMM2764D TMM2764DI | TMM27128D TMM27128DI | TMM27256D TMM27256DI | |
| | CMOS EPROM | | | | | TC57256D | |
| | NMOS Mask ROM | | | TMM2365P TMM2366P | TMM23128P | TMM23256P | |
| | CMOS Mask ROM | | | TC5364P TC5365P/F TC5366P | | TC53257P/F | TC531000P |

MEMORY SELECTION GUIDE (3)

| Word \ Bit | 1 | 4 | 8 |
|------------|--|-----------------------|---|
| 1K | | TC5513AP TC5514AP | |
| 2K | | | TMM2015AP TC5516AP/AF TMM2015BP TC5517AP/AF TMM2016AP TC5517BP/BF TMM2016BP TC5518BP/BF TMM2018D *TC5517CP/CF *TC5518CP/CF |
| 4K | | TMM2068D *TMM2078D | |
| 8K | | | TMM2063P TMM2365P TMM2064P TMM2366P TC5564PL TC5364P TC5565PL/FL TC5365P/F TMM2764D TC5366P |
| 16K | | | TMM27128D TMM23128P |
| 32K | | | *TC55257P TMM23256P TMM27256D TC53257P TC57256D |
| 64K | TMM4164AP TC5561P TC5562P | TMM41464P | |
| 128K | | | TC531000P |
| 256K | TMM41256C/P TMM41257P | | |
| 1M | *TMM411000C *TC511000C *TMM411001C *TC511001C | | |

* : preliminary

[illegible]

CROSS REFERENCE

1. 64K Bit Dynamic RAM

| | |
|------------|--------------|
| TOSHIBA | TMM4164AP |
| Fujitsu | MB8264A |
| Hitachi | HM4864A |
| Mitsubishi | M5K4164AN |
| Motorola | MCM6665A |
| NEC | μ PD4164 |
| Oki | MSM3764A |
| TI | TMS4164 |

2. 256K Bit Dynamic RAM

| Organization | 256K \times 1 (page mode) | 256K \times 1 (nibble mode) | 64K \times 4 (page mode) |
|--------------|-----------------------------|-------------------------------|----------------------------|
| TOSHIBA | TMM41256C/P | TMM41257P | TMM41464P |
| Fujitsu | MB81256 | MB81257 | MB81464 |
| Hitachi | HM50256 | HM50257 | HM50464 |
| Mitsubishi | M5M4256 | M5M4257 | M5M4464 |
| NEC | μ PD41256 | μ PD41257 | μ PD41464 |
| Oki | MSM37256 | MSM37257 | |
| TI | TMS4256 | TMS4257 | TMS4464 |

3. 16K Bit Static RAM

1) NMOS

| Organization | 2K \times 8 | | | 4K \times 4 |
|---------------|---------------|----------------|----------|---------------|
| Package Width | 0.6 inch | 0.3 inch | | |
| TOSHIBA | TMM2016AP/BP | TMM2015AP/BP | TMM2018D | TMM2068D |
| Fujitsu | MB8128 | | | MB8168 |
| Hitachi | HM6116 | HM6116AS | | HM6168 |
| Inmos | | | | IMS1420/1421 |
| Mitsubishi | M58725 | | | M5M2168 |
| Motorola | | | MCM2016H | MCM6168/69 |
| NEC | μ PD4016 | μ PD4016CX | | |
| Oki | MSM2128 | | | |

2) CMOS

| Organization | 2K \times 8 | | |
|--------------|---------------|----------------|-------------|
| TOSHIBA | TC5516AP | TC5517AP/BP/CP | TC5518BP/CP |
| Fujitsu | MB8417 | MB8416 | MB8418 |
| Hitachi | | (HM6116) | (HM6117) |
| NEC | μ PD447 | μ PD446 | μ PD449 |
| Oki | MSM5127 | MSM5128 | MSM5129 |

4. 64K Bit Static RAM

| NMOS/CMOS | NMOS | | CMOS | | |
|---------------|----------|--------------|--------------|--------------|--------------|
| Package Width | 0.3 inch | | 0.6 inch | | 0.3 inch |
| TOSHIBA | TMM2063P | TMM2064P | TC5564P | TC5565P | TC5562P |
| Fujitsu | | MB8464 | | MB8464 | HB81C71 |
| Hitachi | HM6264AS | HM6264 | | HM6264 | HM6287 |
| Mitsubishi | | M5M5165 | M5M5164 | M5M5165 | |
| NEC | | μ PD4364 | μ PD4464 | μ PD4364 | μ PD4361 |
| Oki | | MSM5165 | MSM5164 | MSM5165 | |
| Inmos | | | | | IMS1600 |

5. 64K/128K Bit EPROM & Mask ROM

| Organization | 8K \times 8 | | | 16K \times 8 | |
|--------------|---------------|---------------------------|---------------------|----------------|---------------|
| EPROM/MROM | EPROM | MROM | | EPROM | MROM |
| Pins | 28 | 28 | 24 | 28 | 28 |
| TOSHIBA | TMM2764D | TMM2364/65P TC5364/65P | TMM2366P TC5366P | TMM27128D | TMM23128P |
| AMD | Am2764 | | | Am27128 | |
| Fujitsu | MBM2764 | | MB8364 | MBM27128 | — |
| Hitachi | HN482764 | HN61364 | HN48364 | HN4827128 | HN43128 |
| Intel | i2764 | i2364 | | i27128 | — |
| Mitsubishi | M5L2764 | M5M2364 | M58334 | M5L27128 | |
| Mostek | | MK37000 | MK36000 | | |
| Motorola | — | | MCM68364 | | |
| NEC | μ PD2764 | | μ PD2364 | μ PD27128 | μ PD23128 |
| Oki | MSM2764 | MSM3864 | MSM2965 | MSM27128 | MSM38128 |
| TI | — | | TMS4764 | — | |

6. 256K/1M Bit EPROM & Mask ROM

| Organization | 32K \times 8 | | | | 128K \times 8 |
|--------------|----------------|----------------|---------------|----------------|-----------------|
| EPROM/MROM | EPROM | | MROM | | MROM |
| NMOS/CMOS | NMOS | CMOS | NMOS | CMOS | CMOS |
| TOSHIBA | TMM27256D | TC57256D | TMM23256P | TC53257P | TC531000P |
| AMD | (Am27256) | | | | |
| Fujitsu | (MBM27256) | MBM27C256 | | MB83256 | MB831124 |
| Hitachi | (HN27256) | (HN27C256) | | HN613256P | HN62301 |
| Intel | (i27256) | (i27C256) | — | — | — |
| Mitsubishi | — | — | | | M5M231000 |
| NEC | μ PD27256 | μ PD27C256 | μ PD23256 | μ PD23C256 | μ PD231000 |
| Oki | — | — | MSM38256 | MSM53256 | MSM531000 |
| RCA | — | — | | CDM53256 | |

Note: () ; VPP=12.5V

Note: Toshiba does not assume any responsibility for use of any circuitry described; no circuit patent licenses are implied, and Toshiba reserves the right, at any time without notice, to change said circuitry.

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NMOS Dynamic Random Access Memories

TOSHIBA MOS MEMORY PRODUCTS

65,536 WORD × 1 BIT DYNAMIC RAM
N-CHANNEL SILICON GATE MOS

TMM4164AP-12, TMM4164AP-15
TMM4164AP-20

DESCRIPTION

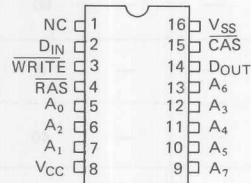
The TMM4164AP is the high speed, low power dynamic RAM organized 65,536 words by 1 bit, it is successor to the industry standard TMM4164P.

The TMM4164AP utilizes TOSHIBA's double poly N-channel Silicon gate process technology as well as advanced circuit techniques to provide wide operating margins, both internally and to the system user.

FEATURES

- 65,536 words by 1 bit organization
- Fast access time and cycle time
- Single power supply of $5V \pm 10\%$ with a built-in V_{BB} generator
- Low power; 275mW operating (MAX.)
22mW standby (MAX.)

PIN CONNECTION (TOP VIEW)



PIN NAMES

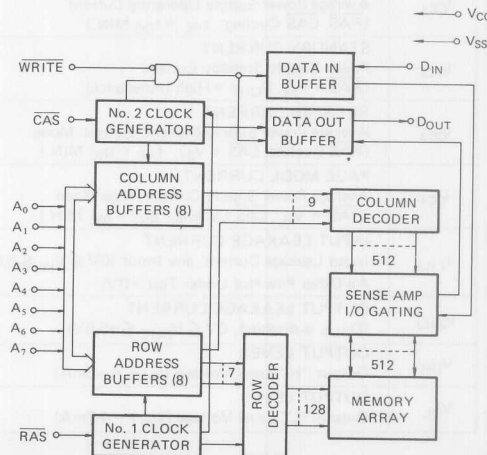
| | |
|----------------|-----------------------|
| $A_0 \sim A_7$ | Address Inputs |
| CAS | Column Address Strobe |
| D_{IN} | Data In |
| NC | No — Connection |
| D_{OUT} | Data Out |
| RAS | Row Address Strobe |
| WRITE | Read/Write Input |
| V_{CC} | Power (+5V) |
| V_{SS} | Ground |

Multiplexed address inputs permit the TMM4164AP to be packaged in a standard 16 pin plastic DIP. This package size provides high system bit densities and is compatible with widely available automated testing and insertion equipment.

System oriented features include single power supply of $5V \pm 10\%$ tolerance, direct interfacing capability with high performance logic families such as Schottky TTL.

- Industry standard 16 pin plastic DIP
- Output unlatched at cycle end allows two-dimensional chip selection
- Common I/O capability using "EARLY WRITE" operation
- Read-Modify-Write, \overline{RAS} -only refresh and Page Mode capability
- All inputs and output TTL compatible
- 128 refresh cycles/2ms

BLOCK DIAGRAM



TMM4164AP-12, TMM4164AP-15 TMM4164AP-20

ABSOLUTE MAXIMUM RATINGS

| ITEM | SYMBOL | RATING | UNITS | NOTES |
|------------------------------|-------------------|-----------|----------|-------|
| Input and Output Voltage | V_{IN}, V_{OUT} | -1 ~ 7 | V | 1 |
| Power Supply Voltage | V_{CC} | -1 ~ 7 | V | 1 |
| Operating Temperature | T_{OPR} | 0 ~ 70 | °C | 1 |
| Storage Temperature | T_{STG} | -55 ~ 150 | °C | 1 |
| Soldering Temperature · Time | T_{SOLDER} | 260 · 10 | °C · sec | 1 |
| Power Dissipation | P_D | 600 | mW | 1 |
| Short Circuit Output Current | I_{OUT} | 50 | mA | 1 |

RECOMMENDED DC OPERATING CONDITIONS (Ta = 0 ~ 70°C)

| SYMBOL | PARAMETER | MIN. | TYP. | MAX. | UNITS | NOTES |
|----------|--------------------|------|------|------|-------|-------|
| V_{CC} | Supply Voltage | 4.5 | 5.0 | 5.5 | V | 2 |
| V_{IH} | Input High Voltage | 2.4 | — | 6.5 | V | 2 |
| V_{IL} | Input Low Voltage | -1.0 | — | 0.8 | V | 2 |

DC ELECTRICAL CHARACTERISTICS ($V_{CC} = 5V \pm 10\%$, Ta = 0 ~ 70°C)

| SYMBOL | PARAMETER | MIN. | TYP. | MAX. | UNITS | NOTES |
|------------|--|------|------|------|---------|-------|
| I_{CC1} | OPERATING CURRENT Average Power Supply Operating Current (RAS, CAS Cycling: $t_{RC} = t_{RC \text{ MIN.}}$) | — | — | 50 | mA | 3,4 |
| I_{CC2} | STANDBY CURRENT Power Supply Standby Current (RAS = V_{IH} , D_{OUT} = High Impedance) | — | — | 4 | mA | |
| I_{CC3} | REFRESH CURRENT Average Power Supply Current, Refresh Mode (RAS Cycling, CAS = V_{IH} : $t_{RC} = t_{RC \text{ MIN.}}$) | — | — | 40 | mA | 3 |
| I_{CC4} | PAGE MODE CURRENT Average Power Supply Current, Page Mode (RAS = V_{IL} , CAS Cycling: $t_{PC} = t_{PC \text{ MIN.}}$) | — | — | 40 | mA | 3, 4 |
| $I_{I(L)}$ | INPUT LEAKAGE CURRENT Input Leakage Current, any Input ($0V \leq V_{IN} \leq 6.5V$, All Other Pins Not Under Test = 0V) | -10 | — | 10 | μA | |
| $I_{O(L)}$ | OUTPUT LEAKAGE CURRENT (D_{OUT} is disabled, $0V \leq V_{OUT} \leq +5.5V$) | -10 | — | 10 | μA | |
| V_{OH} | OUTPUT LEVEL Output "H" Level Voltage ($I_{OUT} = -5mA$) | 2.4 | — | | V | |
| V_{OL} | OUTPUT LEVEL Output "L" Level Voltage ($I_{OUT} = 4.2mA$) | — | — | 0.4 | V | |

TMM4164AP-12, TMM4164AP-15 TMM4164AP-20

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

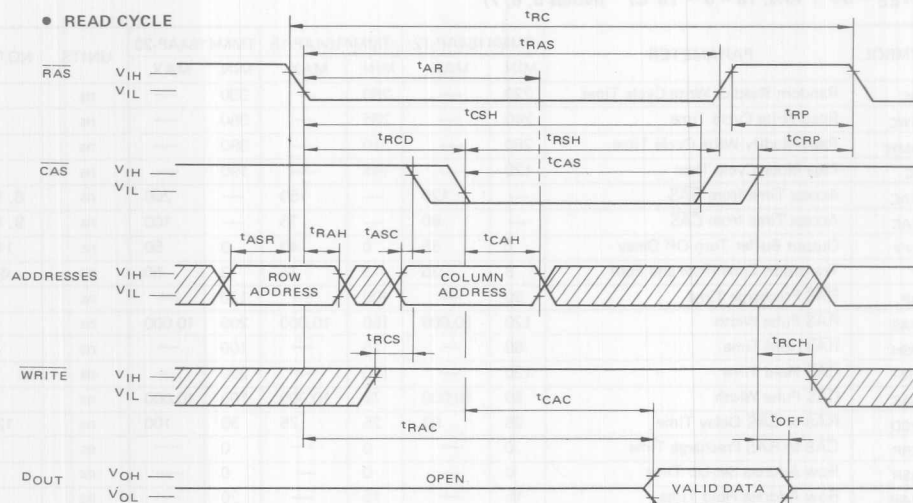
(V_{CC} = 5V ± 10%, T_a = 0 ~ 70°C) (Notes 5, 6, 7)

| SYMBOL | PARAMETER | TMM4164AP-12 | | TMM4164AP-15 | | TMM4164AP-20 | | UNITS | NOTES |
|------------------|---|--------------|--------|--------------|--------|--------------|--------|-------|-------|
| | | MIN. | MAX. | MIN. | MAX. | MIN. | MAX. | | |
| t _{RC} | Random Read or Write Cycle Time | 220 | — | 260 | — | 330 | — | ns | |
| t _{RWC} | Read-Write Cycle Time | 240 | — | 285 | — | 350 | — | ns | |
| t _{RMW} | Read-Modify-Write Cycle Time | 260 | — | 310 | — | 390 | — | ns | |
| t _{PC} | Page Mode Cycle Time | 120 | — | 145 | — | 190 | — | ns | |
| t _{RAC} | Access Time from RAS | — | 120 | — | 150 | — | 200 | ns | 8, 10 |
| t _{CAC} | Access Time from CAS | — | 60 | — | 75 | — | 100 | ns | 9, 10 |
| t _{OFF} | Output Buffer Turn-Off Delay | 0 | 35 | 0 | 40 | 0 | 50 | ns | 11 |
| t _T | Transition Time (Rise and Fall) | 3 | 35 | 3 | 35 | 3 | 50 | ns | 6 |
| t _{RP} | RAS Precharge Time | 90 | — | 100 | — | 120 | — | ns | |
| t _{RAS} | RAS Pulse Width | 120 | 10,000 | 150 | 10,000 | 200 | 10,000 | ns | |
| t _{RSH} | RAS Hold Time | 60 | — | 75 | — | 100 | — | ns | |
| t _{CSH} | CAS Hold Time | 120 | — | 150 | — | 200 | — | ns | |
| t _{CAS} | CAS Pulse Width | 60 | 10,000 | 75 | 10,000 | 100 | 10,000 | ns | |
| t _{RCD} | RAS to CAS Delay Time | 25 | 60 | 25 | 75 | 30 | 100 | ns | 12 |
| t _{CRP} | CAS to RAS Precharge Time | 0 | — | 0 | — | 0 | — | ns | |
| t _{ASR} | Row Address Set-Up Time | 0 | — | 0 | — | 0 | — | ns | |
| t _{RAH} | Row Address Hold Time | 15 | — | 15 | — | 20 | — | ns | |
| t _{ASC} | Column Address Set-Up Time | 0 | — | 0 | — | 0 | — | ns | |
| t _{CAH} | Column Address Hold Time | 35 | — | 45 | — | 55 | — | ns | |
| t _{AR} | Column Address Hold Time Referenced to RAS | 95 | — | 120 | — | 155 | — | ns | |
| t _{RCS} | Read Command Set-Up Time | 0 | — | 0 | — | 0 | — | ns | |
| t _{RCH} | Read Command Hold Time | 0 | — | 0 | — | 0 | — | ns | |
| t _{WCH} | Write Command Hold Time | 35 | — | 45 | — | 55 | — | ns | |
| t _{WCR} | Write Command Hold Time Referenced to RAS | 95 | — | 120 | — | 155 | — | ns | |
| t _{WP} | Write Command Pulse Width | 35 | — | 45 | — | 55 | — | ns | |
| t _{RWL} | Write Command to RAS Lead Time | 35 | — | 45 | — | 55 | — | ns | |
| t _{CWL} | Write Command to CAS Lead Time | 35 | — | 45 | — | 55 | — | ns | |
| t _{DS} | Data-In Set-Up Time | 0 | — | 0 | — | 0 | — | ns | 13 |
| t _{DH} | Data-In Hold Time | 35 | — | 45 | — | 55 | — | ns | 13 |
| t _{DHR} | Data-In Hold Time Referenced to RAS | 95 | — | 120 | — | 155 | — | ns | |
| t _{CP} | CAS Precharge Time (for Page Mode Cycle Only) | 50 | — | 60 | — | 80 | — | ns | |
| t _{REF} | Refresh Period | — | 2 | — | 2 | — | 2 | ms | |
| t _{WCS} | Write Command Set-Up Time | -10 | — | -10 | — | -10 | — | ns | 14 |
| t _{CWD} | CAS to WRITE Delay | 40 | — | 50 | — | 60 | — | ns | 14 |
| t _{RWD} | RAS to WRITE Delay | 100 | — | 125 | — | 160 | — | ns | 14 |

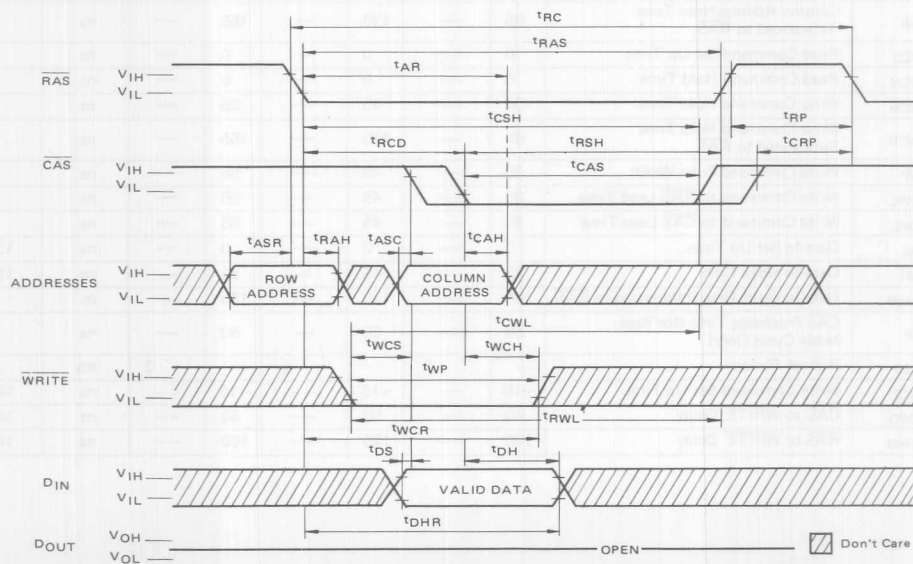
TMM4164AP-12, TMM4164AP-15 TMM4164AP-20

TIMING WAVEFORMS

• READ CYCLE

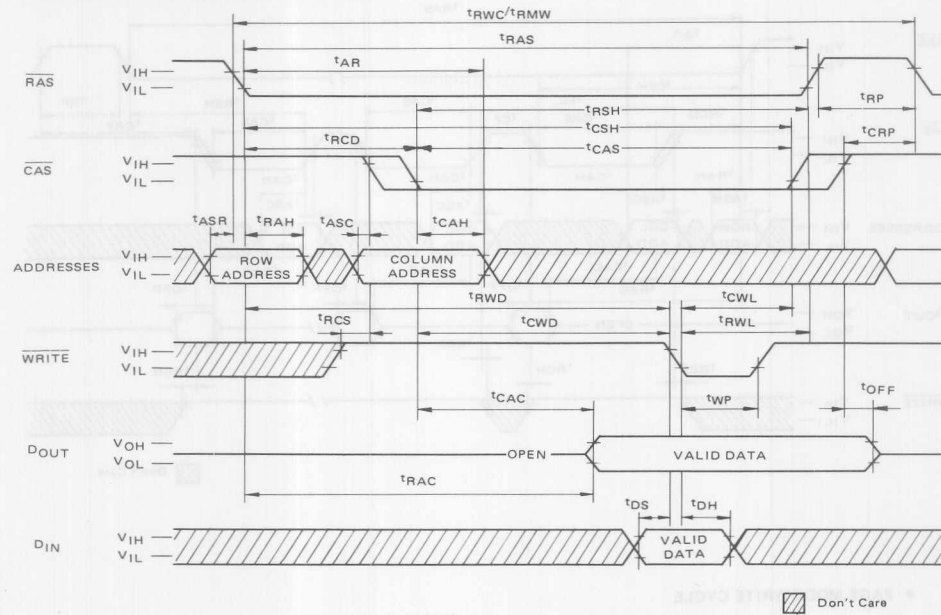


• WRITE CYCLE (EARLY WRITE)

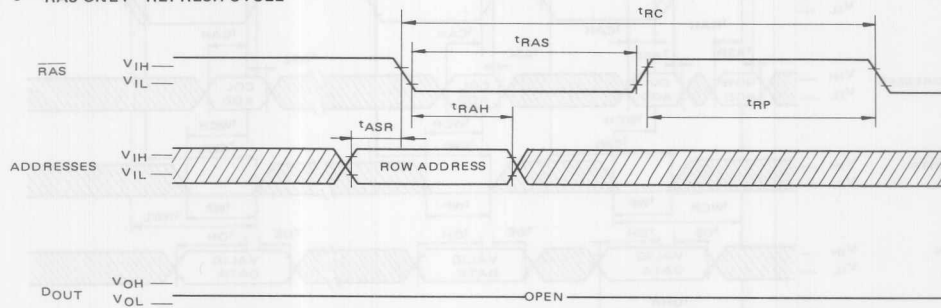


TMM4164AP-12, TMM4164AP-15 TMM4164AP-20

• READ-WRITE/READ-MODIFY-WRITE CYCLE



• "RAS-ONLY" REFRESH CYCLE

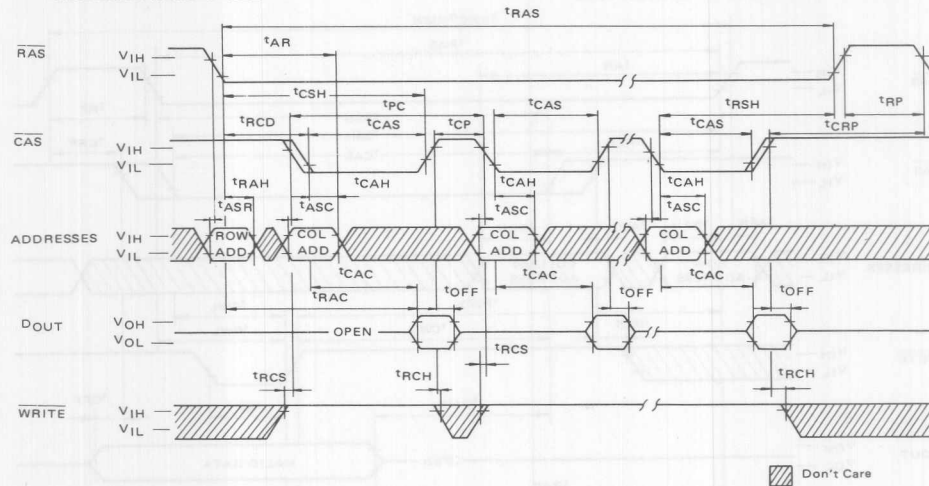


Note: $\overline{CAS} = V_{IH}$, $WRITE = \text{Don't Care}$, $A_7 = \text{Don't Care}$

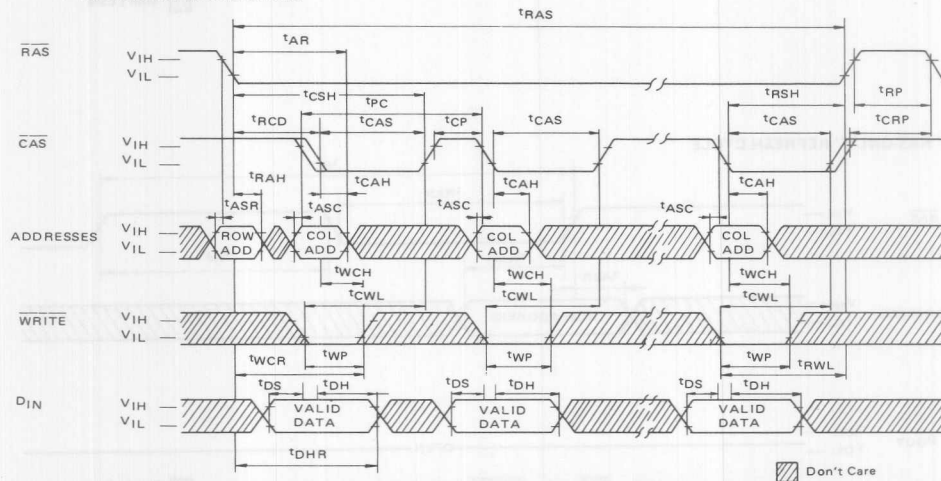
Don't Care

TMM4164AP-12, TMM4164AP-15 TMM4164AP-20

• PAGE MODE READ CYCLE



• PAGE MODE WRITE CYCLE



TMM4164AP-12, TMM4164AP-15 TMM4164AP-20

CAPACITANCE

($V_{CC} = 5V \pm 10\%$, $f = 1\text{MHz}$, $T_a = 0 \sim 70^\circ\text{C}$)

| SYMBOL | PARAMETER | MIN. | TYP. | MAX. | UNITS |
|----------|--|------|------|------|-------|
| C_{I1} | Input Capacitance ($A_0 \sim A_7, D_{IN}$) | — | 4 | 5 | pF |
| C_{I2} | Input Capacitance (RAS, CAS, WRITE) | — | 8 | 10 | pF |
| C_O | Output Capacitance (D_{OUT}) | — | 5 | 7 | pF |

NOTES:

- Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device.
- All voltages are referenced to V_{SS} .
- I_{CC1} , I_{CC3} , I_{CC4} depend on cycle rate.
- I_{CC1} , I_{CC4} depend on output loading. Specified values are obtained with the output open.
- An initial pause of $200\mu\text{s}$ is required after power-up followed by any 8 RAS cycles before proper device operation is achieved.
- AC measurements assume $t_T = 5\text{ns}$.
- V_{IH} (min.) and V_{IL} (max.) are reference levels for measuring timing of input signals. Also, transition times are measured between V_{IH} and V_{IL} .
- Assumes that $t_{RCD} \leq t_{RCD}(\text{max.})$. If t_{RCD} is greater than the maximum recommended value shown in this table, t_{RAC} will increase by the amount that t_{RCD} exceeds the value shown.
- Assumes that $t_{RCD} \geq t_{RCD}(\text{max.})$.
- Measured with a load equivalent to 2 TTL loads and 100pF .
- $t_{OFF}(\text{max.})$ defines the time at which the output achieves the open circuit condition and is not referenced to output voltage levels.
- Operation within the $t_{RCD}(\text{max.})$ limit insures that $t_{RAC}(\text{max.})$ can be met. $t_{RCD}(\text{max.})$ is specified as a reference point only: If t_{RCD} is greater than the specified $t_{RCD}(\text{max.})$ limit, then access time is controlled exclusively by t_{CAC} .
- These parameters are referenced to CAS leading edge in early write cycles and to WRITE leading edge in read-write or read-modify-write cycles.
- t_{WCS} , t_{CWD} and t_{RWD} are not restrictive operating parameters. They are included in the data sheet as electrical characteristics only. If $t_{WCS} \geq t_{WCS}(\text{min.})$, the cycle is an early write cycle and the data out pin will remain open circuit (high impedance) throughout the entire cycle:
If $t_{CWD} \geq t_{CWD}(\text{min.})$ and $t_{RWD} \geq t_{RWD}(\text{min.})$, the cycle is a read-write cycle and the data out will contain data read from the selected cell: If neither of the above sets of conditions is satisfied, the condition of the data out (at access time) is indeterminate.

APPLICATION INFORMATION

ADDRESSING

The 16 address bits required to decode 1 of the 65,536 cell locations within the TMM4164AP are multiplexed onto the 8 address inputs and latched into the on-chip address latches by externally applying two negative going TTL-level clocks.

The first clock, the Row Address Strobe ($\overline{\text{RAS}}$), latches the 8 row address bits into the chip. The second clock, the Column Address Strobe ($\overline{\text{CAS}}$), subsequently latches the 8 column address bits into the chip. Each of these signals, RAS and CAS, triggers a sequence of events which are controlled by different

delayed internal clocks.

The two clock chains are linked together logically in such a way that the address multiplexing operation is done outside of the critical path timing sequence for read data access. The later events in the CAS clock sequence are inhibited until the occurrence of a delayed signal derived from the $\overline{\text{RAS}}$ clock chain. This "gated CAS" feature allows the CAS clock to be externally activated as soon as the Row Address Hold Time specification (t_{RAH}) has been satisfied and the address inputs have been changed from Row address to Column address information.

TMM4164AP-12, TMM4164AP-15 TMM4164AP-20

DATA INPUT/OUTPUT

Data to be written into a selected cell is latched into an on-chip register by a combination of WRITE and $\overline{\text{CAS}}$ while $\overline{\text{RAS}}$ is active. The later of the signals (WRITE or $\overline{\text{CAS}}$) to make its negative transition is the strobe for the Data In (D_{IN}) register. This permits several options in the write cycle timing. In a write cycle, if the WRITE input is brought low (active) prior to $\overline{\text{CAS}}$, the D_{IN} is strobed by $\overline{\text{CAS}}$ and the set-up and hold times are referenced to $\overline{\text{CAS}}$. If the input data is not available at $\overline{\text{CAS}}$ time or if it is desired that the cycle be a read-write cycle, the WRITE signal will be delayed until after $\overline{\text{CAS}}$ has made its negative transition. In this "delayed write cycle" the data input set-up and hold times are referenced to the negative edge of WRITE rather than $\overline{\text{CAS}}$. (To illustrate this feature, D_{IN} is referenced to WRITE in the timing diagrams depicting the read-write and page mode write cycles while the "early write" cycle diagram shows D_{IN} referenced to $\overline{\text{CAS}}$).

Data is retrieved from the memory in a read cycle by maintaining WRITE in the inactive or high state throughout the portion of the memory cycle in which $\overline{\text{CAS}}$ is active (low). Data read from the selected cell will be available at the output within the specified access time.

DATA OUTPUT CONTROL

The normal condition of the Data Output (D_{OUT}) of the TMM4164AP is the high impedance (open cir-

cuit) state. That is to say, anytime $\overline{\text{CAS}}$ is at a high level, the D_{OUT} pin will be floating. The only time the output will turn on and contain either a logic 0 or logic 1 is at access time during a read cycle. D_{OUT} will remain valid from access time until $\overline{\text{CAS}}$ is taken back to the inactive (high level) condition.

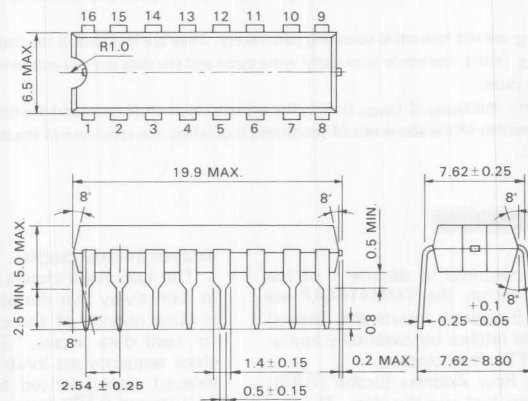
PAGE MODE

The "Page-Mode" feature of the TMM4164AP allows for successive memory operations at multiple column locations of the same row address with increased speed without an increase in power. This is done by strobing the row address into the chip and maintaining the $\overline{\text{RAS}}$ signal at a logic 0 throughout all successive memory cycles in which the row address is common. This "Page-Mode" of operation will not dissipate the power associated with the negative going edge of $\overline{\text{RAS}}$. Also, the time required for strobing in a new row address is eliminated, thereby decreasing the access and cycle times.

REFRESH

Refresh of the dynamic cell matrix is accomplished by performing a memory cycle at each of the 128 row address ($\text{A}_0 \sim \text{A}_6$) within each 2 millisecond time interval. Although any normal memory cycle will perform the refresh operation, this function is most easily accomplished with "RAS-only" cycles, $\overline{\text{RAS}}$ only refresh results in a substantial reduction in operating power. This reduction in power is reflected in the I_{CC3} specification.

OUTLINE DRAWINGS



Note: Each lead pitch is 2.54mm. All leads are located within 0.25mm of their true longitudinal position with respect to No. 1 and No. 16 leads. All dimensions are in millimeters.

Note: Toshiba does not assume any responsibility for use of any circuitry described; no circuit patent licenses are implied, and Toshiba reserves the right, at any time without notice, to change said circuitry.

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TOSHIBA MOS MEMORY PRODUCTS

262,144 WORD × 1 BIT DYNAMIC RAM
N-CHANNEL SILICON GATE MOS

TMM41256C-12, TMM41256C-15
TMM41256C-20

DESCRIPTION

The TMM41256C is the new generation dynamic RAM organized 262,144 words by 1 bit, it is successor to the industry standard TMM4164AP.

The TMM41256C utilizes TOSHIBA's N-channel Silicon gate process technology as well as advanced circuit techniques to provide wide operating margins, both internally and to the system user.

Multiplexed address inputs permit the TMM-

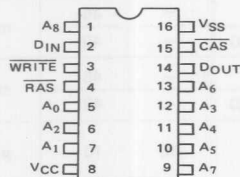
41256C to be packaged in a standard 16 pin ceramic DIP. This package size provides high system bit densities and is compatible with widely available automated testing and insertion equipment.

System oriented features include single power supply of 5V ±10% tolerance, direct interfacing capability with high performance logic families such as Schottky TTL.

FEATURES

- 262,144 words by 1 bit organization
 - Fast access time and cycle time
- | DEVICE | t _{RAC} | t _{CAC} | t _{RC} |
|--------------|------------------|------------------|-----------------|
| TMM41256C-12 | 120 ns | 60 ns | 220 ns |
| TMM41256C-15 | 150 ns | 75 ns | 260 ns |
| TMM41256C-20 | 200 ns | 100 ns | 330 ns |
- Single power supply of 5V ±10% with a built-in V_{BB} generator
 - Low Power:
 - 330mW Operating (MAX.) (TMM41256C-12)
 - 275mW Operating (MAX.) (TMM41256C-15/-20)
 - 28mW Standby (MAX.)

PIN CONNECTION (TOP VIEW)

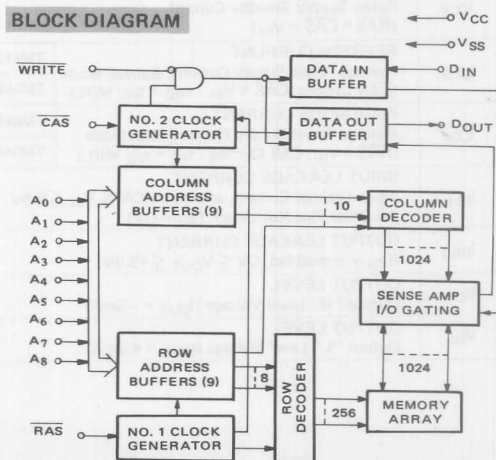


PIN NAMES

| | |
|---------------------------------|-----------------------|
| A ₀ ~ A ₈ | Address Inputs |
| CAS | Column Address Strobe |
| D _{IN} | Data In |
| D _{OUT} | Data Out |
| RAS | Row Address Strobe |
| WRITE | Read/Write Input |
| V _{CC} | Power (+5V) |
| V _{SS} | Ground |

- Industry standard 16 pin ceramic DIP
- Output unlatched at cycle end allows two-dimensional chip selection
- Common I/O capability using "EARLY WRITE" operation
- Read-Modify-Write, RAS-only refresh, Hidden refresh, and Page Mode capability.
- All inputs and output TTL compatible
- 256 refresh cycles/4ms

BLOCK DIAGRAM



TMM41256C-12, TMM41256C-15 TMM41256C-20

ABSOLUTE MAXIMUM RATINGS

| ITEM | SYMBOL | RATING | UNITS | NOTES |
|------------------------------|-------------------|----------------|-------------------------------------|-------|
| Input and Output Voltage | V_{IN}, V_{OUT} | $-1 \sim 7$ | V | 1 |
| Power Supply Voltage | V_{CC} | $-1 \sim 7$ | V | 1 |
| Operating Temperature | T_{OPR} | $0 \sim 70$ | $^{\circ}\text{C}$ | 1 |
| Storage Temperature | T_{STG} | $-55 \sim 150$ | $^{\circ}\text{C}$ | 1 |
| Soldering Temperature · Time | T_{SOLDER} | $260 \cdot 10$ | $^{\circ}\text{C} \cdot \text{sec}$ | 1 |
| Power Dissipation | P_D | 1 | W | 1 |
| Short Circuit Output Current | I_{OUT} | 50 | mA | 1 |

RECOMMENDED DC OPERATING CONDITIONS ($T_a = 0 \sim 70^{\circ}\text{C}$)

| SYMBOL | PARAMETER | MIN. | TYP. | MAX. | UNITS | NOTES |
|----------|--------------------|------|------|------|-------|-------|
| V_{CC} | Supply Voltage | 4.5 | 5.0 | 5.5 | V | 2 |
| V_{IH} | Input High Voltage | 2.4 | — | 6.5 | V | 2 |
| V_{IL} | Input Low Voltage | -1.0 | — | 0.8 | V | 2 |

DC ELECTRICAL CHARACTERISTICS ($V_{CC} = 5V \pm 10\%$, $T_a = 0 \sim 70^{\circ}\text{C}$)

| SYMBOL | PARAMETER | | MIN. | MAX. | UNITS | NOTES |
|-------------------|--|------------------|------|------|-------|-------|
| I _{CC1} | OPERATING CURRENT Average Power Supply Operating Current (RAS, CAS Cycling: t _{RC} = t _{RC} MIN.) | TMM41256C-12 | — | 60 | mA | 3, 4 |
| | | TMM41256C-15/-20 | — | 50 | | |
| I _{CC2} | STANDBY CURRENT Power Supply Standby Current (RAS = CAS = V _{IH}) | | — | 5 | mA | |
| I _{CC3} | REFRESH CURRENT Average Power Supply Current, Refresh Mode (RAS Cycling, CAS = V _{IH} : t _{RC} = t _{RC} MIN.) | TMM41256C-12 | — | 45 | mA | 3 |
| | | TMM41256C-15/-20 | — | 40 | | |
| I _{CC4} | PAGE MODE CURRENT Average Power Supply Current, Page Mode (RAS = V _{IL} , CAS Cycling : t _{PC} = t _{PC} MIN.) | TMM41256C-12 | — | 45 | mA | 3, 4 |
| | | TMM41256C-15/-20 | — | 40 | | |
| I _{I(L)} | INPUT LEAKAGE CURRENT Input Leakage Current, any input (OV ≤ V _{IN} ≤ 6.5V, All Other Pins Not Under Test = OV) | | −10 | 10 | μA | |
| I _{O(L)} | OUTPUT LEAKAGE CURRENT (D _{OUT} is disabled, OV ≤ V _{OUT} ≤ +5.5V) | | −10 | 10 | μA | |
| V _{OH} | OUTPUT LEVEL Output “H” Level Voltage (I _{OUT} = −5mA) | | 2.4 | — | V | |
| V _{OL} | OUTPUT LEVEL Output “L” Level Voltage (I _{OUT} = 4.2mA) | | — | 0.4 | V | |

TMM41256C-12, TMM41256C-15 TMM41256C-20

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

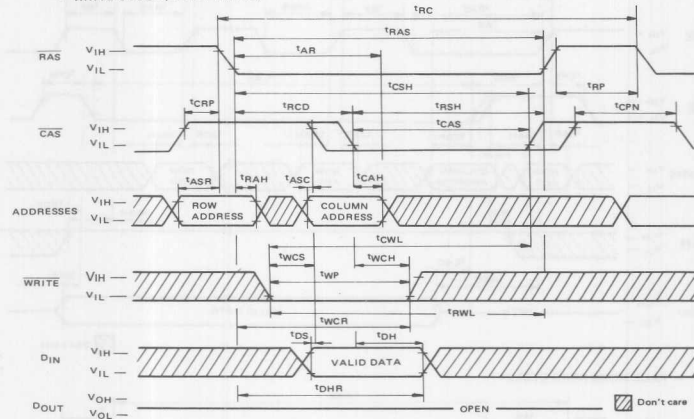
(V_{CC} = 5V ± 10%, T_a = 0 ~ 70°C) (Notes 5, 6, 7)

| SYMBOL | PARAMETER | TMM41256C-12 | | TMM41256C-15 | | TMM41256C-20 | | UNITS | NOTES |
|------------------|---|--------------|--------|--------------|--------|--------------|--------|-------|-------|
| | | MIN. | MAX. | MIN. | MAX. | MIN. | MAX. | | |
| t _{RC} | Random Read or Write Cycle Time | 220 | — | 260 | — | 330 | — | ns | |
| t _{RWC} | Read-Write Cycle Time | 240 | — | 285 | — | 350 | — | ns | |
| t _{RMW} | Read-Modify-Write Cycle Time | 260 | — | 310 | — | 390 | — | ns | |
| t _{PC} | Page Mode Cycle Time | 120 | — | 145 | — | 190 | — | ns | |
| t _{RAC} | Access Time from RAS | — | 120 | — | 150 | — | 200 | ns | 8, 10 |
| t _{CAC} | Access Time from CAS | — | 60 | — | 75 | — | 100 | ns | 9, 10 |
| t _{OFF} | Output Buffer Turn-Off Delay | 0 | 35 | 0 | 40 | 0 | 50 | ns | 11 |
| t _T | Transition Time (Rise and Fall) | 3 | 50 | 3 | 50 | 3 | 50 | ns | 6 |
| t _{RP} | RAS Precharge Time | 90 | — | 100 | — | 120 | — | ns | |
| t _{RAS} | RAS Pulse Width | 120 | 10,000 | 150 | 10,000 | 200 | 10,000 | ns | |
| t _{RSH} | RAS Hold Time | 60 | — | 75 | — | 100 | — | ns | |
| t _{CSH} | CAS Hold Time | 120 | — | 150 | — | 200 | — | ns | |
| t _{CAS} | CAS Pulse Width | 60 | 10,000 | 75 | 10,000 | 100 | 10,000 | ns | |
| t _{RCD} | RAS to CAS Delay Time | 25 | 60 | 25 | 75 | 30 | 100 | ns | 13 |
| t _{CRP} | CAS to RAS Precharge Time | 0 | — | 0 | — | 0 | — | ns | |
| t _{CPN} | CAS Precharge Time | 25 | — | 25 | — | 30 | — | ns | |
| t _{CP} | CAS Precharge Time (for Page Mode Cycle Only) | 50 | — | 60 | — | 80 | — | ns | |
| t _{ASR} | Row Address Set-Up Time | 0 | — | 0 | — | 0 | — | ns | |
| t _{RAH} | Row Address Hold Time | 15 | — | 15 | — | 20 | — | ns | |
| t _{ASC} | Column Address Set-Up Time | 0 | — | 0 | — | 0 | — | ns | |
| t _{CAH} | Column Address Hold Time | 35 | — | 45 | — | 55 | — | ns | |
| t _{AR} | Column Address Hold Time Referenced to RAS | 95 | — | 120 | — | 155 | — | ns | |
| t _{RCS} | Read Command Set-Up Time | 0 | — | 0 | — | 0 | — | ns | |
| t _{RCH} | Read Command Hold Time Referenced to CAS | 0 | — | 0 | — | 0 | — | ns | |
| t _{RRH} | Read Command Hold Time Referenced to RAS | 15 | — | 20 | — | 25 | — | ns | 12 |
| t _{WCH} | Write Command Hold Time | 35 | — | 45 | — | 55 | — | ns | |
| t _{WCR} | Write Command Hold Time Referenced to RAS | 95 | — | 120 | — | 155 | — | ns | |
| t _{WP} | Write Command Pulse Width | 35 | — | 45 | — | 55 | — | ns | |
| t _{RWL} | Write Command to RAS Lead Time | 35 | — | 45 | — | 55 | — | ns | |
| t _{CWL} | Write Command to CAS Lead Time | 35 | — | 45 | — | 55 | — | ns | |
| t _{DS} | Data-In Set-Up Time | 0 | — | 0 | — | 0 | — | ns | 14 |
| t _{DH} | Data-In Hold Time | 35 | — | 45 | — | 55 | — | ns | 14 |
| t _{DHR} | Data-In Hold Time Referenced to RAS | 95 | — | 120 | — | 155 | — | ns | |
| t _{REF} | Refresh Period | — | 4 | — | 4 | — | 4 | ms | |
| t _{WCS} | Write Command Set-Up Time | -10 | — | -10 | — | -10 | — | ns | 15 |
| t _{CWD} | CAS to WRITE Delay | 40 | — | 50 | — | 60 | — | ns | 15 |
| t _{RWD} | RAS to WRITE Delay | 100 | — | 125 | — | 160 | — | ns | 15 |

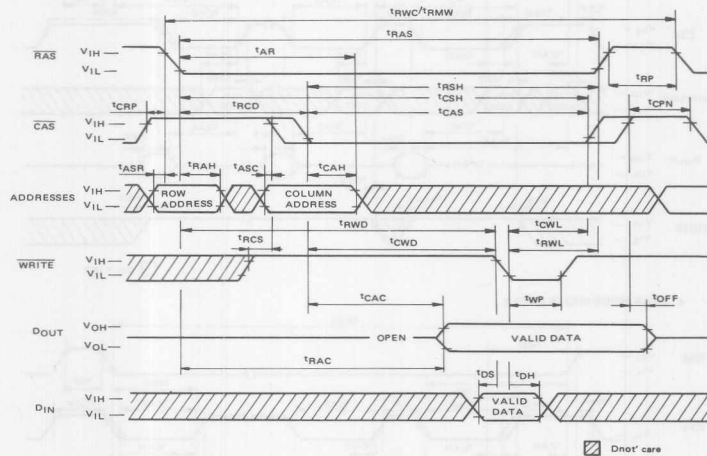


**TMM41256C-12, TMM41256C-15
TMM41256C-20**

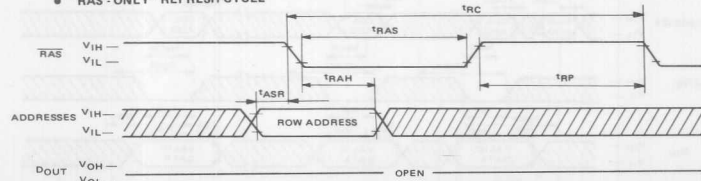
- WRITE CYCLE (EARLY WRITE)



•READ-WRITE/READ-MODIFY-WRITE CYCLE



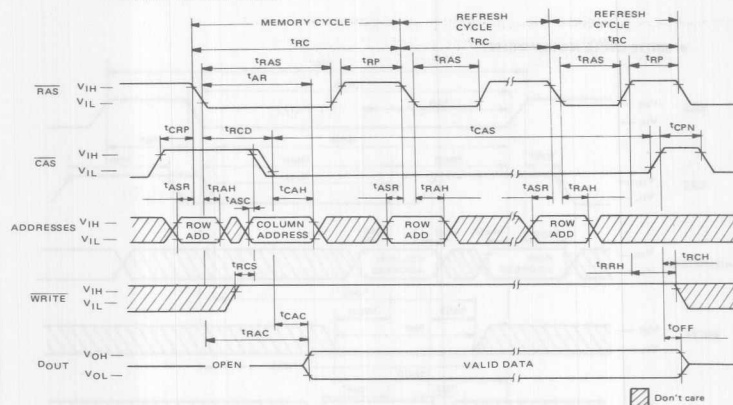
- "RAS - ONLY" REFRESH CYCLE



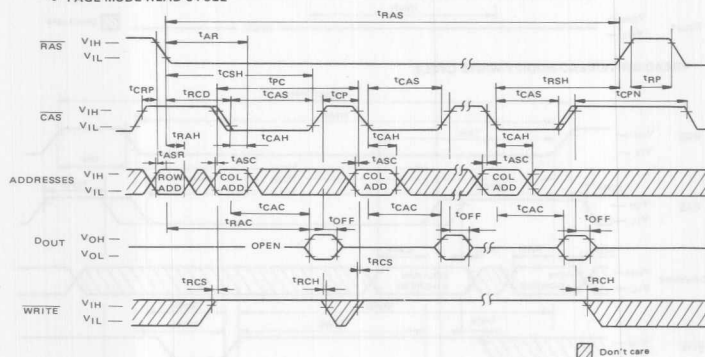
Note: $\overline{\text{CAS}} = V_{IH}$, $\overline{\text{WRITE}} = \text{Don't care}$, $A_8 = \text{Don't care}$

TMM41256C-12, TMM41256C-15 TMM41256C-20

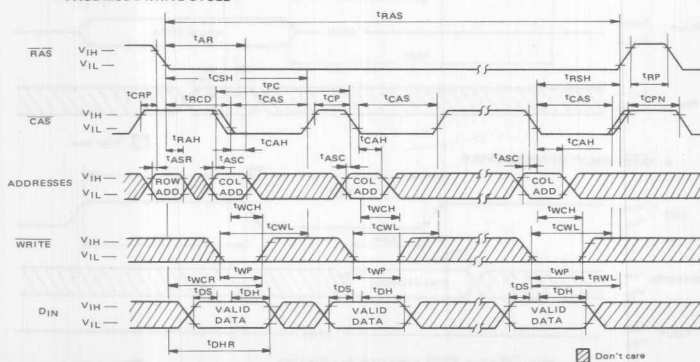
• HIDDEN REFRESH CYCLE



• PAGE MODE READ CYCLE



• PAGE MODE WRITE CYCLE



APPLICATION INFORMATION

ADDRESSING

The 18 address bits required to decode 1 of the 262,144 cell locations within the TMM41256C are multiplexed onto the 9 address inputs and latched into the on-chip address latches by externally applying two negative going TTL-level clocks.

The first clock, the Row Address Strobe ($\overline{\text{RAS}}$), latches the 9 row address bits into the chip. The second clock, the Column Address Strobe ($\overline{\text{CAS}}$), subsequently latches the 9 column address bits into the chip. Each of these signals, $\overline{\text{RAS}}$ and $\overline{\text{CAS}}$, triggers a sequence of events which are controlled by different delayed internal clocks.

The two clock chains are linked together logically in such a way that the address multiplexing operation is done outside of the critical path timing sequence for read data access. The later events in the $\overline{\text{CAS}}$ clock sequence are inhibited until the occurrence of a delayed signal derived from the $\overline{\text{RAS}}$ clock chain. This "gated $\overline{\text{CAS}}$ " feature allows the $\overline{\text{CAS}}$ clock to be externally activated as soon as the Row Address Hold Time specification (t_{RAH}) has been satisfied and the address inputs have been changed from Row address to Column address information.

DATA INPUT/OUTPUT

Data to be written into a selected cell is latched into an on-chip register by a combination of $\overline{\text{WRITE}}$ and $\overline{\text{CAS}}$ while $\overline{\text{RAS}}$ is active. The later of the signals ($\overline{\text{WRITE}}$ or $\overline{\text{CAS}}$) to make its negative transition is the strobe for the Data In (D_{IN}) register. This permits several options in the write cycle timing. In a write cycle, if the $\overline{\text{WRITE}}$ input is brought low (active) prior to $\overline{\text{CAS}}$, the D_{IN} is strobed by $\overline{\text{CAS}}$ and the set-up and hold times are referenced to $\overline{\text{CAS}}$. If the input data is not available at $\overline{\text{CAS}}$ time or if it is desired that the cycle be a read-write cycle, the $\overline{\text{WRITE}}$ signal will be delayed until after $\overline{\text{CAS}}$ has made its negative transition. In this "delayed write cycle" the data input set-up and hold times are referenced to the negative edge of $\overline{\text{WRITE}}$ rather than $\overline{\text{CAS}}$. (To illustrate this feature, D_{IN} is referenced to $\overline{\text{WRITE}}$ in the timing diagrams depicting the read-write and page mode write cycles while the "early write" cycle diagram shows D_{IN} referenced to $\overline{\text{CAS}}$).

Data is retrieved from the memory in a read

cycle by maintaining $\overline{\text{WRITE}}$ in the inactive or high state throughout the portion of the memory cycle in which $\overline{\text{CAS}}$ is active (low). Data read from the selected cell will be available at the output within the specified access time.

DATA OUTPUT CONTROL

The normal condition of the Data Output (D_{OUT}) of the TMM41256C is the high impedance (open circuit) state. This is to say, anytime $\overline{\text{CAS}}$ is at a high level, the D_{OUT} pin will be floating. The only time the output will turn on and contain either a logic 0 or logic 1 is at access time during a read cycle. D_{OUT} will remain valid from access time until $\overline{\text{CAS}}$ is taken back to the inactive (high level) condition.

PAGE MODE

The "Page-Mode" feature of the TMM41256C allows for successive memory operations at multiple column locations of the same row address with increased speed without an increase in power. This is done by strobing the row address into the chip and maintaining the $\overline{\text{RAS}}$ signal at a logic 0 throughout all successive memory cycles in which the row address is common. This "Page Mode" of operation will not dissipate the power associated with the negative going edge of $\overline{\text{RAS}}$. Also, the time required for strobing in a new row address is eliminated, thereby decreasing the access and cycle times.

REFRESH

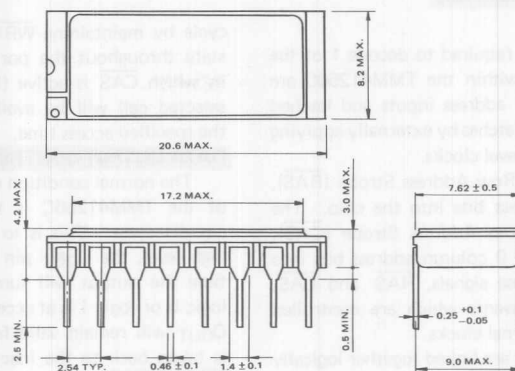
Refresh of the dynamic cell matrix is accomplished by performing a memory cycle at each of the 256 row address ($\text{A}_0 \sim \text{A}_7$) within each 4 millisecond time interval. Although any normal memory cycle will perform the refresh operation, this function is most easily accomplished with " $\overline{\text{RAS}}$ - only" cycles, $\overline{\text{RAS}}$ only refresh results in a substantial reduction in operating power. This reduction in power is reflected in the I_{CC3} specification.

HIDDEN REFRESH

An optional feature of the TMM41256C is that refresh cycles may be performed while maintaining valid data at the output pin. This is referred to as Hidden Refresh. Hidden Refresh is performed by holding $\overline{\text{CAS}}$ at V_{IL} and taking $\overline{\text{RAS}}$ high and after a specified precharge period (t_{RP}), executing a " $\overline{\text{RAS}}$ - only" refresh cycle, but with $\overline{\text{CAS}}$ held low.

TMM41256C-12, TMM41256C-15 TMM41256C-20

OUTLINE DRAWINGS



Note : Each lead pitch is 2.54mm. All leads are located within 0.25mm of their true longitudinal position with respect to No. 1 and No. 16 leads. All dimensions are in millimeters.

Note: Toshiba does not assume any responsibility for use of any circuitry described; no circuit patent licenses are implied, and Toshiba reserves the right, at any time without notice, to change said circuitry.

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TOSHIBA MOS MEMORY PRODUCTS

262,144 WORD \times 1 BIT DYNAMIC RAM
N-CHANNEL SILICON GATE MOS

TMM41256P-12
TMM41256P-15

DESCRIPTION

The TMM41256P is the new generation dynamic RAM organized 262,144 words by 1 bit, it is successor to the industry standard TMM4164AP.

The TMM41256P utilizes TOSHIBA's N-channel Silicon gate process technology as well as advanced circuit techniques to provide wide operating margins, both internally and to the system user.

Multiplexed address inputs permit the TMM-

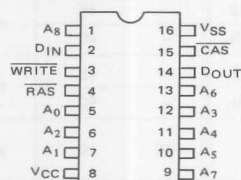
FEATURES

- 262,144 words by 1 bit organization
- Fast access time and cycle time

| DEVICE | t_{RAC} | t_{CAC} | t_{RC} |
|--------------|-----------|-----------|----------|
| TMM41256P-12 | 120 ns | 60 ns | 220 ns |
| TMM41256P-15 | 150 ns | 75 ns | 260 ns |

- Single power supply of 5V $\pm 10\%$ with a built-in V_{BB} generator
- Low Power:
 - 330mW Operating (MAX.) (TMM41256P-12)
 - 275mW Operating (MAX.) (TMM41256P-15)
 - 28mW Stand by (MAX.)

PIN CONNECTION (TOP VIEW)



PIN NAMES

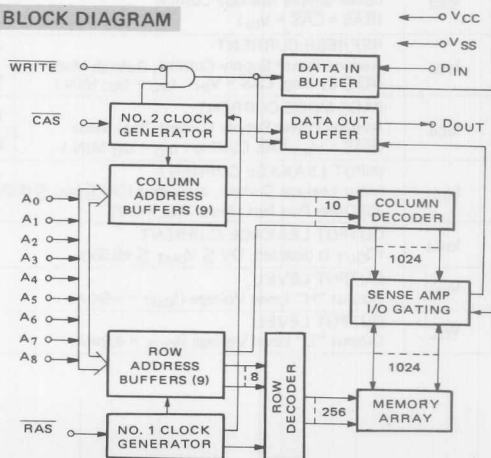
| | |
|---------------------------------|-----------------------|
| A ₀ ~ A ₈ | Address Inputs |
| CAS | Column Address Strobe |
| D _{IN} | Data In |
| D _{OUT} | Data Out |
| RAS | Row Address Strobe |
| WRITE | Read/Write Input |
| V _{CC} | Power (+5V) |
| V _{SS} | Ground |

41256P to be packaged in a standard 16 pin plastic DIP. This package size provides high system bit densities and is compatible with widely available automated testing and insertion equipment.

System oriented features include single power supply of $5V \pm 10\%$ tolerance, direct interfacing capability with high performance logic families such as Schottky TTL.

- Industry standard 16 pin plastic DIP
- Output unlatched at cycle end allows two-dimensional chip selection
- Common I/O capability using "EARLY WRITE" operation
- Read-Modify-Write, $\overline{\text{RAS}}$ -only refresh, Hidden refresh, and Page Mode capability.
- All inputs and output TTL compatible
- 256 refresh cycles/4ms

BLOCK DIAGRAM



TMM41256P-12

TMM41256P-15

ABSOLUTE MAXIMUM RATINGS

| ITEM | SYMBOL | RATING | UNITS | NOTES |
|------------------------------|-------------------|----------------|-------------------------------------|-------|
| Input and Output Voltage | V_{IN}, V_{OUT} | $-1 \sim 7$ | V | 1 |
| Power Supply Voltage | V_{CC} | $-1 \sim 7$ | V | 1 |
| Operating Temperature | T_{OPR} | $0 \sim 70$ | $^{\circ}\text{C}$ | 1 |
| Storage Temperature | T_{STG} | $-55 \sim 150$ | $^{\circ}\text{C}$ | 1 |
| Soldering Temperature - Time | T_{SOLDER} | $260 \cdot 10$ | $^{\circ}\text{C} \cdot \text{sec}$ | 1 |
| Power Dissipation | P_D | 600 | mW | 1 |
| Short Circuit Output Current | I_{OUT} | 50 | mA | 1 |

RECOMMENDED DC OPERATING CONDITIONS ($T_a = 0 \sim 70^{\circ}\text{C}$)

| SYMBOL | PARAMETER | MIN. | TYP. | MAX. | UNITS | NOTES |
|----------|--------------------|------|------|------|-------|-------|
| V_{CC} | Supply Voltage | 4.5 | 5.0 | 5.5 | V | 2 |
| V_{IH} | Input High Voltage | 2.4 | — | 6.5 | V | 2 |
| V_{IL} | Input Low Voltage | -1.0 | — | 0.8 | V | 2 |

DC ELECTRICAL CHARACTERISTICS ($V_{CC} = 5V \pm 10\%$, $T_a = 0 \sim 70^{\circ}\text{C}$)

| SYMBOL | PARAMETER | MIN. | MAX. | UNITS | NOTES |
|------------|--|--------------|------|---------------|----------|
| I_{CC1} | OPERATING CURRENT Average Power Supply Operating Current (RAS, CAS Cycling: $t_{RC} = t_{RC} \text{ MIN.}$) | TMM41256P-12 | — | 60 | mA, 3, 4 |
| | | TMM41256P-15 | — | 50 | |
| I_{CC2} | STANDBY CURRENT Power Supply Standby Current (RAS = CAS = V_{IH}) | — | 5 | mA | |
| I_{CC3} | REFRESH CURRENT Average Power Supply Current, Refresh Mode (RAS Cycling, CAS = V_{IH} : $t_{RC} = t_{RC} \text{ MIN.}$) | TMM41256P-12 | — | 45 | mA, 3 |
| | | TMM41256P-15 | — | 40 | |
| I_{CC4} | PAGE MODE CURRENT Average Power Supply Current, Page Mode (RAS = V_{IL} , CAS Cycling: $t_{PC} = t_{PC} \text{ MIN.}$) | TMM41256P-12 | — | 45 | mA, 3, 4 |
| | | TMM41256P-15 | — | 40 | |
| $I_{I(L)}$ | INPUT LEAKAGE CURRENT Input Leakage Current, any input ($0V \leq V_{IN} \leq 6.5V$, All Other Pins Not Under Test = 0V) | -10 | 10 | μA | |
| $I_{O(L)}$ | OUTPUT LEAKAGE CURRENT (D_{OUT} is disabled, $0V \leq V_{OUT} \leq +5.5V$) | -10 | 10 | μA | |
| V_{OH} | OUTPUT LEVEL Output "H" Level Voltage ($I_{OUT} = -5\text{mA}$) | 2.4 | — | V | |
| V_{OL} | OUTPUT LEVEL Output "L" Level Voltage ($I_{OUT} = 4.2\text{mA}$) | — | 0.4 | V | |

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

(V_{CC} = 5V ± 10%, T_a = 0 ~ 70°C) (Notes 5, 6, 7)

| SYMBOL | PARAMETER | TMM41256P-12 | | TMM41256P-15 | | UNITS | NOTES |
|------------------|---|--------------|--------|--------------|--------|-------|-------|
| | | MIN. | MAX. | MIN. | MAX. | | |
| t _{RC} | Random Read or Write Cycle Time | 220 | — | 260 | — | ns | |
| t _{RWC} | Read-Write Cycle Time | 240 | — | 285 | — | ns | |
| t _{RMW} | Read-Modify-Write Cycle Time | 260 | — | 310 | — | ns | |
| t _{PC} | Page Mode Cycle Time | 120 | — | 145 | — | ns | |
| t _{RAC} | Access Time from $\overline{\text{RAS}}$ | — | 120 | — | 150 | ns | 8, 10 |
| t _{CAC} | Access Time from $\overline{\text{CAS}}$ | — | 60 | — | 75 | ns | 9, 10 |
| t _{OFF} | Output Buffer Turn-Off Delay | 0 | 35 | 0 | 40 | ns | 11 |
| t _T | Transition Time (Rise and Fall) | 3 | 50 | 3 | 50 | ns | 6 |
| t _{RP} | $\overline{\text{RAS}}$ Precharge Time | 90 | — | 100 | — | ns | |
| t _{RAS} | $\overline{\text{RAS}}$ Pulse Width | 120 | 10,000 | 150 | 10,000 | ns | |
| t _{RSH} | $\overline{\text{RAS}}$ Hold Time | 60 | — | 75 | — | ns | |
| t _{CSH} | $\overline{\text{CAS}}$ Hold Time | 120 | — | 150 | — | ns | |
| t _{CAS} | $\overline{\text{CAS}}$ Pulse Width | 60 | 10,000 | 75 | 10,000 | ns | |
| t _{RCD} | $\overline{\text{RAS}}$ to $\overline{\text{CAS}}$ Delay Time | 25 | 60 | 25 | 75 | ns | 13 |
| t _{CRP} | $\overline{\text{CAS}}$ to $\overline{\text{RAS}}$ Precharge Time | 0 | — | 0 | — | ns | |
| t _{CPN} | $\overline{\text{CAS}}$ Precharge Time | 25 | — | 25 | — | ns | |
| t _{CP} | $\overline{\text{CAS}}$ Precharge Time (for Page Mode Cycle Only) | 50 | — | 60 | — | ns | |
| t _{ASR} | Row Address Set-Up Time | 0 | — | 0 | — | ns | |
| t _{RAH} | Row Address Hold Time | 15 | — | 15 | — | ns | |
| t _{ASC} | Column Address Set-Up Time | 0 | — | 0 | — | ns | |
| t _{CAH} | Column Address Hold Time | 35 | — | 45 | — | ns | |
| t _{AR} | Column Address Hold Time Referenced to $\overline{\text{RAS}}$ | 95 | — | 120 | — | ns | |
| t _{RCS} | Read Command Set-Up Time | 0 | — | 0 | — | ns | |
| t _{RCH} | Read Command Hold Time Referenced to $\overline{\text{CAS}}$ | 0 | — | 0 | — | ns | 12 |
| t _{RRH} | Read Command Hold Time Referenced to $\overline{\text{RAS}}$ | 15 | — | 20 | — | ns | 12 |
| t _{WCH} | Write Command Hold Time | 35 | — | 45 | — | ns | |
| t _{WCR} | Write Command Hold Time Referenced to $\overline{\text{RAS}}$ | 95 | — | 120 | — | ns | |
| t _{WP} | Write Command Pulse Width | 35 | — | 45 | — | ns | |
| t _{RWL} | Write Command to $\overline{\text{RAS}}$ Lead Time | 35 | — | 45 | — | ns | |
| t _{CWL} | Write Command to $\overline{\text{CAS}}$ Lead Time | 35 | — | 45 | — | ns | |
| t _{DS} | Data-In Set-Up Time | 0 | — | 0 | — | ns | 14 |
| t _{DH} | Data-In Hold Time | 35 | — | 45 | — | ns | 14 |
| t _{DHR} | Data-In Hold Time Referenced to $\overline{\text{RAS}}$ | 95 | — | 120 | — | ns | |
| t _{REF} | Refresh Period | — | 4 | — | 4 | ms | |
| t _{WCS} | Write Command Set-Up Time | —10 | — | —10 | — | ns | 15 |
| t _{CWD} | $\overline{\text{CAS}}$ to $\overline{\text{WRITE}}$ Delay | 40 | — | 50 | — | ns | 15 |
| t _{RWD} | $\overline{\text{RAS}}$ to $\overline{\text{WRITE}}$ Delay | 100 | — | 125 | — | ns | 15 |

TMM41256P-12

TMM41256P-15

CAPACITANCE

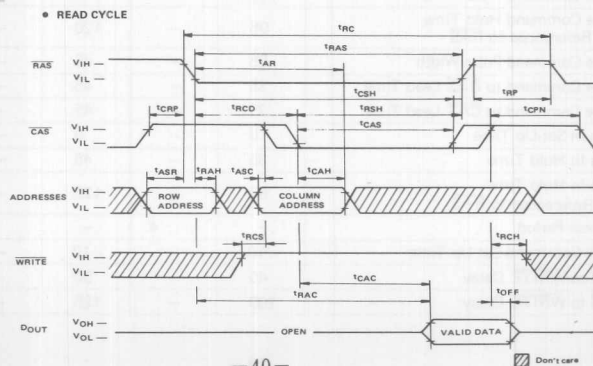
($V_{CC} = 5V \pm 10\%$, $f = 1\text{MHz}$, $T_a = 0 \sim 70^\circ\text{C}$)

| SYMBOL | PARAMETER | MIN. | MAX. | UNITS |
|----------|--|------|------|-------|
| C_{I1} | Input Capacitance ($A_0 \sim A_8, D_{IN}$) | — | 5 | pF |
| C_{I2} | Input Capacitance ($RAS, CAS, WRITE$) | — | 7 | pF |
| C_O | Output Capacitance (D_{OUT}) | — | 7 | pF |

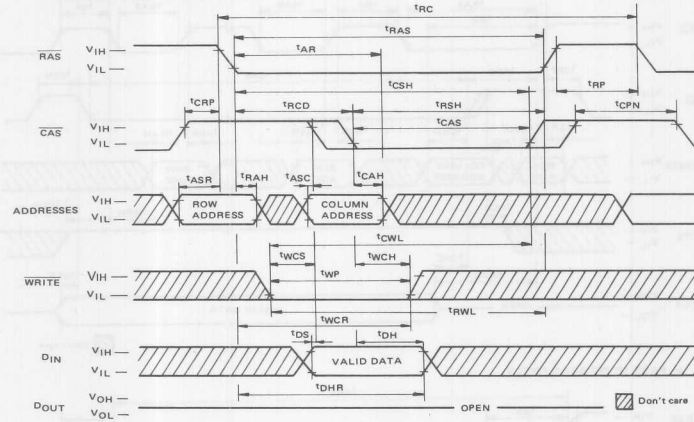
NOTES:

- Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device.
- All voltages are referenced to V_{SS} .
- I_{CC1} , I_{CC3} , I_{CC4} depend on cycle rate.
- I_{CC1} , I_{CC4} depend on output loading. Specified values are obtained with the output open.
- An initial pause of $200\mu\text{s}$ is required after power-up followed by any 8 \overline{RAS} cycles before proper device operation is achieved.
- AC measurements assume $t_T = 5\text{ns}$.
- V_{IH} (min.) and V_{IL} (max.) are reference levels for measuring timing of input signals. Also, transition times are measured between V_{IH} and V_{IL} .
- Assumes that $t_{RCD} \leq t_{RCD}(\text{max.})$. If t_{RCD} is greater than the maximum recommended value shown in this table, t_{RAC} will increase by the amount that t_{RCD} exceeds the value shown.
- Assumes that $t_{RCD} \geq t_{RCD}(\text{max.})$.
- Measured with a load equivalent to 2 TTL loads and 100pF .
- $t_{OFF}(\text{max.})$ defines the time at which the output achieves the open circuit condition and is not referenced to output voltage levels.
- Either t_{RCH} or t_{RRH} must be satisfied for a read cycle.
- Operation within the $t_{RCD}(\text{max.})$ limit insures that $t_{RAC}(\text{max.})$ can be met. $t_{RCD}(\text{max.})$ is specified as a reference point only: If t_{RCD} is greater than the specified $t_{RCD}(\text{max.})$ limit, then access time is controlled exclusively by t_{CAC} .
- These parameters are referenced to \overline{CAS} leading edge in early write cycles and to \overline{WRITE} leading edge in read-write or read-modify-write cycles.
- t_{WCS} , t_{CWD} and t_{RWD} are not restrictive operating parameters. They are included in the data sheet as electrical characteristics only. If $t_{WCS} \geq t_{WCS}(\text{min.})$, the cycle is an early write cycle and the data out pin will remain open circuit (high impedance) throughout the entire cycle; If $t_{CWD} \geq t_{CWD}(\text{min.})$ and $t_{RWD} \geq t_{RWD}(\text{min.})$, the cycle is a read-write cycle or read-modify-write cycle and the data out will contain data read from the selected cell: If neither of the above sets of conditions is satisfied, the condition of the data out (at access time) is indeterminate.

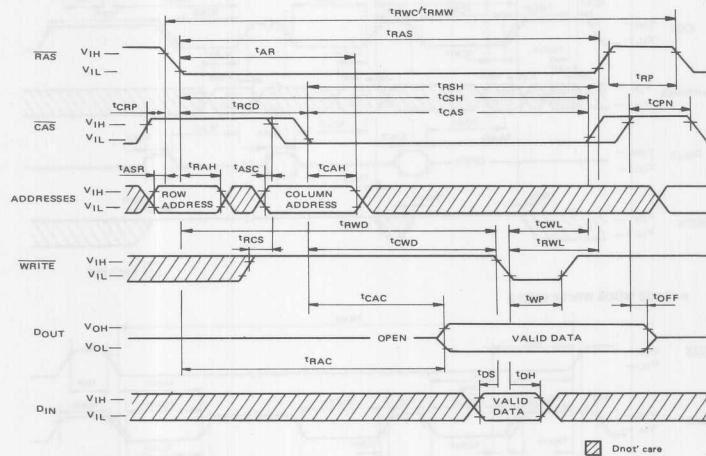
TIMING WAVEFORMS



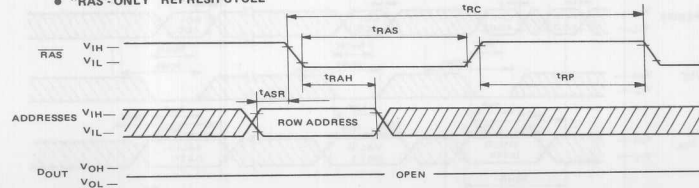
• WRITE CYCLE (EARLY WRITE)



• READ-WRITE/READ-MODIFY-WRITE CYCLE



• "RAS-ONLY" REFRESH CYCLE

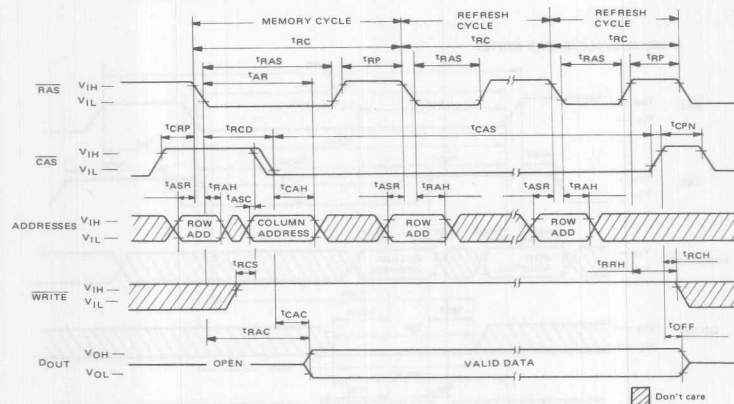


Note: $\overline{CAS} = V_{IH}$, $\overline{WRITE} = \text{Don't care}$, $A_g = \text{Don't care}$

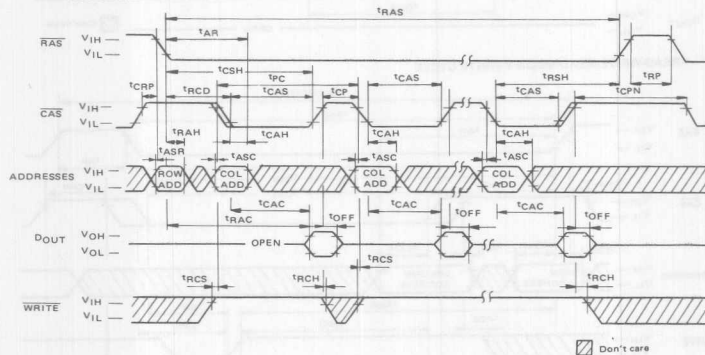
Don't care

TMM41256P-12
TMM41256P-15

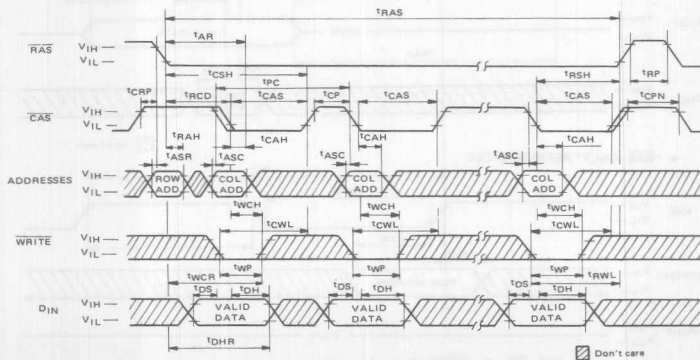
- HIDDEN REFRESH CYCLE



- PAGE MODE READ CYCLE



- PAGE MODE WRITE CYCLE



APPLICATION INFORMATION

ADDRESSING

The 18 address bits required to decode 1 of the 262,144 cell locations within the TMM41256P are multiplexed onto the 9 address inputs and latched into the on-chip address latches by externally applying two negative going TTL-level clocks.

The first clock, the Row Address Strobe ($\overline{\text{RAS}}$), latches the 9 row address bits into the chip. The second clock, the Column Address Strobe ($\overline{\text{CAS}}$), subsequently latches the 9 column address bits into the chip. Each of these signals, $\overline{\text{RAS}}$ and $\overline{\text{CAS}}$, triggers a sequence of events which are controlled by different delayed internal clocks.

The two clock chains are linked together logically in such a way that the address multiplexing operation is done outside of the critical path timing sequence for read data access. The later events in the $\overline{\text{CAS}}$ clock sequence are inhibited until the occurrence of a delayed signal derived from the $\overline{\text{RAS}}$ clock chain. This "gated $\overline{\text{CAS}}$ " feature allows the $\overline{\text{CAS}}$ clock to be externally activated as soon as the Row Address Hold Time specification (t_{RAH}) has been satisfied and the address inputs have been changed from Row address to Column address information.

DATA INPUT/OUTPUT

Data to be written into a selected cell is latched into an on-chip register by a combination of $\overline{\text{WRITE}}$ and $\overline{\text{CAS}}$ while $\overline{\text{RAS}}$ is active. The later of the signals ($\overline{\text{WRITE}}$ or $\overline{\text{CAS}}$) to make its negative transition is the strobe for the Data In (D_{IN}) register. This permits several options in the write cycle timing. In a write cycle, if the $\overline{\text{WRITE}}$ input is brought low (active) prior to $\overline{\text{CAS}}$, the D_{IN} is strobed by $\overline{\text{CAS}}$ and the set-up and hold times are referenced to $\overline{\text{CAS}}$. If the input data is not available at $\overline{\text{CAS}}$ time or if it is desired that the cycle be a read-write cycle, the $\overline{\text{WRITE}}$ signal will be delayed until after $\overline{\text{CAS}}$ has made its negative transition. In this "delayed write cycle" the data input set-up and hold times are referenced to the negative edge of $\overline{\text{WRITE}}$ rather than $\overline{\text{CAS}}$. (To illustrate this feature, D_{IN} is referenced to $\overline{\text{WRITE}}$ in the timing diagrams depicting the read-write and page mode write cycles while the "early write" cycle diagram shows D_{IN} referenced to $\overline{\text{CAS}}$).

Data is retrieved from the memory in a read

cycle by maintaining $\overline{\text{WRITE}}$ in the inactive or high state throughout the portion of the memory cycle in which $\overline{\text{CAS}}$ is active (low). Data read from the selected cell will be available at the output within the specified access time.

DATA OUTPUT CONTROL

The normal condition of the Data Output (D_{OUT}) of the TMM41256P is the high impedance (open circuit) state. This is to say, anytime $\overline{\text{CAS}}$ is at a high level, the D_{OUT} pin will be floating. The only time the output will turn on and contain either a logic 0 or logic 1 is at access time during a read cycle. D_{OUT} will remain valid from access time until $\overline{\text{CAS}}$ is taken back to the inactive (high level) condition.

PAGE MODE

The "Page-Mode" feature of the TMM41256P allows for successive memory operations at multiple column locations of the same row address with increased speed without an increase in power. This is done by strobing the row address into the chip and maintaining the $\overline{\text{RAS}}$ signal at a logic 0 throughout all successive memory cycles in which the row address is common. This "Page Mode" of operation will not dissipate the power associated with the negative going edge of $\overline{\text{RAS}}$. Also, the time required for strobing in a new row address is eliminated, thereby decreasing the access and cycle times.

REFRESH

Refresh of the dynamic cell matrix is accomplished by performing a memory cycle at each of the 256 row address ($\text{A}_0 \sim \text{A}_7$) within each 4 millisecond time interval. Although any normal memory cycle will perform the refresh operation, this function is most easily accomplished with "RAS - only" cycles; $\overline{\text{RAS}}$ only refresh results in a substantial reduction in operating power. This reduction in power is reflected in the I_{CC3} specification.

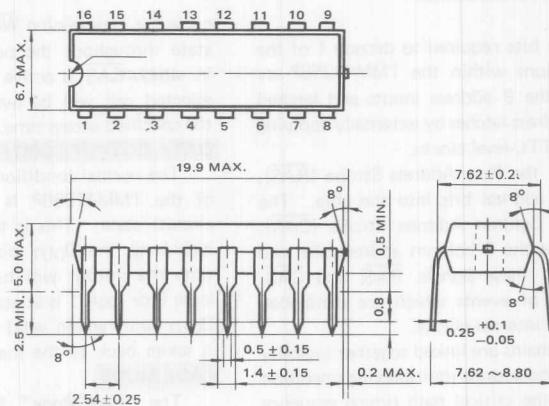
HIDDEN REFRESH

An optional feature of the TMM41256P is that refresh cycles may be performed while maintaining valid data at the output pin. This is referred to as Hidden Refresh. Hidden Refresh is performed by holding $\overline{\text{CAS}}$ at V_{IL} and taking $\overline{\text{RAS}}$ high and after a specified precharge period (t_{RP}), executing a "RAS - only" refresh cycle, but with $\overline{\text{CAS}}$ held low.

TMM41256P-12

TMM41256P-15

OUTLINE DRAWINGS



Note : Each lead pitch is 2.54 mm. All leads are located within 0.25 mm of their true longitudinal position with respect to No. 1 and No. 16 leads. All dimensions are in millimeters.

Note: Toshiba does not assume any responsibility for use of any circuitry described; no circuit patent licenses are implied, and Toshiba reserves the right, at any time without notice, to change said circuitry.

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TOSHIBA MOS MEMORY PRODUCTS

262,144 WORD × 1 BIT DYNAMIC RAM

SILICON MONOLITHIC
N-CHANNEL SILICON GATE MOS

TMM41257P-12 TMM41257P-15

DESCRIPTION

The TMM41257P is the N-channel dynamic RAM organized 262,144 words by 1 bit. Multiplexed address inputs permit the TMM41257P to be packaged in a standard 16 pin plastic DIP. This package size provides high system bit densities and is compatible with widely available automated testing and insertion equipment.

The double layered MOS technology with polycide and poly Si permits the TMM41257P high speed operation. Also, the advanced circuit tech-

niques have realized low power dissipation.

System oriented features include single power supply of $5V \pm 10\%$ tolerance, direct interfacing capability with high performance logic families such as schottky TTL.

In addition to the $\overline{\text{RAS}}$ only refresh mode, a $\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ automatic refresh is available. Another special feature of TMM41257P is nibble mode, allowing the user to serially access 4 bits of data at a high data rate.

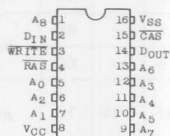
FEATURES

- 262,144 words by 1 bit organization
- Fast access time and cycle time

| | TMM41257P-12 | TMM41257P-15 |
|-----------------|--------------|--------------|
| RAS Access Time | 120ns | 150ns |
| CAS Access Time | 60ns | 75ns |
| Cycle Time | 220ns | 260ns |
| Nibble Mode | | |
| Access Time | 30ns | 40ns |
| Nibble Mode | | |
| Cycle Time | 55ns | 70ns |

- Single power supply of $5V \pm 10\%$ with a built-in V_{BB} generator

PIN CONNECTION (TOP VIEW)

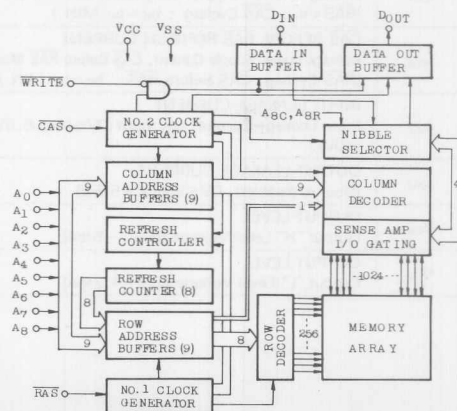


PIN NAMES

| | |
|--------------------------------|-----------------------|
| A ₀ ~A ₈ | Address Inputs |
| CAS | Column Address Strobe |
| D _{1N} | Data In |
| D _{OUT} | Data Out |
| RAS | Row Address Strobe |
| WRITE | Read/Write Input |
| V _{CC} | Power (+5V) |
| V _{SS} | Ground |

- Low Power :
385mW Operating (MAX.) (TMM41257P-12)
330mW Operating (MAX.) (TMM41257P-15)
28mW Standby (MAX.).
- Industry standard 16 pin plastic DIP
- Output unlatched at cycle end allows two-dimensional chip selection
- Common I/O capability using "EARLY WRITE" operation
- Read-Modify-Write, $\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ refresh, $\overline{\text{RAS}}$ -only refresh, Hidden refresh, and Nibble Mode capability
- All inputs and output TTL compatible
- 256 refresh cycles/4ms

BLOCK DIAGRAM



TMM41257P-12

TMM41257P-15

ABSOLUTE MAXIMUM RATINGS

| ITEM | SYMBOL | RATING | UNITS | NOTES |
|------------------------------|-------------------|---------|--------|-------|
| Input and Output Voltage | V_{IN}, V_{OUT} | -1~7 | V | 1 |
| Power Supply Voltage | V_{CC} | -1~7 | V | 1 |
| Operating Temperature | T_{OPR} | 0~70 | °C | 1 |
| Storage Temperature | T_{STG} | -55~150 | °C | 1 |
| Soldering Temperature·Time | T_{SOLDER} | 260·10 | °C·sec | 1 |
| Power Dissipation | P_D | 600 | mW | 1 |
| Short Circuit Output Current | I_{OUT} | 50 | mA | 1 |

RECOMMENDED DC OPERATING CONDITIONS (Ta=0~70°C)

| SYMBOL | PARAMETER | MIN. | TYP. | MAX. | UNITS | NOTES |
|----------|--------------------|------|------|------|-------|-------|
| V_{CC} | Supply Voltage | 4.5 | 5.0 | 5.5 | V | 2 |
| V_{IH} | Input High Voltage | 2.4 | — | 6.5 | V | 2 |
| V_{IL} | Input Low Voltage | -1.0 | — | 0.8 | V | 2 |

DC ELECTRICAL CHARACTERISTICS (V_{CC}=5V±10%, Ta=0~70°C)

| SYMBOL | PARAMETER | MIN. | MAX. | UNITS | NOTES |
|------------------|--|--------------|------|-------|-----------|
| I _{CC1} | OPERATING CURRENT Average Power Supply Operating Current (RAS, CAS Cycling : t _{RC} =t _{RC} MIN.) | TMM41257P-12 | — | 70 | mA 3,4 |
| | | TMM41257P-15 | — | 60 | |
| I _{CC2} | STANDBY CURRENT Power Supply Standby Current (RAS=CAS=V _{IL}) | — | 5 | mA | |
| I _{CC3} | RAS ONLY REFRESH CURRENT Average Power Supply Current, RAS Only Mode (RAS Cycling, CAS=V _{IL} : t _{RC} =t _{RC} MIN.) | TMM41257P-12 | — | 60 | mA 3 |
| | | TMM41257P-15 | — | 50 | |
| I _{CC4} | NIBBLE MODE CURRENT Average Power Supply Current, Nibble Mode (RAS=V _{IL} , CAS Cycling : t _{NC} =t _{NC} MIN.) | TMM41257P-12 | — | 40 | mA 3,4 |
| | | TMM41257P-15 | — | 30 | |
| I _{CC5} | CAS BEFORE RAS REFRESH CURRENT Average Power Supply Current, CAS Before RAS Mode (RAS Cycling, CAS Before RAS : t _{RC} =t _{RC} MIN.) | TMM41257P-12 | — | 60 | mA 3 |
| | | TMM41257P-15 | — | 50 | |
| I _{IL1} | INPUT LEAKAGE CURRENT Input Leakage Current, any input (0V≤V _{IN} ≤6.5V, All Other Pins Not Under Test = 0V) | -10 | 10 | μA | |
| I _{OL1} | OUTPUT LEAKAGE CURRENT (D _{OUT} is disabled, 0V≤V _{OUT} ≤+5.5V) | -10 | 10 | μA | |
| V _{OH} | OUTPUT LEVEL Output "H" Level Voltage (I _{OUT} =-5mA) | 2.4 | — | V | |
| V _{OL} | OUTPUT LEVEL Output "L" Level Voltage (I _{OUT} =4.2mA) | — | 0.4 | V | |

ELECTRIAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

(V_{CC}=5V±10%, Ta=0~70°C) (Notes 5, 6, 7)

| SYMBOL | PARAMETER | TMM41257P-12 | | TMM41257P-15 | | UNITS | NOTES |
|--------------------|--|--------------|--------|--------------|--------|-------|-------|
| | | MIN. | MAX. | MIN. | MAX. | | |
| t _{RC} | Random Read or Write Cycle Time | 220 | — | 260 | — | ns | |
| t _{RWC} | Read-Write Cycle Time | 240 | — | 285 | — | ns | |
| t _{RMW} | Read-Modify-Write Cycle Time | 260 | — | 310 | — | ns | |
| t _{RAC} | Access Time from RAS | — | 120 | — | 150 | ns | 8,10 |
| t _{CAC} | Access Time from CAS | — | 60 | — | 75 | ns | 9,10 |
| t _{OFF} | Output Buffer Turn-Off Delay | 5 | 30 | 5 | 35 | ns | 11 |
| t _T | Transition Time (Rise and Fall) | 3 | 50 | 3 | 50 | ns | 7 |
| t _{RP} | RAS Precharge Time | 90 | — | 100 | — | ns | |
| t _{RAS} | RAS Pulse Width | 120 | 10,000 | 150 | 10,000 | ns | |
| t _{RSH} | RAS Hold Time | 60 | — | 75 | — | ns | |
| t _{CSH} | CAS Hold Time | 120 | — | 150 | — | ns | |
| t _{CAS} | CAS Pulse Width | 60 | 10,000 | 75 | 10,000 | ns | |
| t _{RCD} | RAS to CAS Delay Time | 25 | 60 | 25 | 75 | ns | 13 |
| t _{CRP} | CAS to RAS Precharge Time | 10 | — | 10 | — | ns | |
| t _{CPN} | CAS Precharge Time | 20 | — | 25 | — | ns | |
| t _{ASR} | Row Address Set-Up Time | 0 | — | 0 | — | ns | |
| t _{RAH} | Row Address Hold Time | 15 | — | 15 | — | ns | |
| t _{ASC} | Column Address Set-Up Time | 0 | — | 0 | — | ns | |
| t _{CAH} | Column Address Hold Time | 25 | — | 30 | — | ns | |
| t _{AR} | Column Address Hold Time Reference to RAS | 85 | — | 105 | — | ns | |
| t _{RCS} | Read Command Set-Up Time | 0 | — | 0 | — | ns | |
| t _{RCH} | Read Command Hold Time Reference to CAS | 0 | — | 0 | — | ns | 12 |
| t _{RRH} | Read Command Hold Time Reference to RAS | 15 | — | 20 | — | ns | 12 |
| t _{WCH} | Write Command Hold Time | 25 | — | 30 | — | ns | |
| t _{WCR} | Write Command Hold Time Reference to RAS | 85 | — | 105 | — | ns | |
| t _{WP} | Write Command Pulse Width | 25 | — | 30 | — | ns | |
| t _{RWL} | Write Command to RAS Lead Time | 35 | — | 45 | — | ns | |
| t _{CWL} | Write Command to CAS Lead Time | 35 | — | 45 | — | ns | |
| t _{DS} | Data-In Set-Up Time | 0 | — | 0 | — | ns | 14 |
| t _{DH} | Data-In Hold Time | 25 | — | 30 | — | ns | 14 |
| t _{DHR} | Data-In Hold Time Reference to RAS | 85 | — | 105 | — | ns | |
| t _{REF} | Refresh Period | — | 4 | — | 4 | ms | |
| t _{WCS} | Write Command Set-Up Time | 0 | — | 0 | — | ns | 15 |
| t _{CWD} | CAS to WRITE Delay | 40 | — | 50 | — | ns | 15 |
| t _{RWD} | RAS to WRITE Delay | 100 | — | 125 | — | ns | 15 |
| t _{CSR} | CAS Set-Up Time (CAS before RAS) | 10 | — | 10 | — | ns | |
| t _{CHR} | CAS Hold Time (CAS before RAS) | 30 | — | 30 | — | ns | |
| t _{RPC} | RAS Precharge to CAS Active Time | 0 | — | 0 | — | ns | |
| t _{CPT} | CAS Precharge Time (CAS before RAS Counter Test) | 50 | — | 60 | — | ns | |
| t _{NC} | Nibble Mode Cycle Time | 55 | — | 70 | — | ns | |
| t _{NCAC} | Nibble Mode Access Time | — | 30 | — | 40 | ns | 10 |
| t _{NCAS} | Nibble Mode Pulse Width | 30 | — | 40 | — | ns | |
| t _{NCP} | Nibble Mode CAS Precharge Time | 15 | — | 20 | — | ns | |
| t _{NRRSH} | Nibble Mode RAS Hold Time (Read) | 25 | — | 30 | — | ns | |
| t _{NWRSH} | Nibble Mode RAS Hold Time (Write) | 45 | — | 50 | — | ns | |
| t _{NCWD} | Nibble Mode CAS to WRITE Delay Time | 30 | — | 40 | — | ns | |
| t _{NCWL} | Nibble Mode WRITE Command to CAS Read Time | 25 | — | 30 | — | ns | |

TMM41257P-12

TMM41257P-15

CAPACITANCE (V_{CC}=5V±10%, f=1MHz, T_a=0~70°C)

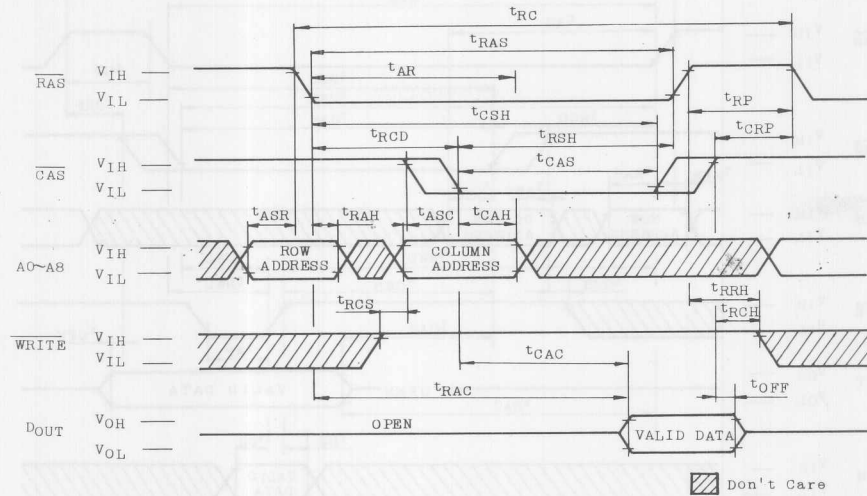
| SYMBOL | PARAMETER | MIN. | MAX. | UNITS |
|-----------------|---|------|------|-------|
| C _{II} | Input Capacitance (A ₀ ~A ₈ , D _{IN}) | — | 5 | pF |
| C _{I2} | Input Capacitance (RAS, CAS, WRITE) | — | 7 | pF |
| C _O | Output Capacitance (D _{OUT}) | — | 7 | pF |

NOTES :

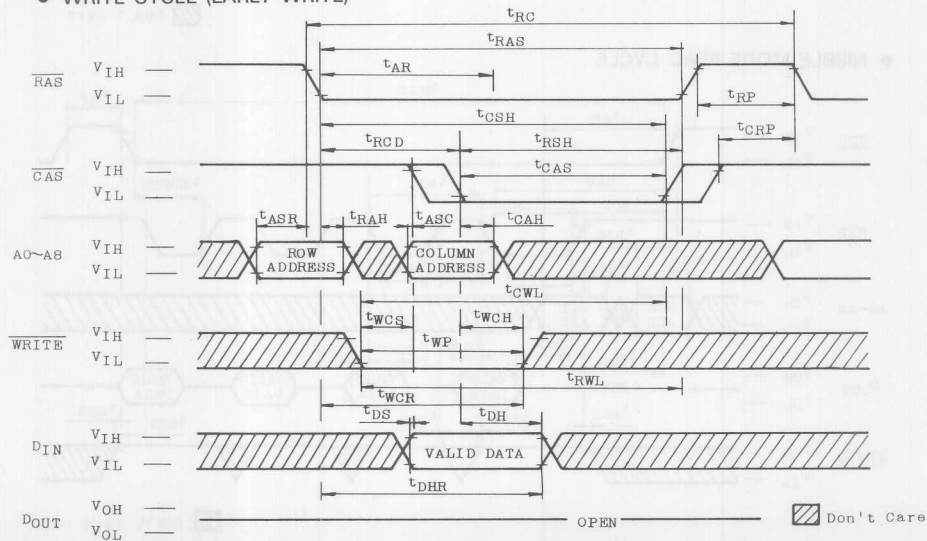
1. Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device.
2. All voltages are referenced to V_{SS}.
3. I_{CC1}, I_{CC3}, I_{CC4}, I_{CC5}, depend on cycle rate.
4. I_{CC1}, I_{CC4} depend on output loading. Specified values are obtained with the output open.
5. An initial pause of 200μs is required after power-up followed by any 8 RAS cycles before proper device operation is achieved. In case of using internal refresh counter, a minimum of 8 CAS Before RAS initialization cycles instead of 8 RAS cycles are required.
6. AC measurements assume t_r=5ns.
7. V_{IH}(min.) and V_{IL}(max.) are reference levels for measuring timing of input signals. Also, transition times are measured between V_{IH} and V_{IL}.
8. Assumes that t_{RCD} ≤ t_{RCD}(max.). If t_{RCD} is greater than the maximum recommended value shown in this table, t_{RAC} will increase by the amount that t_{RCD} exceeds the value shown.
9. Assumes that t_{RCD} ≤ t_{RCD}(max.).
10. Measured with a load equivalent to 2 TTL loads and 100pF.
11. t_{OFF}(max.) defines the time at which the output achieves the open circuit condition and is not referenced to output voltage levels.
12. Either t_{RCH} or t_{RRH} must be satisfied for a read cycle.
13. Operation within the t_{RCD}(max.) limit insures that t_{RAC}(max.) can be met. t_{RCD}(max.) is specified as a reference point only : If t_{RCD} is greater than the specified t_{RCD}(max.) limit, then access time is controlled exclusively by t_{CAC}.
14. These parameters are referenced to CAS leading edge in early write cycles and to WRITE leading edge in read-write or read-modify-write cycles.
15. t_{WCS}, t_{CWD} and t_{RWD} are not restrictive operating parameters. They are included in the data sheet as electrical characteristics only. If t_{WCS} ≥ t_{WCS}(min.), the cycle is an early write cycle and the data out pin will remain open circuit (high impedance) throughout the entire cycle ; If t_{CWD} ≥ t_{CWD}(min.) and t_{RWD} ≥ t_{RWD}(min.), the cycle is a read-write cycle or read- modify- write cycle and the data out will contain data read from the selected cell : If neither of the above sets of conditions is satisfied, the condition of the data out (at access time) is indeterminate.

TIMING WAVEFORMS

• READ CYCLE



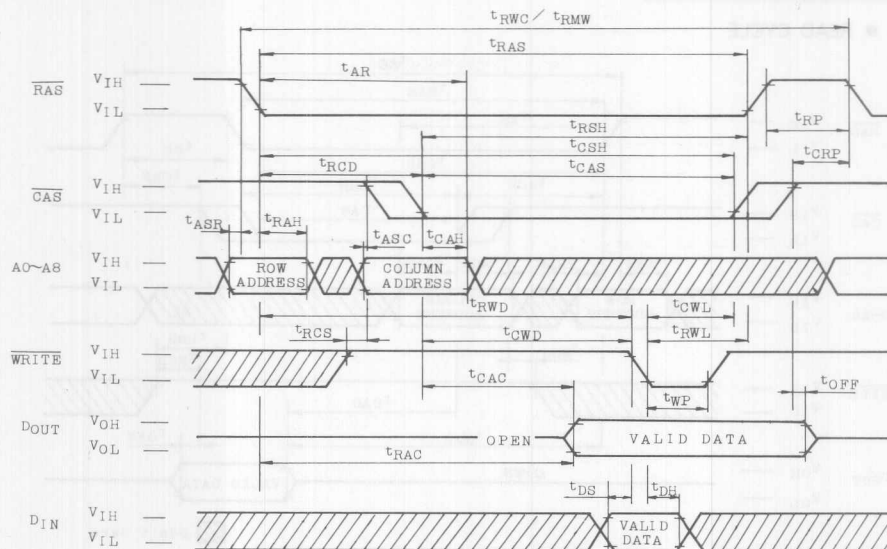
• WRITE CYCLE (EARLY WRITE)



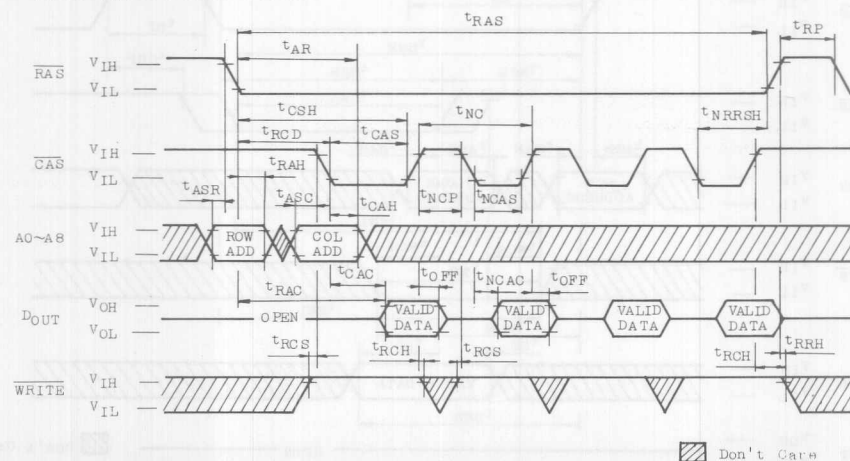
TMM41257P-12

TMM41257P-15

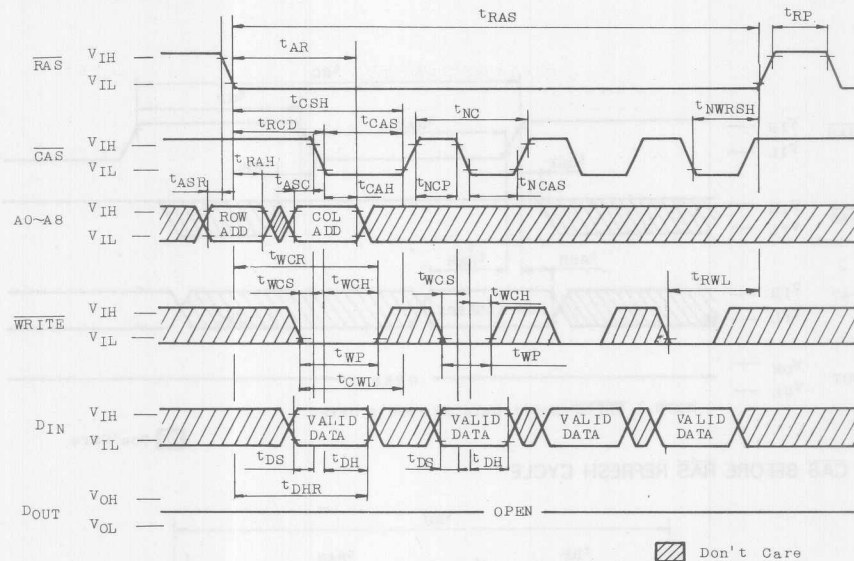
● READ-WRITE/READ-MODIFY-WRITE CYCLE



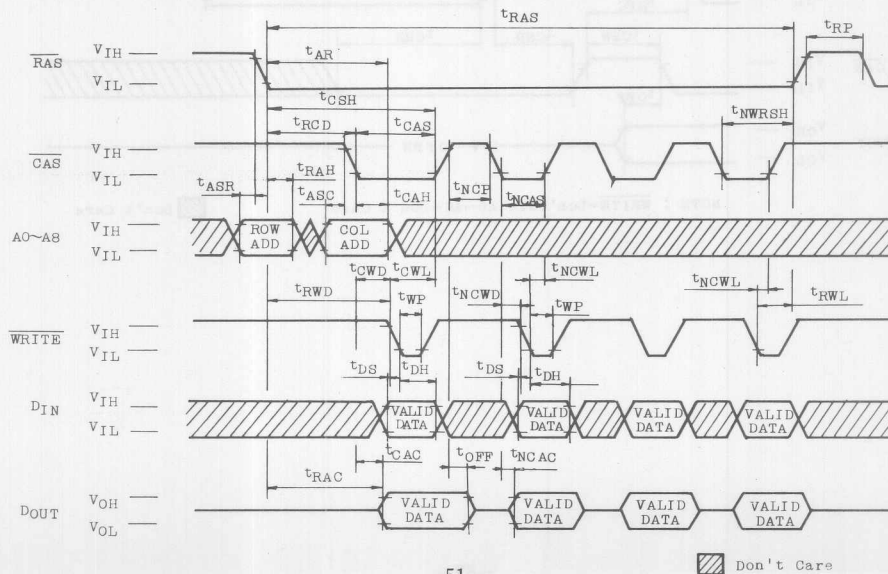
● NIBBLE MODE READ CYCLE



● NIBBLE MODE WRITE CYCLE

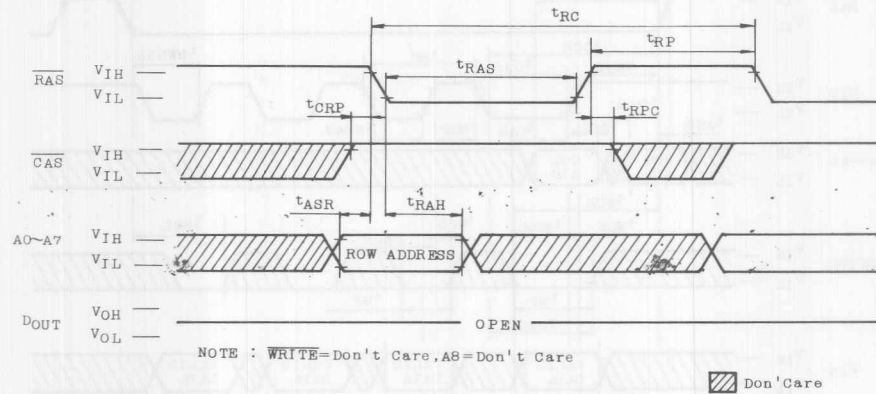


● NIBBLE MODE READ-WRITE/READ-MODIFY-WRITE CYCLE

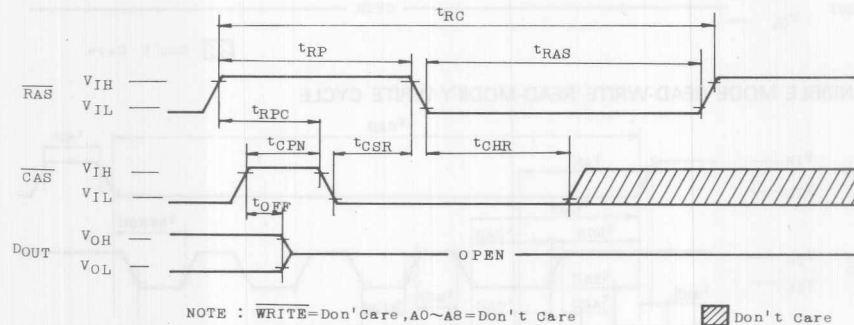


TMM41257P-12 TMM41257P-15

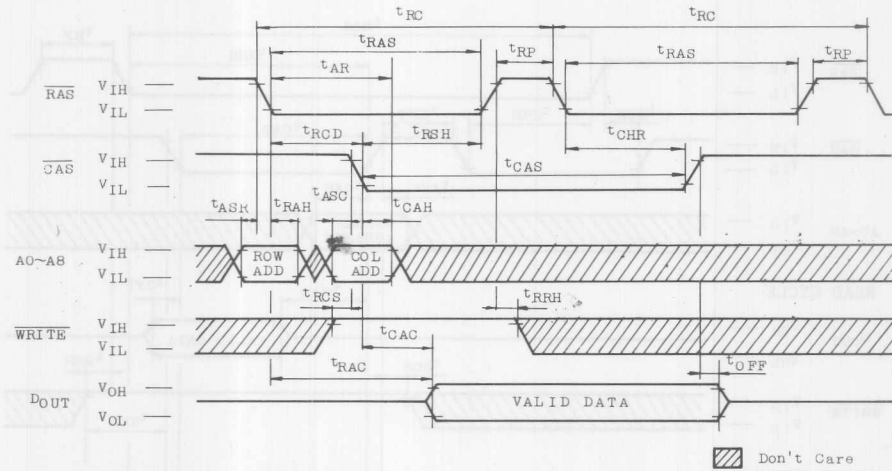
• $\overline{\text{RAS}}$ ONLY REFRESH CYCLE



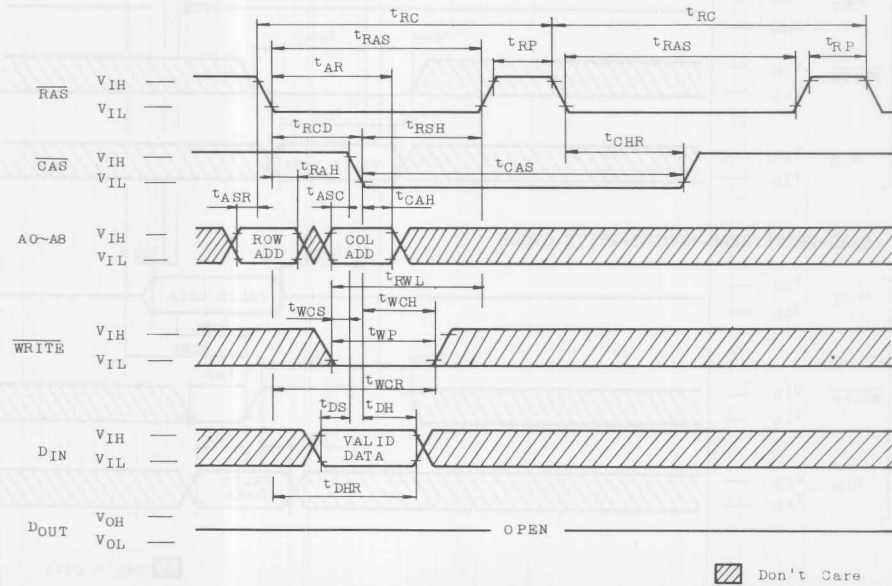
• $\overline{\text{CAS}}$ BEFORE $\overline{\text{RAS}}$ REFRESH CYCLE



● HIDDEN REFRESH CYCLE (READ)



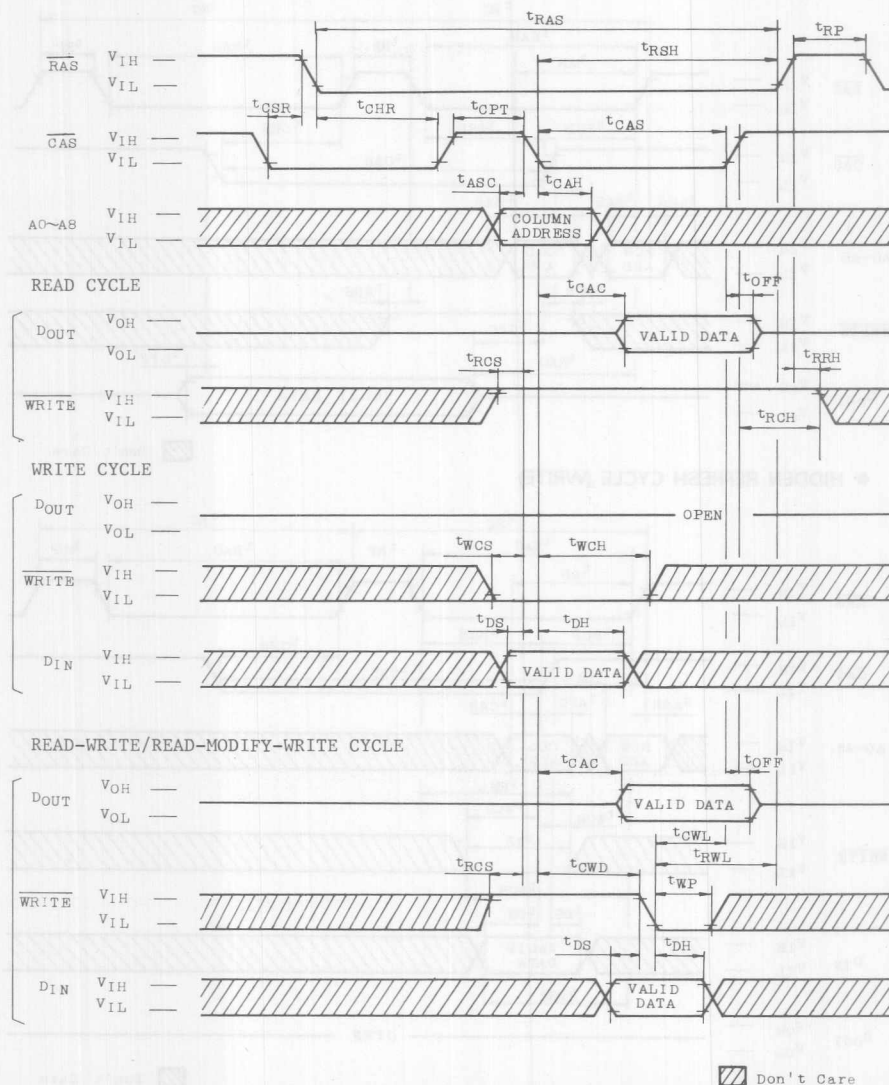
● HIDDEN REFRESH CYCLE (WRITE)



TMM41257P-12

TMM41257P-15

• CAS BEFORE RAS REFRESH COUNTER TEST CYCLE



APPLICATION INFORMATION

ADDRESSING

The 18 address bits required to decode 1 of the 262,144 cell locations within the TMM41257P are multiplexed onto the 9 address inputs and latched into the on-chip address latches by externally applying two negative going TTL-level clocks.

The first clock, the Row Address Strobe (RAS), latches the 9 row address bits into the chip. The second clock, the Column Address Strobe (CAS), subsequently latches the 9 column address bits into the chip. Each of these signals, RAS, and CAS, triggers a sequence of events which are controlled by different delayed internal clocks.

The two clock chains are linked together logically in such a way that the address multiplexing operation is done outside of the critical path timing sequence for read data access. The later events in the CAS clock sequence are inhibited until the occurrence of a delayed signal derived from the RAS clock chain. This "gated CAS" feature allows the CAS clock to be externally activated as soon as the Row address Hold Time specification (trAH) has been satisfied and the address inputs have been changed from Row address to Column address information.

DATA INPUT/OUTPUT

Data to be written into a selected cell is latched into an on-chip register by a combination of WRITE and CAS while RAS is active. The later of the signals (WRITE or CAS) to make its negative transition is the strobe for the Data in (DIN) register. This permits several options in the write cycle timing. In a write cycle, if the WRITE input is brought low(active) prior to CAS, the DIN is strobed by CAS and the set-up and hold times are referenced to CAS. If the input data is not available at CAS time or if it is desired that the cycle be a read-write cycle, the WRITE signal will be delayed until after CAS has made its negative transition. In this "delayed write cycle" the data input set-up and hold times are referenced to the negative edge of WRITE rather than CAS. (To illustrate this feature, DIN is referenced to WRITE in the timing diagrams depicting the read-write and nibble mode write cycles while the "early write" cycle diagram shows DIN referenced to CAS).

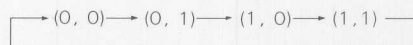
Data is retrieved from the memory in a read cycle by maintaining WRITE in the inactive or high state throughout the portion of memory cycle in which CAS is active (low). Data read from the selected cell will be available at the output within the specified access time.

DATA OUTPUT CONTROL

The normal condition of the Data Output (Dout) of the TMM41257P is the high impedance (open circuit) state. This is to say, anytime CAS is at a high level, the Dout pin will be floating. The only time the output will turn on and contain either a logic 0 or logic 1 is at access time during a read cycle. Dout will remain valid from access time until CAS is taken back to the inactive (high level) condition.

NIBBLE MODE

Nibble mode operation allows faster successive data operation on 4 bits. The first of 4 bits is accessed in the usual manner with read data coming out at tCAC time. By keeping RAS low, CAS can be cycled up and then down, to read or write the next three pages at high data rate (faster than tCAC). Row and column addresses need only be supplied for the first access of cycles. From then on, the falling edge of CAS will activate the next bit. After four bits have been accessed, the next bit will be the same as the first bit accessed (wrap-around method).



Pin one (A₈) determines the starting point the circular 4 bits nibble. Row A₈ and column A₈ provide the two binary bits needed to select one of four bits. From then on, successive bits come out in a binary fashion; 00 → 01 → 10 → 11 with A₈ row being the least significant address.

A nibble cycle can be a read, write, or late write cycle. Any combinations of reads and writes or late writes will be allowed. In addition, the circular wraparound will continue for as long as RAS is kept low.

RAS ONLY REFRESH

Refresh of the dynamic cell matrix is accomplished by performing a memory cycle at each of the 256 row address (A₀~A₇) within each 4 millisecond time interval. Although any normal memory cycle will perform the refresh operation, this function is most easily accomplished with "RAS-only" cycles, RAS only refresh results in a substantial reduction in operating power. This reduction in power is reflected in the Icc3 specification.

TMM41257P-12

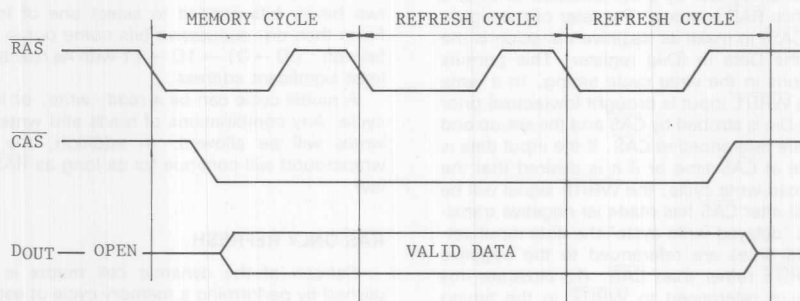
TMM41257P-15

CAS BEFORE RAS REFRESH

CAS before RAS refreshing available on the TMM41257P offers an alternate refresh method. If CAS is held on low for the specified period (tcsr) before RAS goes to low, on chip refresh control clock generators and refresh address counter are enabled, and an internal refresh operation takes place. After the refresh operation is performed, the refresh address counter is automatically incremented in preparation for the next CAS before RAS refresh operation.

HIDDEN REFRESH

An optional feature of the TMM41257P is that refresh cycles may be performed while maintaining valid data at the output pin. This is referred to as Hidden Refresh. Hidden Refresh is performed by holding CAS at V_{IL} and taking RAS high and after a specified precharge period (tRP), executing a CAS before RAS refresh cycle, (see Figure below)



This feature allows a refresh cycle to be "hidden" among data cycles without affecting the data availability.

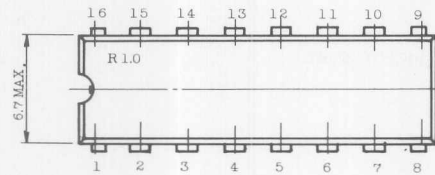
CAS BEFORE RAS REFRESH COUNTER TEST

The internal refresh operation of TMM41257P can be tested by CAS BEFORE RAS REFRESH COUNTER TEST. This cycle performs READ/WRITE operation taking the internal counter address as row address and the input address as column address.

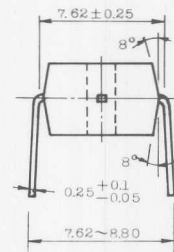
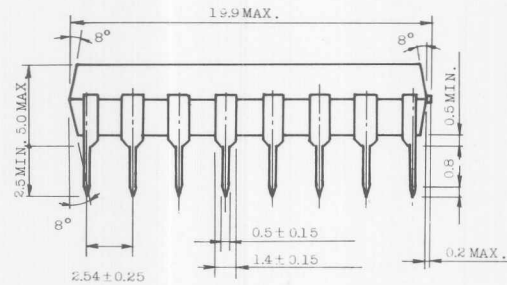
The test is performed after a minimum of 8 CAS before RAS cycles as initialization cycles. The test procedure is as follows.

- ① Write "0" into all the memory cells at normal write mode.
- ② Select one certain column address and read "0" out and write "1" in each cell by performing CAS BEFORE RAS REFRESH COUNTER TEST (READ-WRITE CYCLE). Repeat this operation 256 times.
- ③ Check "1" out of 256 bits at normal read mode, which was written at ②.
- ④ Using the same column as ②, read "1" out and write "0" in each cell performing CAS BEFORE RAS REFRESH COUNTER TEST. Repeat this operation 256 times.
- ⑤ Check "0" out of 256 bits at normal read mode, which was written at ④.
- ⑥ Perform the above ① to ⑤ the complement data.

OUTLINE DRAWINGS



Unit in mm



NOTES : Each lead pitch is 2.54mm. All leads are located within 0.25mm of their true longitudinal position with respect to No. 1 and No. 16 leads. All dimensions are in millimeters.

TMM41257P-12 TMM41257P-15



Note : Toshiba does not assume any responsibility for use of any circuitry described ; no circuit patent licenses are implied, and Toshiba reserves the right, at any time without notice, to change said circuitry.
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TOSHIBA MOS MEMORY PRODUCTS

65,536 WORD × 4 BIT DYNAMIC RAM

SILICON MONOLITHIC
N-CHANNEL SILICON GATE MOS

TMM41464P-12 TMM41464P-15

DESCRIPTION

The TMM41464P is the new generation dynamic RAM organized 65,536 word by 4 bit, it is successor to the industry standard TMM4164AP.

The TMM41464P utilizes TOSHIBA's N-channel/Silicon gate process technology as well as advanced circuit techniques to provide wide operating margins, both internally and to the system user.

Multiplexed address inputs permit the TMM

41464P to be packaged in a standard 18 pin plastic DIP. This package size provides high system bit densities and is compatible with widely available automated testing and insertion equipment.

System oriented features include single power supply of $5V \pm 10\%$ tolerance, direct interfacing capability with high performance logic families such as schottky TTL.

FEATURES

- 65,536 words by 4 bit organization
- Fast access Time and cycle time

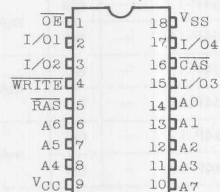
| DEVICE | t _{TRAC} | t _{CAC} | t _{TRC} |
|--------------|-------------------|------------------|------------------|
| TMM41464P-12 | 120ns | 60ns | 220ns |
| TMM41464P-15 | 150ns | 75ns | 260ns |

- Single power supply of $5V \pm 10\%$ with a built-in V_{BB} generator
- Low power:
385mW Operating (MAX.) (TMM41464-12)

330mW Operating (MAX.) (TMM41464-15)
28mW Standby (MAX.)

- Industry standard 18 pin plastic DIP
- Output unlatched at cycle end allows two-dimensional chip selection
- Read-Modify-Write, \overline{RAS} only refresh, Hidden refresh, CAS before RAS refresh, and Page Mode capability.
- All inputs and outputs TTL compatible
- 256 refresh cycles/4ms

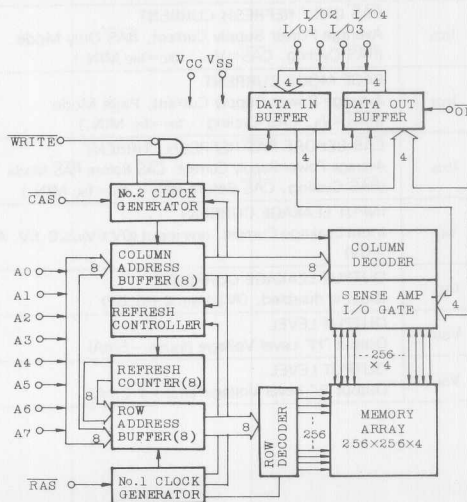
PIN CONNECTION



PIN NAMES

| | |
|-------------------------------------|-----------------------|
| A ₀ ~ A ₇ | Address Inputs |
| CAS | Column Address Strobe |
| I/O ₁ ~ I/O ₄ | Data Input/Output |
| RAS | Row Address Strobe |
| WRITE | Read/Write Input |
| OE | Output Enable |
| V _{CC} | Power (+5V) |
| V _{SS} | Ground |

BLOCK DIAGRAM



TMM41464P-12

TMM41464P-15

ABSOLUTE MAXIMUM RATINGS

| ITEM | SYMBOL | RATING | UNITS | NOTES |
|------------------------------|-------------------|---------|--------|-------|
| Input and Output Voltage | V_{IN}, V_{OUT} | -1~7 | V | 1 |
| Power Supply Voltage | V_{CC} | -1~7 | V | 1 |
| Operating Temperature | T_{OPR} | 0~70 | °C | 1 |
| Storage Temperature | T_{STG} | -55~150 | °C | 1 |
| Soldering Temperature·Time | T_{SOLDER} | 260·10 | °C·sec | 1 |
| Power Dissipation | P_D | 600 | mW | 1 |
| Short Circuit Output Current | I_{OUT} | 50 | mA | 1 |

RECOMMENDED DC OPERATING CONDITIONS (Ta=0~70°C)

| SYMBOL | PARAMETER | MIN. | TYP. | MAX. | UNITS | NOTES |
|----------|--------------------|------|------|------|-------|-------|
| V_{CC} | Supply Voltage | 4.5 | 5.0 | 5.5 | V | 2 |
| V_{IH} | Input High Voltage | 2.4 | — | 6.5 | V | 2 |
| V_{IL} | Input Low Voltage | -1.0 | — | 0.8 | V | 2 |

DC ELECTRICAL CHARACTERISTICS (V_{CC}=5V±10%, Ta=0~70°C)

| SYMBOL | PARAMETER | MIN. | MAX. | UNITS | NOTES |
|-----------|---|--------------|------|---------|-----------|
| I_{CC1} | OPERATING CURRENT Average Power Supply Operating Current (RAS, CAS Cycling : $t_{RC}=t_{RC}$ MIN.) | TMM41464P-12 | — | 70 | mA 3,4 |
| | | TMM41464P-15 | — | 60 | |
| I_{CC2} | STANDBY CURRENT Power Supply Standby Current (RAS=CAS= V_{IH}) | — | 5 | mA | |
| I_{CC3} | RAS ONLY REFRESH CURRENT Average Power Supply Current, RAS Only Mode (RAS Cycling, CAS= V_{IH} : $t_{RC}=t_{RC}$ MIN.) | TMM41464P-12 | — | 60 | mA 3 |
| | | TMM41464P-15 | — | 50 | |
| I_{CC4} | PAGE MODE CURRENT Average Power Supply Current, Page Mode (RAS= V_{IL} , CAS Cycling : $t_{PC}=t_{PC}$ MIN.) | TMM41464P-12 | — | 60 | mA 3,4 |
| | | TMM41464P-15 | — | 50 | |
| I_{CC5} | CAS BEFORE RAS REFRESH CURRENT Average Power Supply Current, CAS Before RAS Mode (RAS Cycling, CAS Before RAS : $t_{RC}=t_{RC}$ MIN.) | TMM41464P-12 | — | 60 | mA 3 |
| | | TMM41464P-15 | — | 50 | |
| I_{IL1} | INPUT LEAKAGE CURRENT Input Leakage Current, any input ($0V \leq V_{IN} \leq 6.5V$, All Other Pins Not Under Test = 0V) | -10 | 10 | μA | |
| I_{OL1} | OUTPUT LEAKAGE CURRENT (DOUT is disabled, $0V \leq V_{OUT} \leq +5.5V$) | -10 | 10 | μA | |
| V_{OH} | OUTPUT LEVEL Output "H" Level Voltage ($I_{OUT} = -5mA$) | 2.4 | | V | |
| V_{OL} | OUTPUT LEVEL Output "L" Level Voltage ($I_{OUT} = 4.2mA$) | | 0.4 | V | |

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

(V_{CC}=5V±10%, Ta=0~70°C) (Notes 5, 6, 7)

| SYMBOL | PARAMETER | TMM41464P-12 | | TMM41464P-15 | | UNITS | NOTES |
|------------------|---|--------------|--------|--------------|--------|-------|-------|
| | | MIN. | MAX. | MIN. | MAX. | | |
| t _{RC} | Random Read or Write Cycle Time | 220 | — | 260 | — | ns | |
| t _{RMW} | Read-Modify-Write Cycle Time | 295 | — | 355 | — | ns | |
| t _{PC} | Page Mode Cycle Time | 120 | — | 145 | — | ns | |
| t _{RAC} | Access Time from RAS | — | 120 | — | 150 | ns | 8, 10 |
| t _{CAC} | Access Time from CAS | — | 60 | — | 75 | ns | 9, 10 |
| t _{OFF} | Output Buffer Turn-Off Delay | 0 | 35 | 0 | 40 | ns | 11 |
| t _T | Transition Time (Rise and Fall) | 3 | 50 | 3 | 50 | ns | 7 |
| t _{RP} | RAS Precharge Time | 90 | — | 100 | — | ns | |
| t _{RAS} | RAS Pulse Width | 120 | 10,000 | 150 | 10,000 | ns | |
| t _{RSH} | RAS Hold Time | 60 | — | 75 | — | ns | |
| t _{CSH} | CAS Hold Time | 120 | — | 150 | — | ns | |
| t _{CAS} | CAS Pulse Width | 60 | 10,000 | 75 | 10,000 | ns | |
| t _{RCD} | RAS to CAS Delay Time | 25 | 60 | 25 | 75 | ns | 13 |
| t _{CRP} | CAS to RAS Precharge Time | 10 | — | 10 | — | ns | |
| t _{CPN} | CAS Precharge Time | 20 | — | 25 | — | ns | |
| t _{CP} | CAS Precharge Time (for Page Mode Cycle Only) | 50 | — | 60 | — | ns | |
| t _{ASR} | Row Address Set-Up Time | 0 | — | 0 | — | ns | |
| t _{RAH} | Row Address Hold Time | 15 | — | 15 | — | ns | |
| t _{ASC} | Column Address Set-Up Time | 0 | — | 0 | — | ns | |
| t _{CAH} | Column Address Hold Time | 25 | — | 35 | — | ns | |
| t _{AR} | Column Address Hold Time Reference to RAS | 85 | — | 110 | — | ns | |
| t _{RCS} | Read Command Set-Up Time | 0 | — | 0 | — | ns | |
| t _{RCH} | Read Command Hold Time Reference to CAS | 0 | — | 0 | — | ns | 12 |
| t _{RRH} | Read Command Hold Time Reference to RAS | 15 | — | 20 | — | ns | 12 |
| t _{WCH} | Write Command Hold Time | 35 | — | 45 | — | ns | |
| t _{WCR} | Write Command Hold Time Reference to RAS | 95 | — | 120 | — | ns | |
| t _{WP} | Write Command Pulse Width | 35 | — | 45 | — | ns | |
| t _{RWL} | Write Command to RAS Lead Time | 35 | — | 45 | — | ns | |
| t _{CWL} | Write Command to CAS Lead Time | 35 | — | 45 | — | ns | |
| t _{DS} | Data-In Set-Up Time | 0 | — | 0 | — | ns | 14 |
| t _{DH} | Data-In Hold Time | 35 | — | 45 | — | ns | 14 |
| t _{DHR} | Data-In Hold Time Reference to RAS | 95 | — | 120 | — | ns | |
| t _{REF} | Refresh Period | — | 4 | — | 4 | ms | |
| t _{WCS} | Write Command Set-Up Time | 0 | — | 0 | — | ns | 15 |
| t _{CWD} | CAS to WRITE Delay | 100 | — | 120 | — | ns | 15 |
| t _{RWD} | RAS to WRITE Delay | 160 | — | 195 | — | ns | 15 |
| t _{OEa} | OE Access time | — | 30 | — | 40 | ns | |
| t _{OED} | OE to Data Delay | 30 | — | 40 | — | ns | |
| t _{OEZ} | Output Buffer Turn-Off Delay Time from OE | 0 | 30 | 0 | 40 | ns | |
| t _{OEh} | OE Command Hold Time | 30 | — | 40 | — | ns | |

TMM41464P-12

TMM41464P-15

| SYMBOL | PARAMETER | TMM41464P-12 | | TMM41464P-15 | | UNITS | NOTES |
|------------------|--|--------------|------|--------------|------|-------|-------|
| | | MIN. | MAX. | MIN. | MAX. | | |
| t _{CHR} | CAS Hold Time for $\overline{\text{CAS}}$ Before RAS Refresh | 30 | — | 30 | — | ns | |
| t _{CSR} | CAS Set-Up Time for CAS Before RAS Refresh | 10 | — | 10 | — | ns | |
| t _{RPC} | CAS Precharge to CAS Active Time | 0 | — | 0 | — | ns | |
| t _{CPT} | CAS Precharge Time for CAS Before RAS Counter Test | 50 | — | 60 | — | ns | |

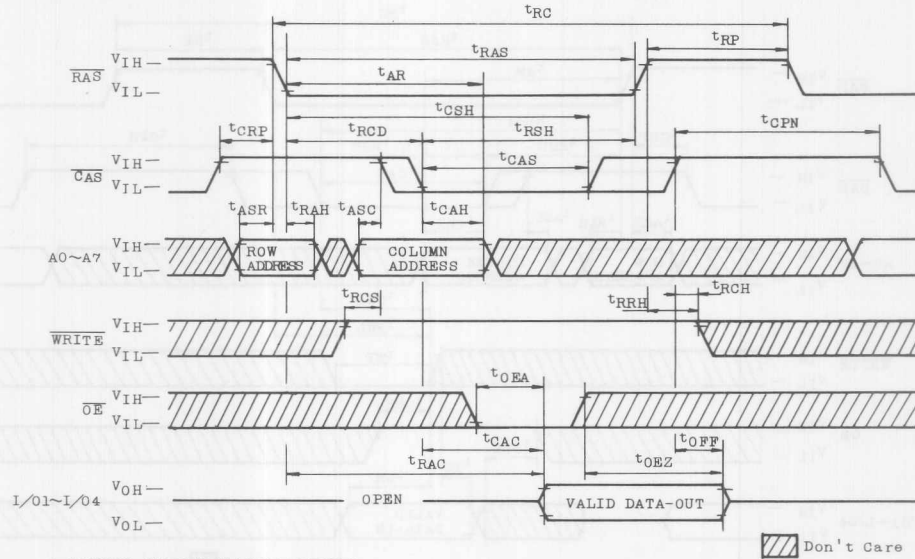
CAPACITANCE (V_{CC}=5V±10%, f=1MHz, Ta=0~70°C)

| SYMBOL | PARAMETER | MIN. | MAX. | UNITS |
|-----------------|---|------|------|-------|
| C _{I1} | Input Capacitance (A ₀ ~A ₇) | — | 5 | pF |
| C _{I2} | Input Capacitance (RAS, CAS, WRITE, OE) | — | 7 | pF |
| C _O | Input/Output Capacitance (I/O1~I/O4) | — | 7 | pF |

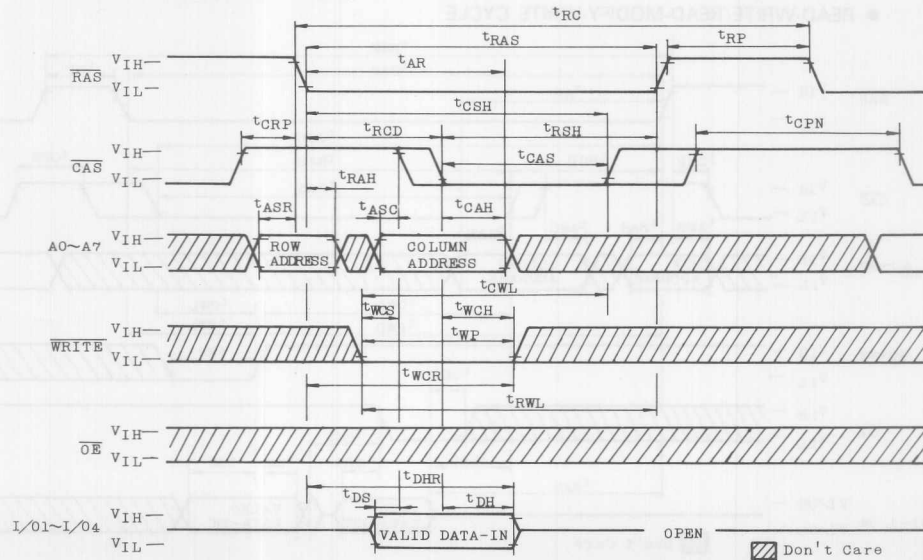
NOTES:

- Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device.
- All voltages are referenced to V_{SS}.
- I_{CC1}, I_{CC3}, I_{CC4}, I_{CC5} depend on cycle rate.
- I_{CC1}, I_{CC4} depend on output loading. Specified values are obtained with the output open.
- An initial pause of 200μs is required after power-up followed by any 8 $\overline{\text{CAS}}$ cycles before proper device operation is achieved. In case of using internal refresh counter, a minimum of 8 CAS Before RAS initialization cycles instead of 8 $\overline{\text{RAS}}$ cycle are required.
- AC measurements assume t_r = 5ns.
- V_{IH}(min.) and V_{IL}(max.) are reference levels for measuring timing of input signals. Also, transition times are measured between V_{IH} and V_{IL}.
- Assumes that t_{RCD} ≤ t_{RCD} (max.). If t_{RCD} is greater than the maximum recommended value shown in this table, t_{TRAC} will increase by the amount that t_{RCD} exceeds the value shown.
- Assumes that t_{RCD} ≥ t_{RCD} (max.).
- Measured with a load equivalent to 2 TLL loads and 100pF.
- t_{OFF} (max.) defines the time at which the output achieves the open circuit condition and is not referenced to output voltage levels.
- Either t_{TRCH} or t_{TRRH} must be satisfied for a read cycle.
- Operation within the t_{RCD} (max.) limit insures that t_{TRAC} (max.) can be met.
t_{RCD} (max.) is specified as a reference point only: If t_{RCD} is greater than the specified t_{RCD} (max.) limit, then access time is controlled exclusively by t_{CAC}.
- These parameters are referenced to $\overline{\text{CAS}}$ leading edge in early write cycles and to $\overline{\text{WRITE}}$ leading edge in read-write or read-modify-write cycles.
- t_{WCS}, t_{WD} and t_{WD} are not restrictive operating parameters. They are included in the data sheet as electrical characteristics only. If t_{WCS} ≥ t_{WCS} (min.), the cycle is an early write cycle and the input/output pin will remain open circuits (high impedance) throughout the entire cycle; If t_{WD} ≥ t_{WD} (min.) and t_{WD} ≥ t_{WD}(min.), the cycle is a read-write cycle or read-modify-write cycle and the data out will contain data read from the selected cell.

● READ CYCLE



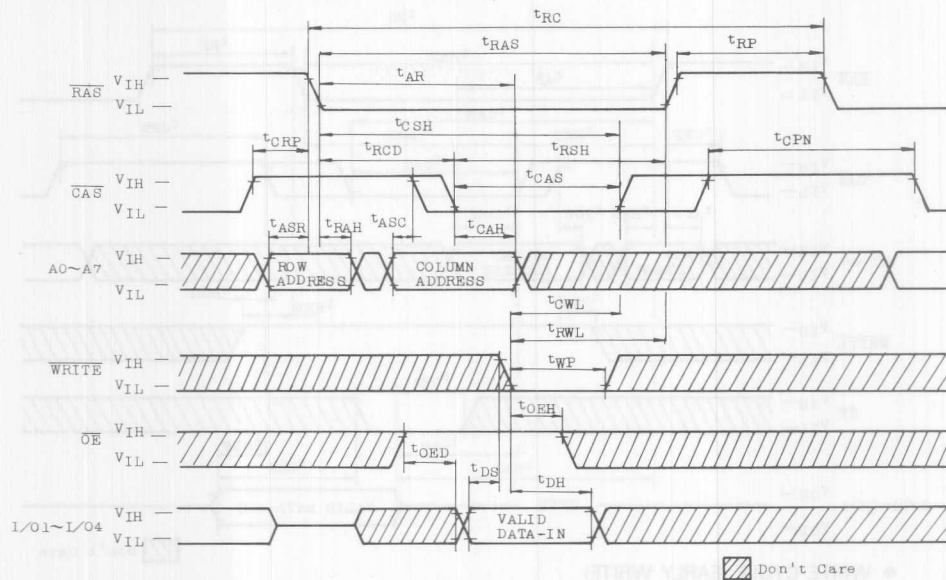
● WRITE CYCLE (EARLY WRITE)



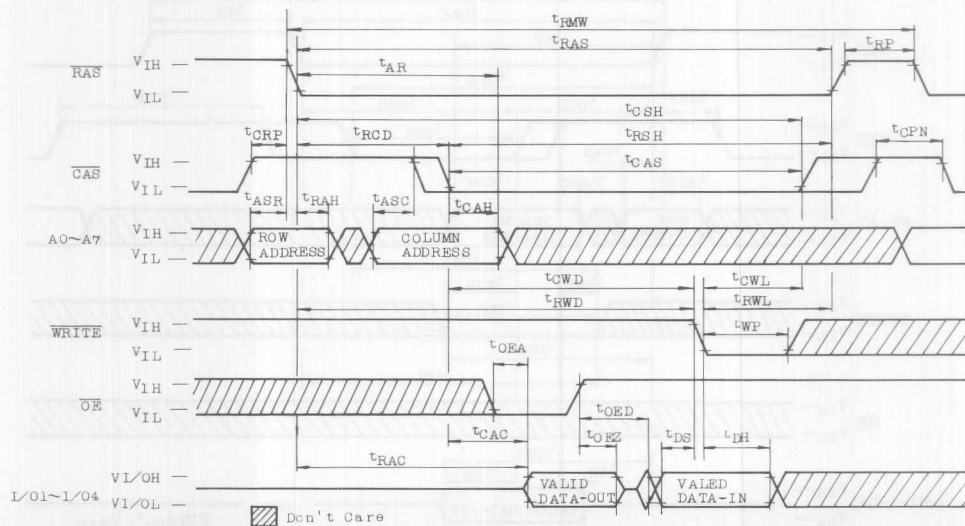
TMM41464P-12

TMM41464P-15

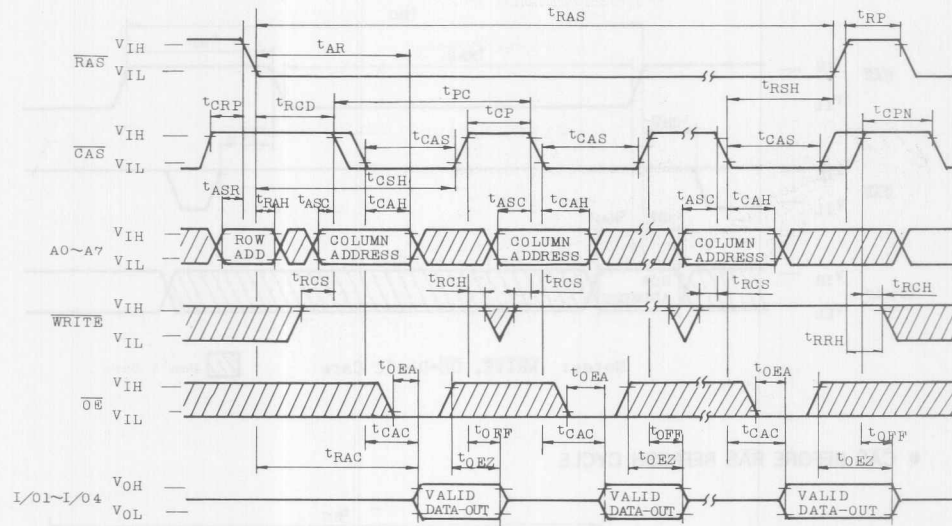
● WRITE CYCLE ($\overline{\text{OE}}$ CONTROLLED WRITE)



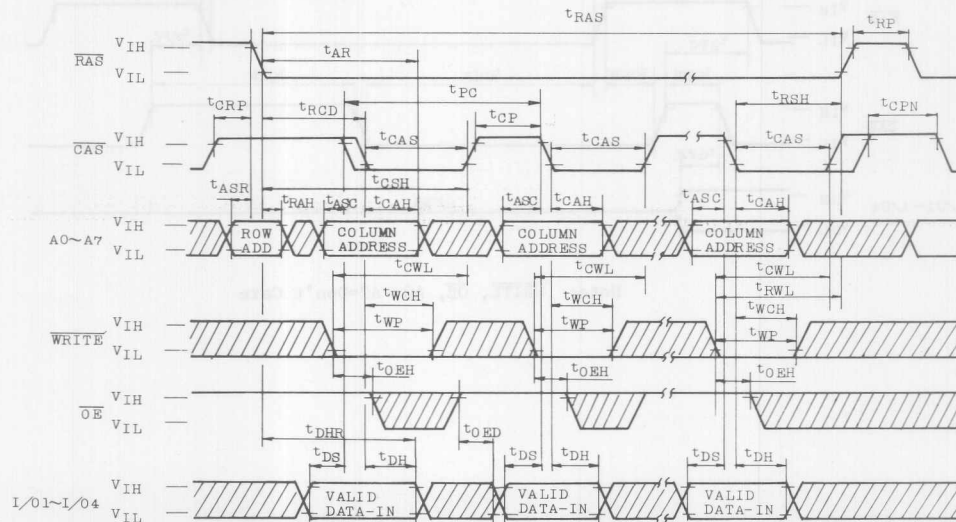
● READ-WRITE/READ-MODIFY-WRITE CYCLE



● PAGE MODE READ CYCLE

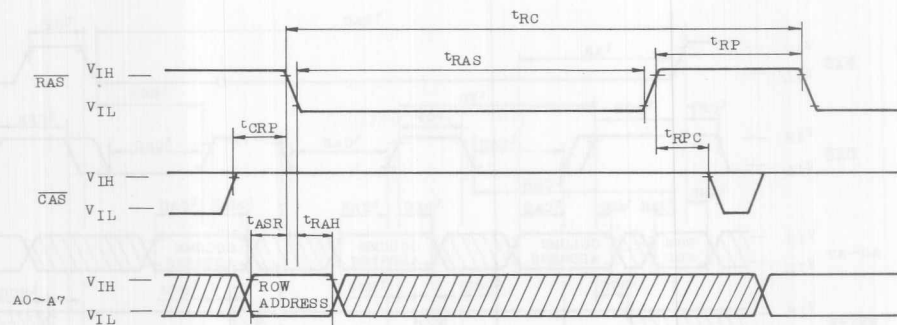


● PAGE MODE WRITE CYCLE



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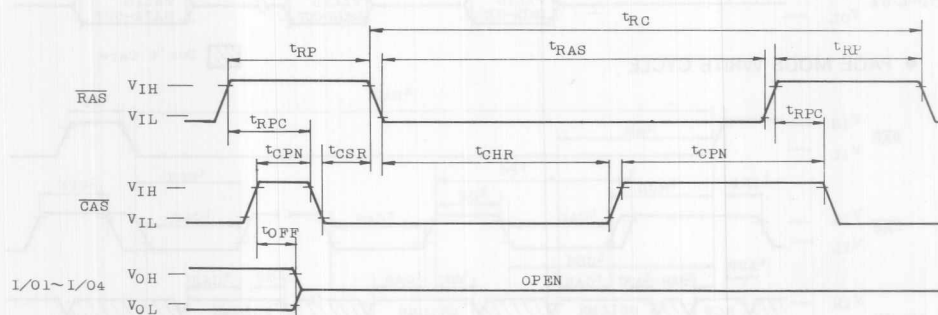
● $\overline{\text{RAS}}$ ONLY REFRESH CYCLE



Notes: $\overline{\text{WRITE}}$, $\overline{\text{OE}}$ =Don't Care

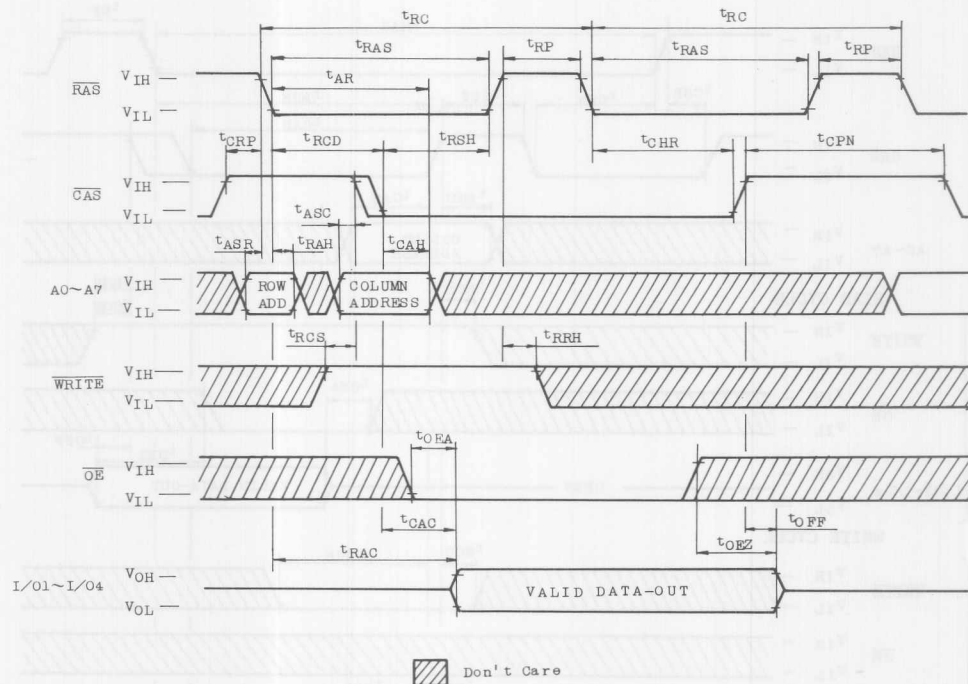
Don't Care

● $\overline{\text{CAS}}$ BEFORE $\overline{\text{RAS}}$ REFRESH CYCLE



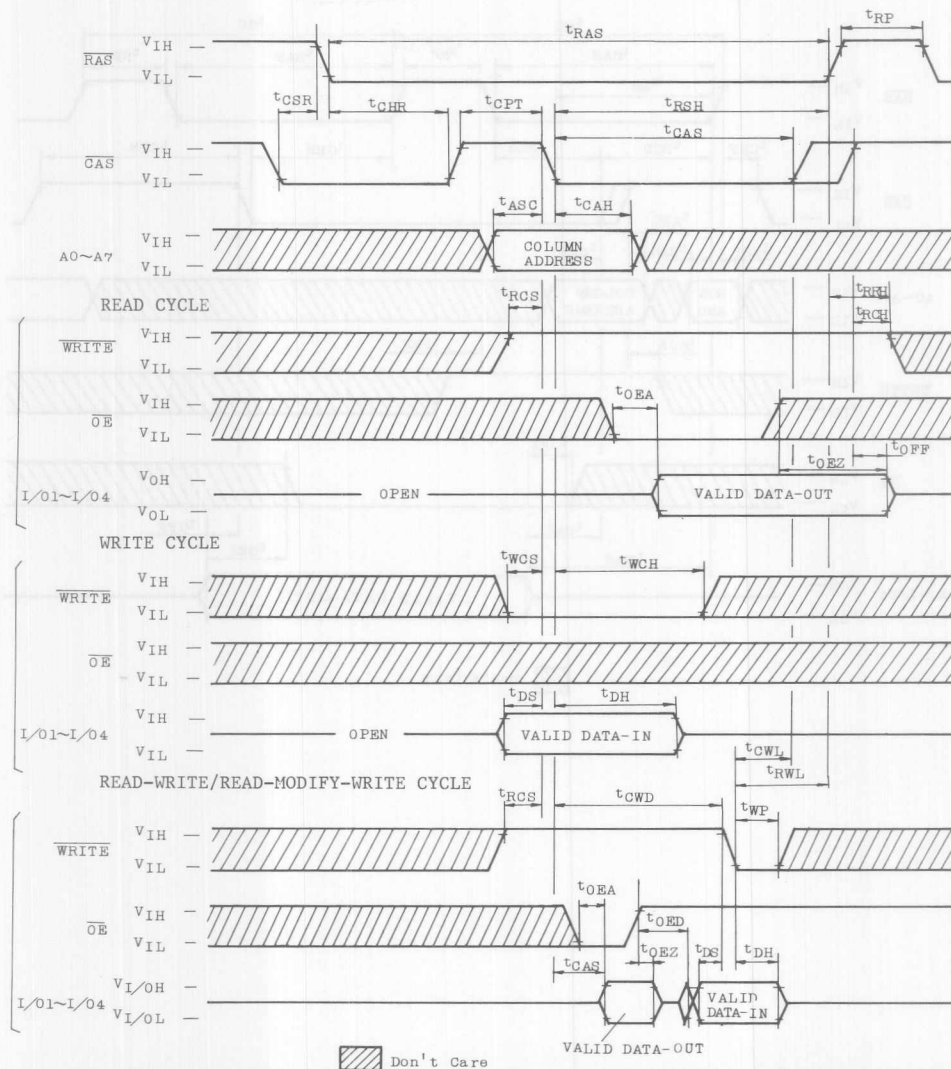
Note: $\overline{\text{WRITE}}$, $\overline{\text{OE}}$, $\text{A0} \sim \text{A7}$ =Don't Care

● HIDDEN REFRESH CYCLE



TMM41464P-12 TMM41464P-15

• CAS BEFORE RAS REFRESH COUNTER TEST CYCLE



APPLICATION INFORMATION

ADDRESSING

The 16 address bits required to decode 1 of the 65,536 cell locations within the TMM41464P are multiplexed onto the 8 address inputs and latched into the on-chip address latches by externally applying two negative going TTL-level clocks.

The first clock, the Row Address Strobe ($\overline{\text{RAS}}$), latches the 8 row address bits into the chip. The second clock, the Column Address Strobe ($\overline{\text{CAS}}$), subsequently latches the 8 column address bits into the chip. Each of these signals, $\overline{\text{RAS}}$, and $\overline{\text{CAS}}$, triggers a sequence of events which are controlled by different delayed internal clocks.

The two clock chains are linked together logically in such a way that the address multiplexing operation is done outside of the critical path timing sequence for read data access. The later events in the $\overline{\text{CAS}}$ clock sequence are inhibited until the occurrence of a delayed signal derived from the $\overline{\text{RAS}}$ clock chain. This "gated $\overline{\text{CAS}}$ " feature allows the $\overline{\text{CAS}}$ clock to be externally activated as soon as the Row Address Hold Time specification (t_{RAH}) has been satisfied and the address inputs have been changed from Row address to Column address information.

Data Inputs

Data is written during write or read-modify-write cycle.

The falling edge of $\overline{\text{CAS}}$ or $\overline{\text{WRITE}}$ strobes data into the on-chip data latches.

In an early-write cycle, $\overline{\text{WRITE}}$ is brought low prior to $\overline{\text{CAS}}$ and the data is strobed in by $\overline{\text{CAS}}$ with setup and hold times referenced to this signal. In delayed write or read-modify-write cycle, $\overline{\text{CAS}}$ will already be low, thus the data will be strobed in by $\overline{\text{WRITE}}$ with setup and hold time referenced to this signal.

In delayed or read-modify-write, $\overline{\text{OE}}$ must be high to bring the output buffers to high impedance prior to impressing data on the I/O lines.

Data outputs

The three-state output buffers provide direct TTL compatibility with a fan-out of two standard TTL loads. Data-out is the same polarity as data-in. The outputs are in the high-impedance state until $\overline{\text{CAS}}$ is brought low. In a read cycle the outputs go active after the access time interval t_{RAc} and t_{OEa} are satisfied.

The outputs become valid after the access time has elapsed and remain valid while $\overline{\text{CAS}}$ and $\overline{\text{OE}}$ are

low. $\overline{\text{CAS}}$ or $\overline{\text{OE}}$ going high returns it to a high impedance state. In an early-write cycle, the outputs are always in the high-impedance state. In a delayed-write or read-modify-write cycle, the outputs will follow the sequence for the read cycle.

The $\overline{\text{OE}}$ controls the impedance of the output buffers. In the logic high position the buffers will remain in a high impedance state.

When the $\overline{\text{OE}}$ input is brought to a logic low level, the output buffers are enabled. Both $\overline{\text{CAS}}$ and $\overline{\text{OE}}$ can control the outputs. Thus in a read operation, either $\overline{\text{OE}}$ or $\overline{\text{CAS}}$ returning high forces the outputs into the high impedance state.

$\overline{\text{RAS}}$ ONLY REFRESH

Refresh of the dynamic cell matrix is accomplished by performing a memory cycle at each of the 256 row address (A_0 - A_7) within each 4 millisecond time interval. Although any normal memory cycle will perform the refresh operation, this function is most easily accomplished with "RAS-only" cycles. RAS only refresh results in a substantial reduction in operating power. This reduction in power is reflected in the I_{CC3} specification.

$\overline{\text{CAS}}$ BEFORE $\overline{\text{RAS}}$ REFRESH

$\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ refreshing available on the TMM41464P offers an alternate refresh method. If $\overline{\text{CAS}}$ is held on low for the specified period (t_{CSR}) before $\overline{\text{RAS}}$ goes to low, on chip refresh control clock generators and the refresh address counter are enabled, and an internal refresh operation takes place.

After the refresh operation is performed, the refresh address counter is automatically incremented in preparation for the next $\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ refresh operation.

PAGE MODE

The "Page-Mode" feature of the TMM41464P allows for successive memory operations at multiple column locations of the same row address with increased speed without an increase in power. This is done by strobing the row address into the chip and maintaining the $\overline{\text{RAS}}$ signal at a logic 0 throughout all successive memory cycles in which the row address is common. This "Page-Mode" of operation will not dissipate the power associated with the negative

TMM41464P-12

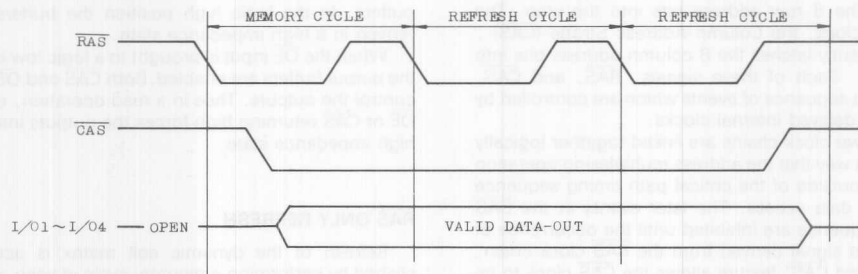
TMM41464P-15

going edge of $\overline{\text{RAS}}$. Also, the time required for strobing in a new address is eliminated, thereby decreasing the access and cycle times.

HIDDEN REFRESH

An optional feature of the TMM41464P is that

refresh cycle may be performed while maintaining valid data at the output pin. This is referred to as Hidden Refresh. Hidden Refresh is performed by holding $\overline{\text{CAS}}$ at V_{IL} and taking $\overline{\text{RAS}}$ high after a specified precharge period (t_{RP}), executing a $\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ refresh cycle. (see Figure below)



This feature allows a refresh cycle to be "hidden" among data cycles without affecting the data availability.

$\overline{\text{CAS}}$ BEFORE $\overline{\text{RAS}}$ REFRESH COUNTER TEST

The internal refresh operation of TMM41464P can be tested by $\overline{\text{CAS}}$ BEFORE $\overline{\text{RAS}}$ REFRESH COUNTER TEST. This cycle performs READ/WRITE operation taking the internal counter address as row address and the input address as column address.

The test is performed after a minimum of 8 $\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ cycles as initialization cycles. The test procedure is as follows.

- ① Write "0" into all the memory cells at normal write mode.
- ② Select one certain column address and read "0" out and write "1" in each cell by performing $\overline{\text{CAS}}$

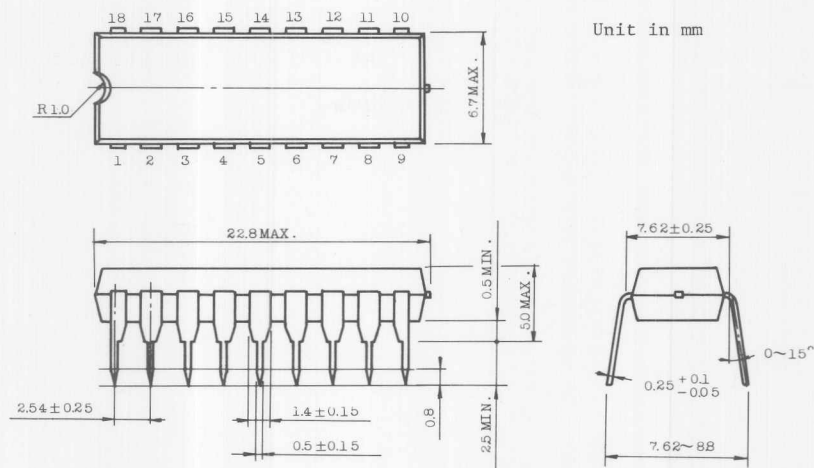
BEFORE $\overline{\text{RAS}}$ REFRESH COUNTER TEST (READ-WRITE CYCLE).

Repeat this operation 256 times.

- ③ Check "1" out of 256 bits at normal read mode, which was written at ②.
- ④ Using the same column as ②, read "1" out and write "0" in each cell performing $\overline{\text{CAS}}$ BEFORE $\overline{\text{RAS}}$ REFRESH COUNTER TEST. Repeat this operation 256 times.
- ⑤ Check "0" out of 256 bits at normal read mode, which was written at ④.
- ⑥ Perform the above ① to ⑤ to the complement data.

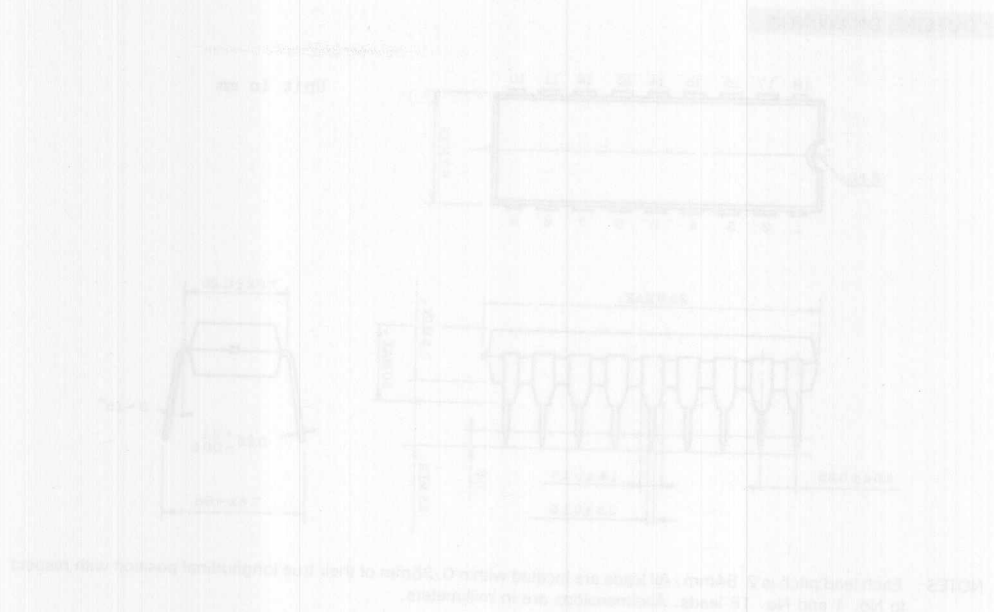
TMM41464P-12 TMM41464P-15

OUTLINE DRAWINGS



NOTES : Each lead pitch is 2.54mm. All leads are located within 0.25mm of their true longitudinal position with respect to No. 1 and No. 18 leads. All dimensions are in millimeters.

TMM41464P-12 TMM41464P-15



Note : Toshiba does not assume any responsibility for use of any circuitry described ; no circuit patent licenses are implied, and Toshiba reserves the right, at any time without notice, to change said circuitry.
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TOSHIBA MOS MEMORY PRODUCTS

1,048,576 WORD × 1 BIT DYNAMIC RAM
SILICON MONOLITHIC
N-CHANNEL SILICON GATE MOS

TMM411000C-10
TMM411000C-12

PRELIMINARY

DESCRIPTION

The TMM411000C is the new generation dynamic RAM organized 1,048,576 words by 1 bit, it is successor to the industry standard TMM41256P. The TMM411000C utilizes TOSHIBA's N-channel Silicon gate process technology as well as advanced circuit techniques to provide wide operating margins, both internally and to the system user. Multiplexed address inputs permit the TMM411000C to be packaged in a standard 18 pin

ceramic DIP. This package size provides high system bit densities and is compatible with widely available automated testing and insertion equipment. System oriented features include single power supply of $5V \pm 10\%$ tolerance, direct interfacing capability with high performance logic families such as Schottky TTL. In addition to the RAS only refresh mode, a CAS before RAS automatic refresh is available.

FEATURES

- 1,048,576 words by 1 bit organization
- Fast access time and cycle time

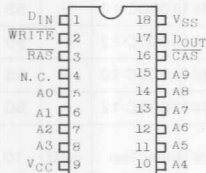
| | TMM411000C-10 | TMM411000C-12 |
|-----------------|---------------|---------------|
| RAS Access Time | 100ns | 120ns |
| CAS Access Time | 50ns | 60ns |
| Cycle Time | 190ns | 220ns |

- Single power supply of $5V \pm 10\%$ with a built-in V_{BB} generator
- Low Power :
385mW Operating(MAX.) (TMM411000C-10)
330mW Operating(MAX.) (TMM411000C-12)

22mW Standby(MAX.)

- Industry standard 18 pin ceramic DIP
- Output unlatched at cycle end allows two-dimensional chip selection
- Common I/O capability using "EARLY WRITE" operation
- Read-Modify-Write, $\overline{\text{CAS}}$ before RAS refresh, RAS-only refresh, Hidden refresh, and Page Mode capability
- All inputs and output TTL compatible
- 512 refresh cycles/8ms

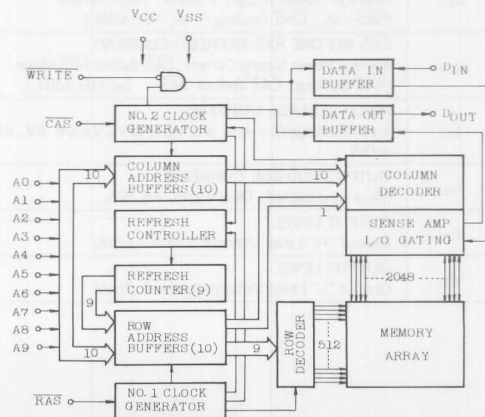
PIN CONNECTION (TOP VIEW)



PIN NAMES

| | |
|--------------------------------|-----------------------|
| A ₀ ~A ₉ | Address Inputs |
| CAS | Column Address Strobe |
| D _{IN} | Data In |
| D _{OUT} | Data Out |
| RAS | Row Address Strobe |
| WRITE | Read/Write Input |
| V _{CC} | Power (+5V) |
| V _{SS} | Ground |
| N. C. | No Connection |

BLOCK DIAGRAM



TMM411000C-10

TMM411000C-12

ABSOLUTE MAXIMUM RATINGS

| ITEM | SYMBOL | RATING | UNITS | NOTES |
|------------------------------|-------------------|---------|--------|-------|
| Input and Output Voltage | V_{IN}, V_{OUT} | -1~7 | V | 1 |
| Power Supply Voltage | V_{CC} | -1~7 | V | 1 |
| Operating Temperature | T_{OPR} | 0~70 | °C | 1 |
| Storage Temperature | T_{STG} | -55~150 | °C | 1 |
| Soldering Temperature•Time | T_{SOLDER} | 260•10 | °C•sec | 1 |
| Power Dissipation | P_D | 1 | W | 1 |
| Short Circuit Output Current | I_{OUT} | 50 | mA | 1 |

RECOMMENDED DC OPERATING CONDITIONS (Ta=0~70°C)

| SYMBOL | PARAMETER | MIN. | TYP. | MAX. | UNIT | NOTES |
|----------|--------------------|------|------|------|------|-------|
| V_{CC} | Supply Voltage | 4.5 | 5.0 | 5.5 | V | 2 |
| V_{IH} | Input High Voltage | 2.4 | — | 6.5 | V | 2 |
| V_{IL} | Input Low Voltage | -1.0 | — | 0.8 | V | 2 |

DC ELECTRICAL CHARACTERISTICS (Vcc=5V±10%, Ta=0~70°C)

| SYMBOL | PARAMETER | MIN. | MAX. | UNITS | NOTES |
|-----------------|--|---------------|------|-------|-------|
| Icc1 | OPERATING CURRENT Average Power Supply Operating Current (RAS, CAS Cycling : t _{RC} =t _{RC} MIN.) | TMM411000C-10 | — 70 | mA | 3, 4 |
| | | TMM411000C-12 | — 60 | | |
| Icc2 | STANDBY CURRENT Power Supply Standby Current (RAS=CAS=V _{IH}) | — | 4 | mA | |
| Icc3 | RAS ONLY REFRESH CURRENT Average Power Supply Current, RAS Only Mode (RAS Cycling, CAS=V _{IH} : t _{RC} =t _{RC} MIN.) | TMM411000C-10 | — 55 | mA | 3 |
| | | TMM411000C-12 | — 50 | | |
| Icc4 | PAGE MODE CURRENT Average Power Supply Current, PAGE Mode (RAS=V _{IL} , CAS Cycling : t _{PC} =t _{PC} MIN.) | TMM411000C-10 | — 55 | mA | 3, 4 |
| | | TMM411000C-12 | — 50 | | |
| Icc5 | CAS BEFORE RAS REFRESH CURRENT Average Power Supply Current, CAS Before RAS Mode (RAS Cycling, CAS Before RAS : t _{RC} =t _{RC} MIN.) | TMM411000C-10 | — 55 | mA | 3 |
| | | TMM411000C-12 | — 50 | | |
| I _{IL} | INPUT LEAKAGE CURRENT Input Leakage Current, any input (0V≤V _{IN} ≤6.5V, All Other Pins Not Under Test =0V) | -10 | 10 | μA | |
| I _{OL} | OUTPUT LEAKAGE CURRENT (Dout is disabled, 0V≤V _{OUT} ≤+5.5V) | -10 | 10 | μA | |
| V _{OH} | OUTPUT LEVEL Output "H" Level Voltage (I _{OUT} =-5mA) | 2.4 | — | V | |
| V _{OL} | OUTPUT LEVEL Output "L" Level Voltage (I _{OUT} =+4.2mA) | — | 0.4 | V | |

TMM411000C-10

TMM411000C-12

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

(V_{CC}=5V±10%, T_a=0~70°C) (Notes 5, 6, 7)

| SYMBOL | PARAMETER | TMM411000C-10 | | TMM411000C-12 | | UNITS | NOTES |
|------------------|--|---------------|--------|---------------|--------|-------|-------|
| | | MIN. | MAX. | MIN. | MAX. | | |
| t _{RC} | Random Read or Write Cycle Time | 190 | — | 220 | — | ns | |
| t _{RWC} | Read-Write Cycle Time | 210 | — | 240 | — | ns | |
| t _{RMW} | Read-Modify-Write Cycle Time | 225 | — | 260 | — | ns | |
| t _{PC} | Page Mode Cycle Time | 100 | — | 120 | — | ns | |
| t _{RAC} | Access Time from RAS [—] | — | 100 | — | 120 | ns | 8,10 |
| t _{CAC} | Access Time from CAS [—] | — | 50 | — | 60 | ns | 9,10 |
| t _{OFF} | Output Buffer Turn-Off Delay | 5 | 30 | 5 | 35 | ns | 11 |
| t _T | Transition Time (Rise and Fall) | 3 | 50 | 3 | 50 | ns | 7 |
| t _{RP} | RAS Precharge Time | 80 | — | 90 | — | ns | |
| t _{RAS} | RAS Pulse Width | 100 | 10,000 | 120 | 10,000 | ns | |
| t _{RSH} | RAS Hold Time | 50 | — | 60 | — | ns | |
| t _{CSH} | CAS Hold Time | 100 | — | 120 | — | ns | |
| t _{CAS} | CAS Pulse Width | 50 | 10,000 | 60 | 10,000 | ns | |
| t _{RCD} | RAS to CAS Delay Time | 20 | 50 | 25 | 60 | ns | 13 |
| t _{CRP} | CAS to RAS Precharge Time | 10 | — | 10 | — | ns | |
| t _{CPN} | CAS Precharge Time | 20 | — | 25 | — | ns | |
| t _{CP} | CAS Precharge Time (Page mode only) | 40 | — | 50 | — | ns | |
| t _{ASR} | Row Address Set-Up Time | 0 | — | 0 | — | ns | |
| t _{RAH} | Row Address Hold Time | 10 | — | 15 | — | ns | |
| t _{ASC} | Column Address Set-Up Time | 0 | — | 0 | — | ns | |
| t _{CAH} | Column Address Hold Time | 20 | — | 25 | — | ns | |
| t _{AR} | Column Address Hold Time Reference to RAS [—] | 70 | — | 85 | — | ns | |
| t _{RCS} | Read Command Set-Up Time | 0 | — | 0 | — | ns | |
| t _{RCH} | Read Command Hold Time Reference to CAS [—] | 0 | — | 0 | — | ns | 12 |
| t _{RRH} | Read Command Hold Time Reference to RAS [—] | 10 | — | 15 | — | ns | 12 |
| t _{WCH} | Write Command Hold Time | 20 | — | 25 | — | ns | |
| t _{WCR} | Write Command Hold Time Reference to RAS [—] | 70 | — | 85 | — | ns | |
| t _{WP} | Write Command Pulse Width | 20 | — | 25 | — | ns | |
| t _{RWL} | Write Command to RAS Lead Time | 30 | — | 35 | — | ns | |
| t _{CWL} | Write Command to CAS Lead Time | 30 | — | 35 | — | ns | |
| t _{DS} | Data-In Set-Up Time | 0 | — | 0 | — | ns | 14 |
| t _{DH} | Data-In Hold Time | 20 | — | 25 | — | ns | 14 |
| t _{DHR} | Data-In Hold Time Reference to RAS [—] | 70 | — | 85 | — | ns | |
| t _{REF} | Refresh Period | — | 8 | — | 8 | ms | |
| t _{WCS} | Write Command Set-Up Time | —5 | — | —5 | — | ns | 15 |
| t _{CWD} | CAS to WRITE Delay | 35 | — | 40 | — | ns | 15 |
| t _{RWD} | RAS to WRITE Delay | 85 | — | 100 | — | ns | 15 |
| t _{CSR} | CAS Set-up Time (CAS before RAS) | 10 | — | 10 | — | ns | |
| t _{CHR} | CAS Hold Time (CAS before RAS) | 30 | — | 30 | — | ns | |
| t _{RPC} | RAS Precharge to CAS Active Time | 0 | — | 0 | — | ns | |
| t _{CPT} | CAS Precharge Time (CAS before RAS Counter Test) | 40 | — | 50 | — | ns | |

TMM411000C-10

TMM411000C-12

CAPACITANCE (V_{CC}=5V±10%, f=1MHz, Ta=0~70°C)

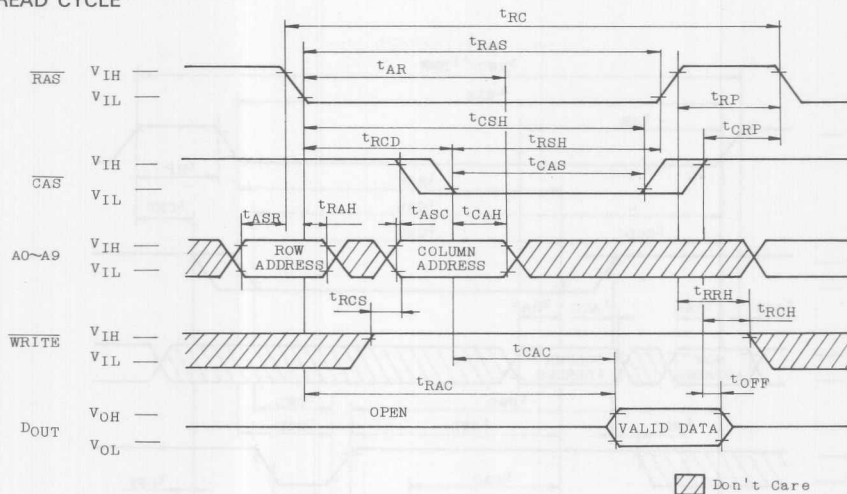
| SYMBOL | PARAMETER | MIN. | MAX. | UNIT |
|-----------------|---|------|------|------|
| C _{I1} | Input Capacitance (A ₀ ~A ₉ , D _{IN}) | — | 6 | pF |
| C _{I2} | Input Capacitance (RAS, CAS, WRITE) | — | 7 | pF |
| C _O | Output Capacitance (D _{OUT}) | — | 7 | pF |

NOTES:

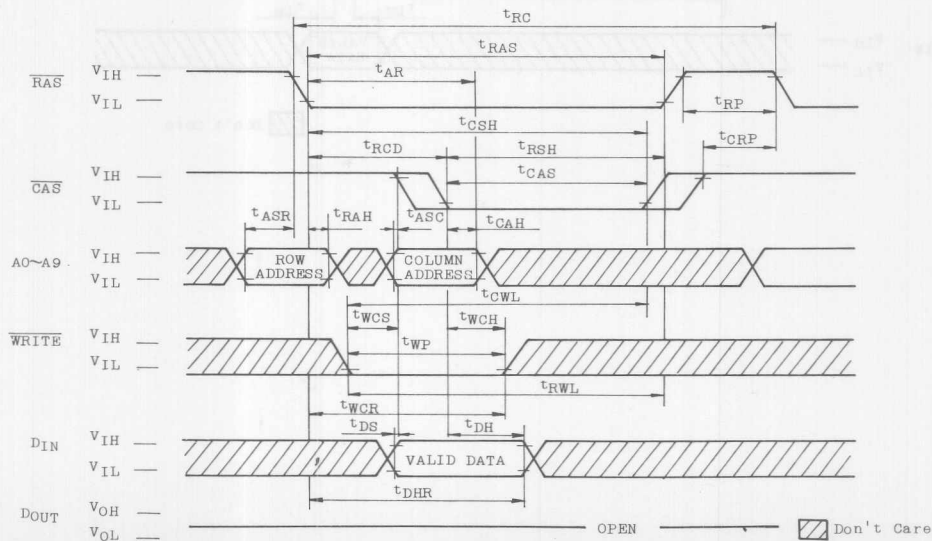
- Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device.
- All voltages are referenced to V_{SS}.
- I_{CC1}, I_{CC3}, I_{CC4}, I_{CC5} depend on cycle rate.
- I_{CC1}, I_{CC4} depend on output loading. Specified values are obtained with the output open.
- An initial pause of 200μs is required after power-up followed by any 8 RAS cycles before proper device operation is achieved. In case of using internal refresh counter, a minimum of 8 CAS Before RAS initialization cycles instead of 8 RAS cycles are required.
- AC measurements assume t_r=5ns.
- V_{IH}(min.) and V_{IL}(max.) are reference levels for measuring timing of input signals. Also, transition times are measured between V_{IH} and V_{IL}.
- Assumes that t_{RCD} ≤ t_{RCD}(max.). If t_{RCD} is greater than the maximum recommended value shown in this table, t_{RAC} will increase by the amount that t_{RCD} exceeds the value shown.
- Assume that t_{RCD} ≥ t_{RCD}(max.).
- Measured with a load equivalent to 2 TTL loads and 100pF.
- t_{OFF}(max.) defines the time at which the output achieves the open circuit condition and is not referenced to output voltage levels.
- Either t_{RCH} or t_{RRH} must be satisfied for a read cycle.
- Operation within the t_{RCD}(max.) limit insures that t_{RAC}(max.) can be met.
t_{RCD}(max.) is specified as a reference point only: If t_{RCD} is greater than the specified t_{RCD}(max.) limit, then access time is controlled exclusively by t_{CAC}.
- These parameters are referenced to CAS leading edge in early write cycles and to WRITE leading edge in read-write or read-modify-write cycles.
- t_{WCS}, t_{CWD} and t_{RWD} are not restrictive operating parameters. They are included in the data sheet as electrical characteristics only. If t_{WCS} ≥ t_{WCS}(min.), the cycle is an early write cycle and the data out pin will remain open circuit (high impedance) throughout the entire cycle; If t_{CWD} ≥ t_{CWD}(min.) and t_{RWD} ≥ t_{RWD}(min.), the cycle is a read-write cycle or read-modify-write cycle and the data out will contain data read from the selected cell: If neither of the above sets of conditions is satisfied, the condition of the data out (at access time) is indeterminate.

TIMING WAVEFORMS

● READ CYCLE

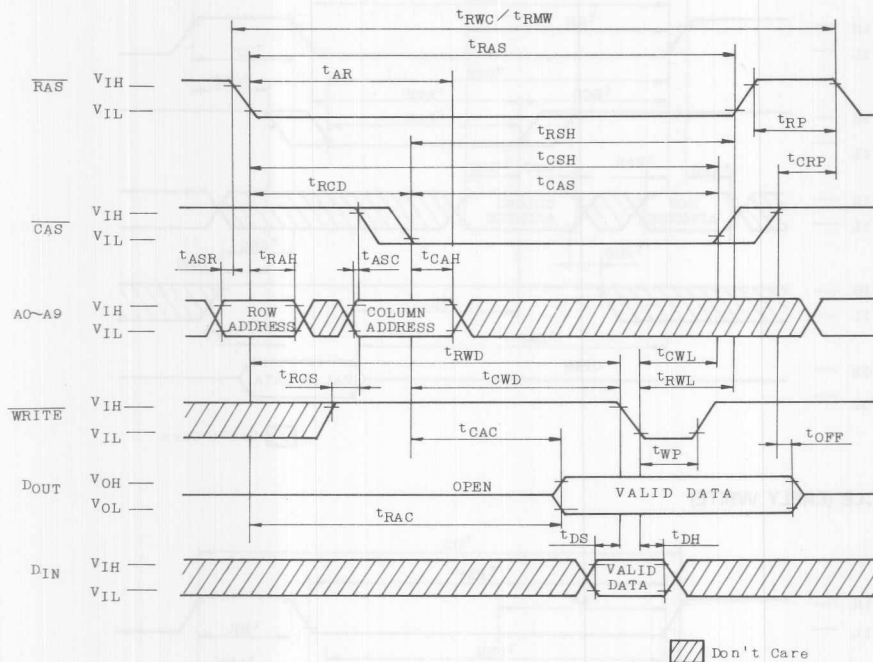


● WRITE CYCLE (EARLY WRITE)

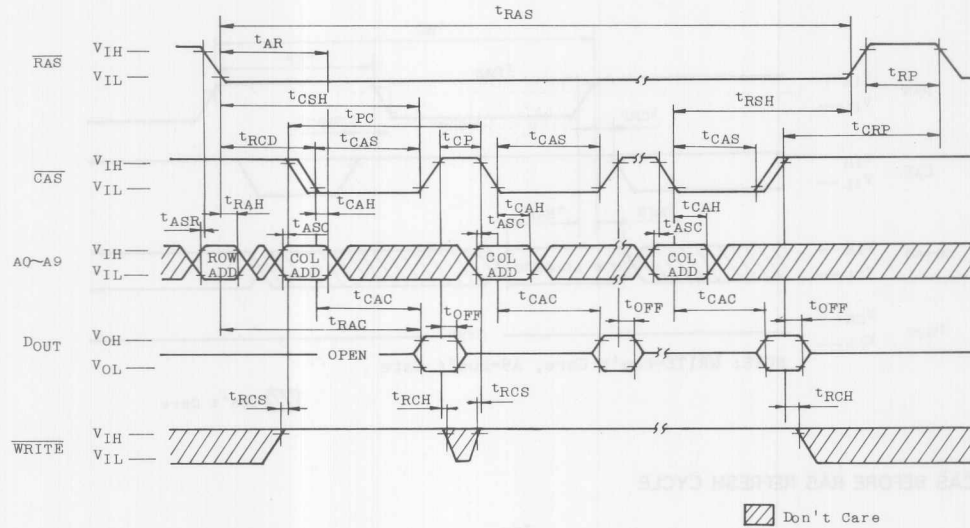


TMM411000C-10 TMM411000C-12

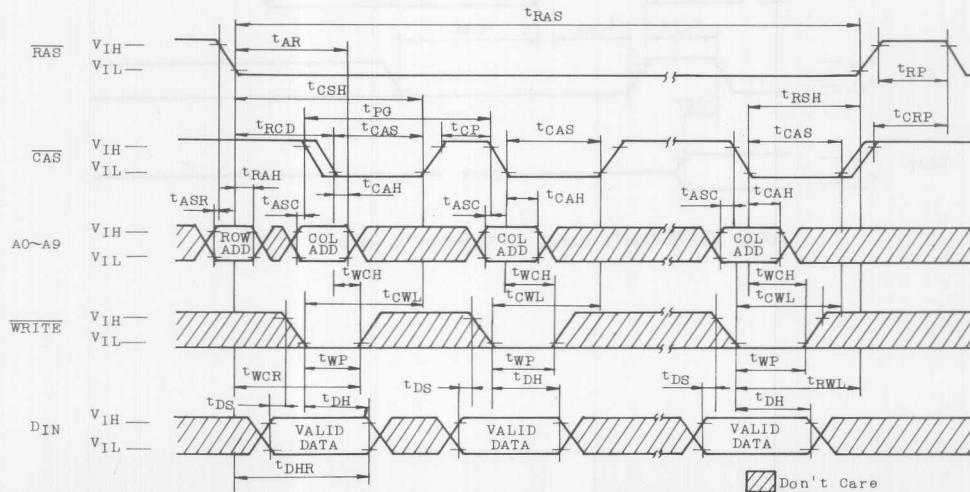
• READ-WRITE/READ-MODIFY-WRITE CYCLE



● PAGE MODE READ CYCLE

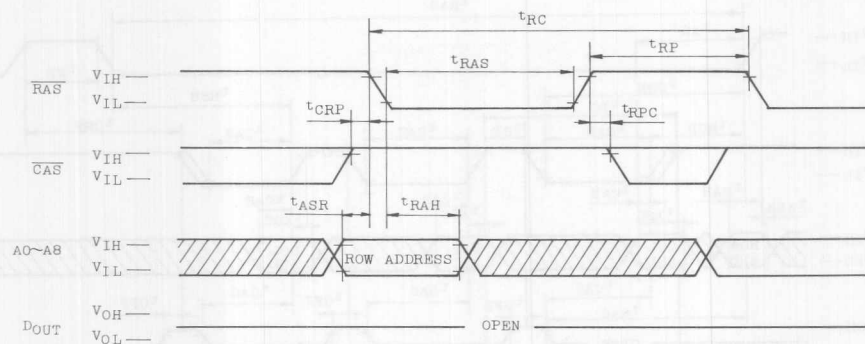


● PAGE MODE WRITE CYCLE



TMM411000C-10 TMM411000C-12

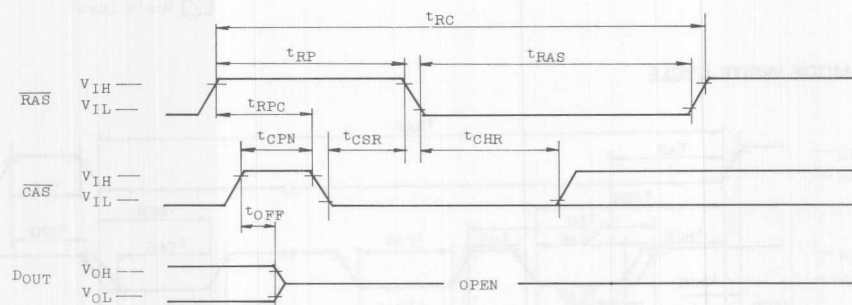
● $\overline{\text{RAS}}$ ONLY REFRESH CYCLE



NOTE: $\overline{\text{WRITE}}$ =Don't Care, A9 =Don't Care

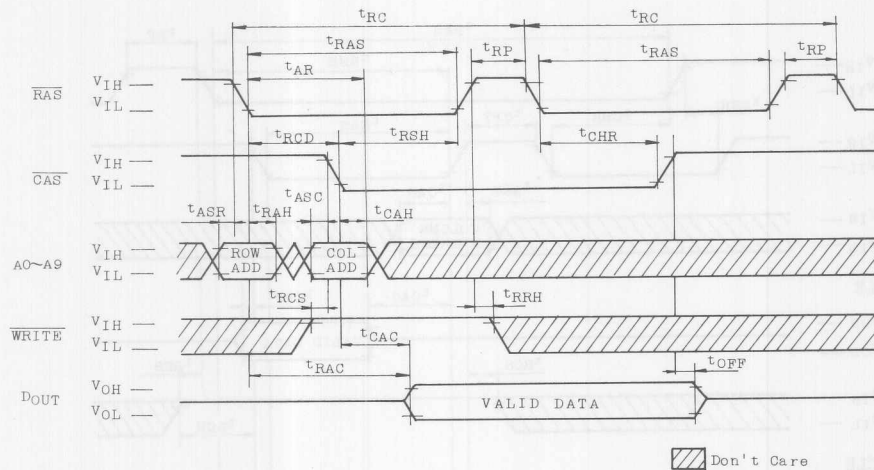
Don't Care

● $\overline{\text{CAS}}$ BEFORE $\overline{\text{RAS}}$ REFRESH CYCLE

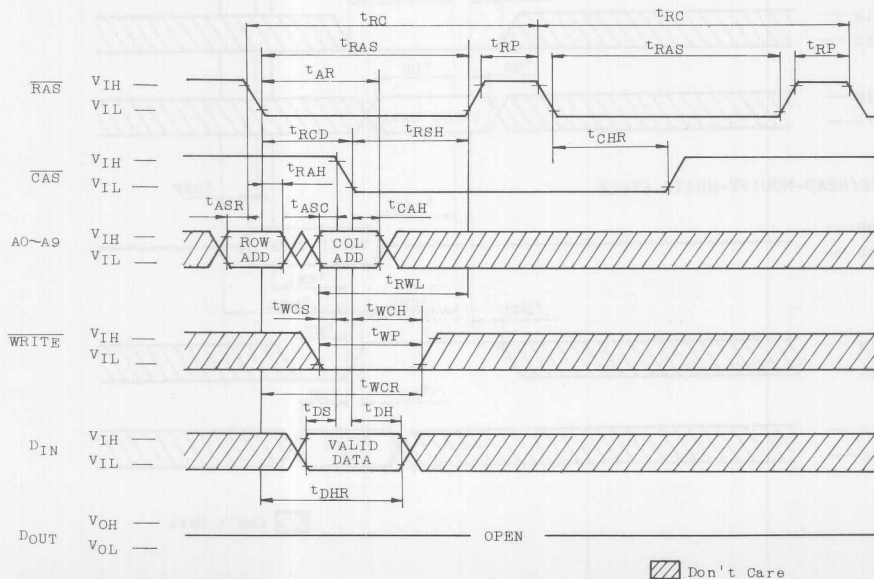


NOTE: $\overline{\text{WRITE}}$ =Don't Care, $\text{A0} \sim \text{A9}$ =Don't Care

- HIDDEN REFRESH CYCLE (READ)



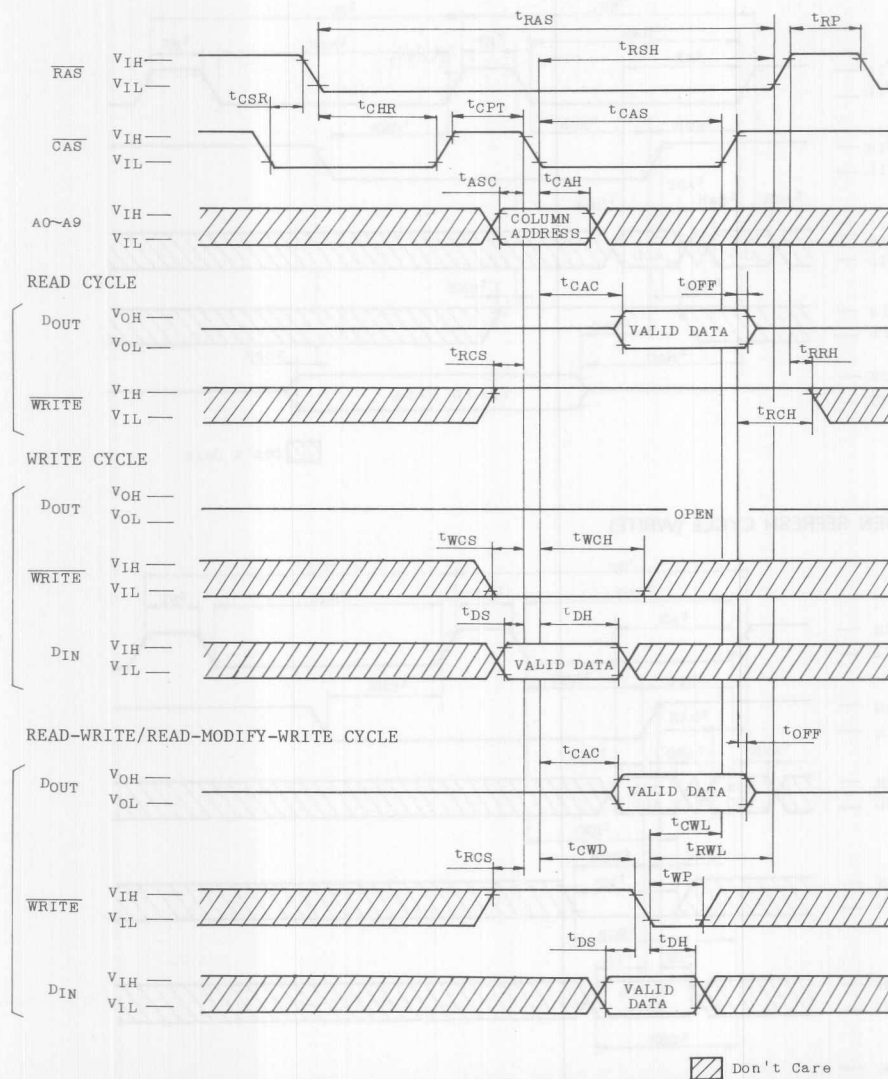
- HIDDEN REFRESH CYCLE (WRITE)



TMM411000C-10

TMM411000C-12

● $\overline{\text{CAS}}$ BEFORE $\overline{\text{RAS}}$ REFRESH COUNTER TEST CYCLE



APPLICATION INFORMATION

ADDRESSING

The 20 address bits required to decode 1 of the 1,048,576 cell locations within the TMM411000C are multiplexed onto the 10 address inputs and latched into the on-chip address latches by externally applying two negative going TTL-level clocks.

The first clock, the Row Address Strobe (RAS), latches the 10 row address bits into the chip. The second clock, the Column Address Strobe (CAS), subsequently latches the 10 column address bits into the chip. Each of these signals, RAS, and CAS, triggers a sequence of events which are controlled by different delayed internal clocks.

The two clock chains are linked together logically in such a way that the address multiplexing operation is done outside of the critical path timing sequence for read data access. The later events in the CAS clock sequence are inhibited until the occurrence of a delayed signal derived from the RAS clock chain. This "gated CAS" feature allows the CAS clock to be externally activated as soon as the Row Address Hold Time specification (t_{RAH}) has been satisfied and the address inputs have been changed from Row address to Column address information.

DATA INPUT/OUTPUT

Data to be written into a selected cell is latched into an on-chip register by a combination of \overline{WRITE} and \overline{CAS} while \overline{RAS} is active. The later of the signals (\overline{WRITE} or \overline{CAS}) to make its negative transition is the strobe for the Data In (D_{IN}) register. This permits several options in the write cycle timing. In a write cycle, if the \overline{WRITE} input is brought low (active) prior to \overline{CAS} , the D_{IN} is strobed by \overline{CAS} and the set-up and hold times are referenced to \overline{CAS} . If the input data is not available at \overline{CAS} time or if it is desired that the cycle be a read-write cycle, the \overline{WRITE} signal will be delayed until after \overline{CAS} has made its negative transition. In this "delayed write cycle" the data input set-up and hold times are referenced to the negative edge of \overline{WRITE} rather than \overline{CAS} . (To illustrate this feature, D_{IN} is referenced to \overline{WRITE} in the timing diagrams depicting the read-write and nibble mode write cycles while the "early write" cycle diagram shows D_{IN} referenced to \overline{CAS}).

Data is retrieved from the memory in a read cycle by maintaining \overline{WRITE} in the inactive or high state throughout the portion of the memory cycle in which \overline{CAS} is active (low). Data read from the selected cell will be available at the output within the specified access time.

DATA OUTPUT CONTROL

The normal condition of the Data Output (D_{OUT}) of the TMM411000C is the high impedance (open circuit) state. This is to say, anytime \overline{CAS} is at a high level, the D_{OUT} pin will be floating. The only time the output will turn on and contain either a logic 0 or logic 1 is at access time during a read cycle. D_{OUT} will remain valid from access time until \overline{CAS} is taken back to the inactive (high level) condition.

PAGE MODE

The "Page-Mode" feature of the TMM411000C allows for successive memory operations at multiple column locations of the same row address with increased speed without an increase in power. This is done by strobing the row address into the chip and maintaining the \overline{RAS} signal at a logic 0 throughout all successive memory cycles in which the row address is common. This "Page Mode" of operation will not dissipate the power associated with the negative going edge of \overline{RAS} . Also, the time required for strobing in a new row address is eliminated, thereby decreasing the access and cycle times.

\overline{RAS} ONLY REFRESH

Refresh of the dynamic cell matrix is accomplished by performing a memory cycle at each of the 512 row address ($A_0 \sim A_8$) within each 8 millisecond time interval. Although any normal memory cycle will perform the refresh operation, this function is most easily accomplished with " \overline{RAS} -only" cycles. \overline{RAS} only refresh results in a substantial reduction in operating power. This reduction in power is reflected in the I_{CC3} specification.

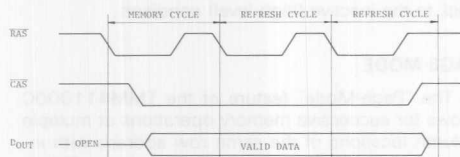
\overline{CAS} BEFORE \overline{RAS} REFRESH

\overline{CAS} before \overline{RAS} refreshing available on the TMM411000C offers an alternate refresh method. If \overline{CAS} is held on low for the specified period (t_{CSR}) before \overline{RAS} goes to low, on chip refresh control clock generators and the refresh address counter are enabled, and an internal refresh operation takes place. After the refresh operation is performed, the refresh address counter is automatically incremented in preparation for the next \overline{CAS} before \overline{RAS} refresh operation.

TMM411000C-10 TMM411000C-12

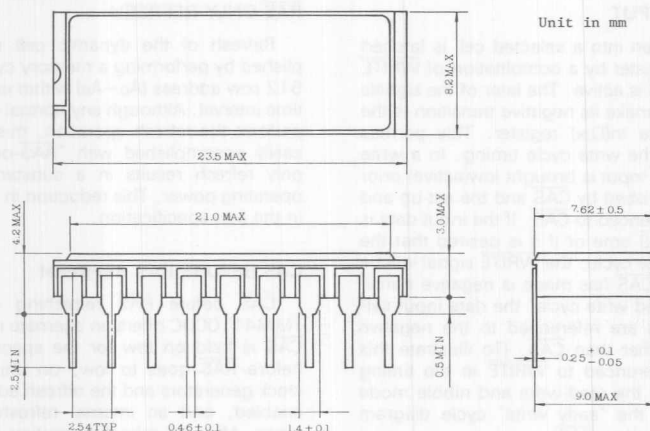
HIDDEN REFRESH

An optional feature of the TMM411000C is that refresh cycles may be performed while maintaining valid data at the output pin. This is referred to as Hidden Refresh. Hidden Refresh is performed by holding CAS at V_{IL} and taking RAS high and after a specified precharge period (t_{RP}), executing a CAS before RAS refresh cycle. (see Figure below)



This feature allows a refresh cycle to be "hidden" among data cycles without affecting the data availability.

OUTLINE DRAWINGS



NOTE : Each lead pitch is 2.54mm. All leads are located within 0.25mm of their true longitudinal position with respect to No. 1 and No. 18 leads. All dimensions are in millimeters.

Note : Toshiba does not assume any responsibility for use of any circuitry described; no circuit patent licenses are implied, and Toshiba reserves the right, at any time without notice, to change said circuitry.

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CAS BEFORE RAS REFRESH COUNTER TEST

The internal refresh operation of TMM411000C can be tested by CAS BEFORE RAS REFRESH COUNTER TEST. This cycle performs READ/WRITE operation taking the internal counter address as row address and the input address as column address.

The test is performed after a minimum of 8 CAS before RAS cycles as initialization cycles. The test procedure is as follows.

- ① Write "0" into all the memory cells at normal write mode.
- ② Select one certain column address and read "0" out and write "1" in each cell by performing CAS BEFORE RAS REFRESH COUNTER TEST (READ-WRITE CYCLE). Repeat this operation 512 times.
- ③ Check "1" out of 512 bits at normal read mode, which was written at ②.
- ④ Using the same column as ②, read "1" out and write "0" in each cell performing CAS BEFORE RAS REFRESH COUNTER TEST. Repeat this operation 512 times.
- ⑤ Check "0" out of 512 bits at normal read mode, which was written at ④.
- ⑥ Perform the above ① to ⑤ the complement data.

TOSHIBA MOS MEMORY PRODUCTS

1,048,576 WORD × 1 BIT DYNAMIC RAM
SILICON MONOLITHIC
N-CHANNEL SILICON GATE MOS

TMM411001C-10
TMM411001C-12

PRELIMINARY

DESCRIPTION

The TMM411001C is the new generation dynamic RAM organized 1,048,576 words by 1 bit, it is successor to the industry standard TMM41257P. The TMM411001C utilizes TOSHIBA's N-channel Silicon gate process technology as well as advanced circuit techniques to provide wide operating margins, both internally and to the system user. Multiplexed address inputs permit the TMM411001C to be packaged in a standard 18 pin ceramic DIP. This package size provides high system

bit densities and is compatible with widely available automated testing and insertion equipment. System oriented features include single power supply of $5V \pm 10\%$ tolerance, direct interfacing capability with high performance logic families such as Schottky TTL. In addition to the RAS only refresh mode, a CAS before RAS automatic refresh is available. Another special feature of TMM411001C is nibble mode, allowing the user to serially access 4 bits of data at a high data rate.

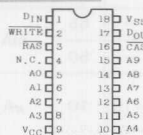
FEATURES

- 1,048,576 words by 1 bit organization
- Fast access time and cycle time

| | TMM411001C-10 | TMM411001C-12 |
|----------------------------|---------------|---------------|
| RAS Access Time | 100ns | 120ns |
| CAS Access Time | 50ns | 60ns |
| Cycle Time | 190ns | 220ns |
| Nibble Mode Access Time | 20ns | 25ns |
| Nibble Mode Cycle Time | 40ns | 50ns |

- Single power supply of $5V \pm 10\%$ with a built-in V_{BB} generator

PIN CONNECTION (TOP VIEW)

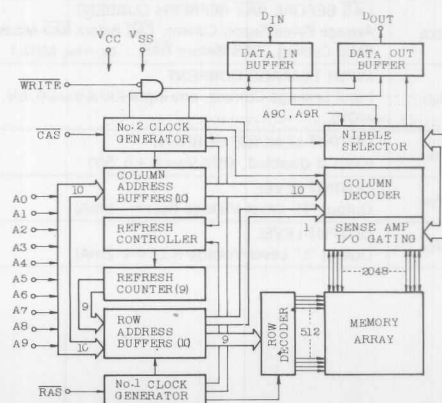


PIN NAMES

| | |
|----------------|-----------------------|
| $A_0 \sim A_9$ | Address Inputs |
| CAS | Column Address Strobe |
| DIN | Data In |
| DOUT | Data Out |
| RAS | Row Address Strobe |
| WRITE | Read/Write Input |
| Vcc | Power (+5V) |
| Vss | Ground |
| N. C. | No Connection |

- Low Power :
385mW Operating(MAX.) (TMM411001C-10)
330mW Operating(MAX.) (TMM411001C-12)
22mW Standby(MAX.).
- Industry standard 18 pin ceramic DIP
- Output unlatched at cycle end allows two-dimensional chip selection
- Common I/O capability using "EARLY WRITE" operation
- Read-Modify-Write, CAS before RAS refresh, RAS-only refresh, Hidden refresh, and Nibble Mode capability
- All inputs and output TTL compatible
- 512 refresh cycles/8ms

BLOCK DIAGRAM



TMM411001C-10

TMM411001C-12

ABSOLUTE MAXIMUM RATINGS

| ITEM | SYMBOL | RATING | UNITS | NOTES |
|------------------------------|-------------------|---------|--------|-------|
| Input and Output Voltage | V_{IN}, V_{OUT} | -1~7 | V | 1 |
| Power Supply Voltage | V_{CC} | -1~7 | V | 1 |
| Operating Temperature | T_{OPR} | 0~70 | °C | 1 |
| Storage Temperature | T_{STG} | -55~150 | °C | 1 |
| Soldering Temperature·Time | T_{SOLDER} | 260·10 | °C·sec | 1 |
| Power Dissipation | P_D | 1 | W | 1 |
| Short Circuit Output Current | I_{OUT} | 50 | mA | 1 |

RECOMMENDED DC OPERATING CONDITIONS (Ta=0~70°C)

| SYMBOL | PARAMETER | MIN. | TYP. | MAX. | UNIT | NOTES |
|----------|--------------------|------|------|------|------|-------|
| V_{CC} | Supply Voltage | 4.5 | 5.0 | 5.5 | V | 2 |
| V_{IH} | Input High Voltage | 2.4 | — | 6.5 | V | 2 |
| V_{IL} | Input Low Voltage | -1.0 | — | 0.8 | V | 2 |

DC ELECTRICAL CHARACTERISTICS (Vcc=5V±10%, Ta=0~70°C)

| SYMBOL | PARAMETER | MIN. | MAX. | UNITS | NOTES |
|-------------|---|---------------|------|---------|-------|
| I_{CC1} | OPERATING CURRENT Average Power Supply Operating Current (RAS, CAS Cycling : $t_{RC}=t_{RC}$ MIN.) | TMM411001C-10 | — 70 | mA | 3, 4 |
| | | TMM411001C-12 | — 60 | | |
| I_{CC2} | STANDBY CURRENT Power Supply Standby Current (RAS=CAS= V_{IH}) | — | 4 | mA | |
| I_{CC3} | RAS ONLY REFRESH CURRENT Average Power Supply Current, RAS Only Mode (RAS Cycling, $\overline{CAS}=V_{IH}$: $t_{RC}=t_{RC}$ MIN.) | TMM411001C-10 | — 55 | mA | 3 |
| | | TMM411001C-12 | — 50 | | |
| I_{CC4} | NIBBLE MODE CURRENT Average Power Supply Current, Nibble Mode (RAS= V_{IL} , \overline{CAS} Cycling : $t_{RC}=t_{RC}$ MIN.) | TMM411001C-10 | — 55 | mA | 3, 4 |
| | | TMM411001C-12 | — 50 | | |
| I_{CC5} | CAS BEFORE RAS REFRESH CURRENT Average Power Supply Current, \overline{CAS} Before RAS Mode (RAS Cycling, \overline{CAS} Before RAS : $t_{RC}=t_{RC}$ MIN.) | TMM411001C-10 | — 55 | mA | 3 |
| | | TMM411001C-12 | — 50 | | |
| $I_{IL(L)}$ | INPUT LEAKAGE CURRENT Input Leakage Current, any input ($0V \leq V_{IN} \leq 6.5V$, All Other Pins Not Under Test = 0V) | -10 | 10 | μA | |
| $I_{OL(L)}$ | OUTPUT LEAKAGE CURRENT (D_{OUT} is disabled, $0V \leq V_{OUT} \leq +5.5V$) | -10 | 10 | μA | |
| V_{OH} | OUTPUT LEVEL Output "H" Level Voltage ($I_{OUT} = -5mA$) | 2.4 | — | V | |
| V_{OL} | OUTPUT LEVEL Output "L" Level Voltage ($I_{OUT} = 4.2mA$) | — | 0.4 | V | |

TMM411001C-10

TMM411001C-12

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

(V_{CC}=5V±10%, T_a=0~70°C) (Notes 5, 6, 7)

| SYMBOL | PARAMETER | TMM411001C-10 | | TMM411001C-12 | | UNITS | NOTES |
|--------------------|--|---------------|--------|---------------|--------|-------|-------|
| | | MIN. | MAX. | MIN. | MAX. | | |
| t _{RC} | Random Read or Write Cycle Time | 190 | — | 220 | — | ns | |
| t _{RWC} | Read-Write Cycle Time | 210 | — | 240 | — | ns | |
| t _{RMW} | Read-Modify-Write Cycle Time | 225 | — | 260 | — | ns | |
| t _{RAC} | Access Time from RAS | — | 100 | — | 120 | ns | 8, 10 |
| t _{CAC} | Access Time from CAS | — | 50 | — | 60 | ns | 9, 10 |
| t _{OFF} | Output Buffer Turn-Off Delay | 5 | 30 | 5 | 35 | ns | 11 |
| t _t | Transition Time (Rise and Fall) | 3 | 50 | 3 | 50 | ns | 7 |
| t _{RP} | RAS Precharge Time | 80 | — | 90 | — | ns | |
| t _{RAS} | RAS Pulse Width | 100 | 10,000 | 120 | 10,000 | ns | |
| t _{RSH} | RAS Hold Time | 50 | — | 60 | — | ns | |
| t _{CSH} | CAS Hold Time | 100 | — | 120 | — | ns | |
| t _{CAS} | CAS Pulse Width | 50 | 10,000 | 60 | 10,000 | ns | |
| t _{RCO} | RAS to CAS Delay Time | 20 | 50 | 25 | 60 | ns | 13 |
| t _{CRP} | CAS to RAS Precharge Time | 10 | — | 10 | — | ns | |
| t _{CPN} | CAS Precharge Time | 20 | — | 25 | — | ns | |
| t _{ASR} | Row Address Set-Up Time | 0 | — | 0 | — | ns | |
| t _{RAH} | Row Address Hold Time | 10 | — | 15 | — | ns | |
| t _{ASC} | Column Address Set-Up Time | 0 | — | 0 | — | ns | |
| t _{CAH} | Column Address Hold Time | 20 | — | 25 | — | ns | |
| t _{AR} | Column Address Hold Time Reference to RAS | 70 | — | 85 | — | ns | |
| t _{RCS} | Read Command Set-Up Time | 0 | — | 0 | — | ns | |
| t _{RCH} | Read Command Hold Time Reference to CAS | 0 | — | 0 | — | ns | 12 |
| t _{RRH} | Read Command Hold Time Reference to RAS | 10 | — | 15 | — | ns | 12 |
| t _{WCH} | Write Command Hold Time | 20 | — | 25 | — | ns | |
| t _{WCR} | Write Command Hold Time Reference to RAS | 70 | — | 85 | — | ns | |
| t _{WP} | Write Command Pulse Width | 20 | — | 25 | — | ns | |
| t _{RWL} | Write Command to RAS Lead Time | 30 | — | 35 | — | ns | |
| t _{CWL} | Write Command to CAS Lead Time | 30 | — | 35 | — | ns | |
| t _{DS} | Data-In Set-Up Time | 0 | — | 0 | — | ns | 14 |
| t _{DH} | Data-In Hold Time | 20 | — | 25 | — | ns | 14 |
| t _{DHR} | Data-In Hold Time Reference to RAS | 70 | — | 85 | — | ns | |
| t _{REF} | Refresh Period | — | 8 | — | 8 | ms | |
| t _{WCS} | Write Command Set-Up Time | —5 | — | —5 | — | ns | 15 |
| t _{CWD} | CAS to WRITE Delay | 35 | — | 40 | — | ns | 15 |
| t _{RWD} | RAS to WRITE Delay | 85 | — | 100 | — | ns | 15 |
| t _{CSR} | CAS Set-Up Time (CAS before RAS) | 10 | — | 10 | — | ns | |
| t _{CHR} | CAS Hold Time (CAS before RAS) | 30 | — | 30 | — | ns | |
| t _{RPC} | RAS Precharge to CAS Active Time | 0 | — | 0 | — | ns | |
| t _{CPT} | CAS Precharge Time (CAS before RAS Counter Test) | 40 | — | 50 | — | ns | |
| t _{NC} | Nibble Mode Cycle Time | 40 | — | 50 | — | ns | |
| t _{NCAC} | Nibble Mode Access Time | — | 20 | — | 25 | ns | 10 |
| t _{NCAS} | Nibble Mode Pulse Width | 20 | — | 25 | — | ns | |
| t _{NCP} | Nibble Mode CAS Precharge Time | 10 | — | 15 | — | ns | |
| t _{NRRSH} | Nibble Mode RAS Hold Time (Read) | 20 | — | 25 | — | ns | |
| t _{NWRSH} | Nibble Mode RAS Hold Time (Write) | 40 | — | 45 | — | ns | |
| t _{NCWD} | Nibble Mode CAS to WRITE Delay Time | 20 | — | 25 | — | ns | |
| t _{NCWL} | Nibble Mode WRITE Command to CAS Read Time | 20 | — | 25 | — | ns | |

TMM411001C-10

TMM411001C-12

CAPACITANCE (V_{CC}=5V±10%, f=1MHz, T_a=0~70°C)

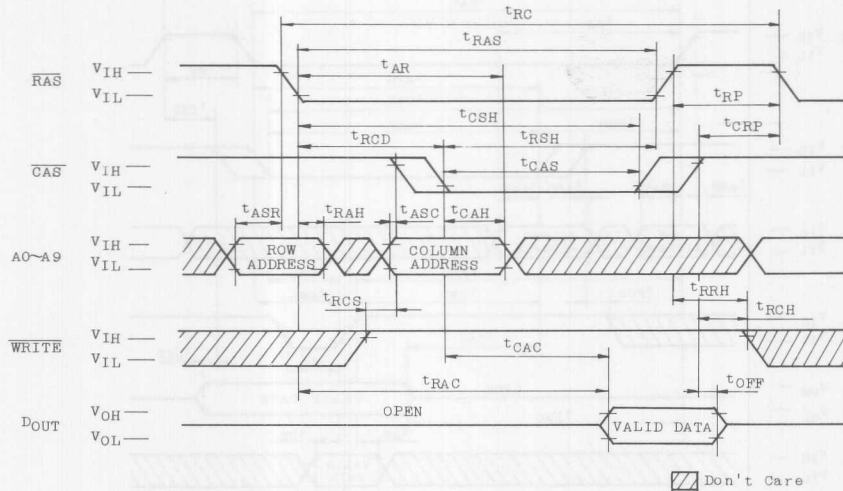
| SYMBOL | PARAMETER | MIN. | MAX. | UNIT |
|-----------------|---|------|------|------|
| C _{I1} | Input Capacitance (A ₀ ~A ₉ , D _{IN}) | — | 6 | pF |
| C _{I2} | Input Capacitance (RAS, CAS, WRITE) | — | 7 | pF |
| C _O | Output Capacitance (D _{OUT}) | — | 7 | pF |

NOTES :

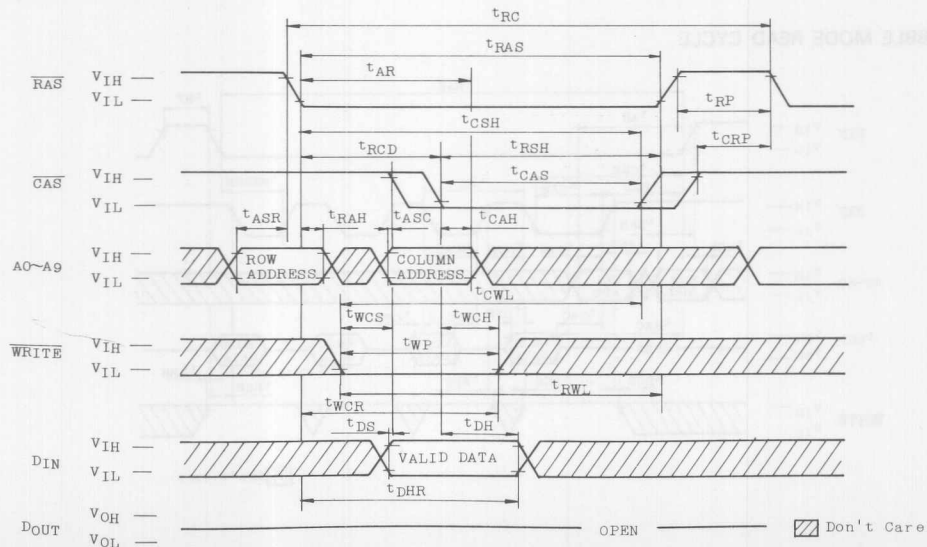
1. Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device.
2. All voltages are referenced to V_{SS}.
3. I_{CC1}, I_{CC3}, I_{CC4}, I_{CC5} depend on cycle rate.
4. I_{CC1}, I_{CC4} depend on output loading. Specified values are obtained with the output open.
5. An initial pause of 200μs is required after power-up followed by any 8 RAS cycles before proper device operation is achieved. In case of using internal refresh counter, a minimum of 8 CAS Before RAS initialization cycles instead of 8 RAS cycles are required.
6. AC measurements assume t_r=5ns.
7. V_{IH}(min.) and V_{IL}(max.) are reference levels for measuring timing of input signals. Also, transition times are measured between V_{IH} and V_{IL}.
8. Assumes that t_{RCD} ≤ t_{RCD}(max.). If t_{RCD} is greater than the maximum recommended value shown in this table, t_{RAC} will increase by the amount that t_{RCD} exceeds the value shown.
9. Assumes that t_{RCD} ≥ t_{RCD}(max.).
10. Measured with a load equivalent to 2 TTL loads and 100pF.
11. t_{OFF}(max.) defines the time at which the output achieves the open circuit condition and is not referenced to output voltage levels.
12. Either t_{RCH} or t_{RRH} must be satisfied for a read cycle.
13. Operation within the t_{RCD}(max.) limit insures that t_{RAC}(max.) can be met. t_{RCD}(max.) is specified as a reference point only : If t_{RCD} is greater than the specified t_{RCD}(max.) limit, then access time is controlled exclusively by t_{CAC}.
14. These parameters are referenced to CAS leading edge in early write cycles and to WRITE leading edge in read-write or read-modify-write cycles.
15. t_{WCS}, t_{WVD} and t_{WWD} are not restrictive operating parameters. They are included in the data sheet as electrical characteristics only. If t_{WCS} ≥ t_{WCS}(min.), the cycle is an early write cycle and the data out pin will remain open circuit (high impedance) throughout the entire cycle ; If t_{WVD} ≥ t_{WVD}(min.) and t_{WWD} ≥ t_{WWD}(min.), the cycle is a read-write cycle or read-modify-write cycle and the data out will contain data read from the selected cell : If neither of the above sets of conditions is satisfied, the condition of the data out (at access time) is indeterminate.

TIMING WAVEFORMS

• READ CYCLE

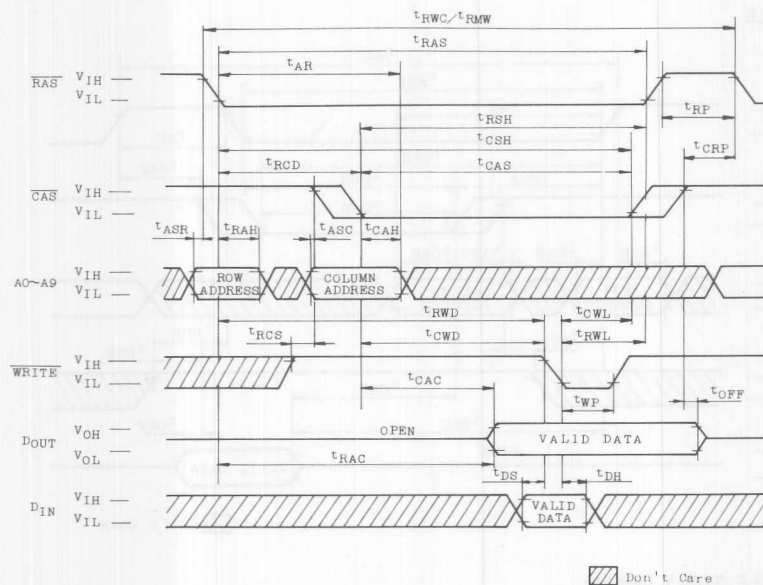


• WRITE CYCLE (EARLY WRITE)

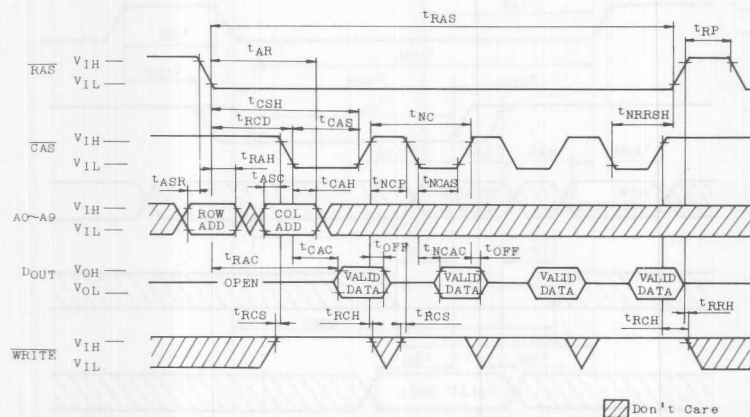


TMM411001C-10 TMM411001C-12

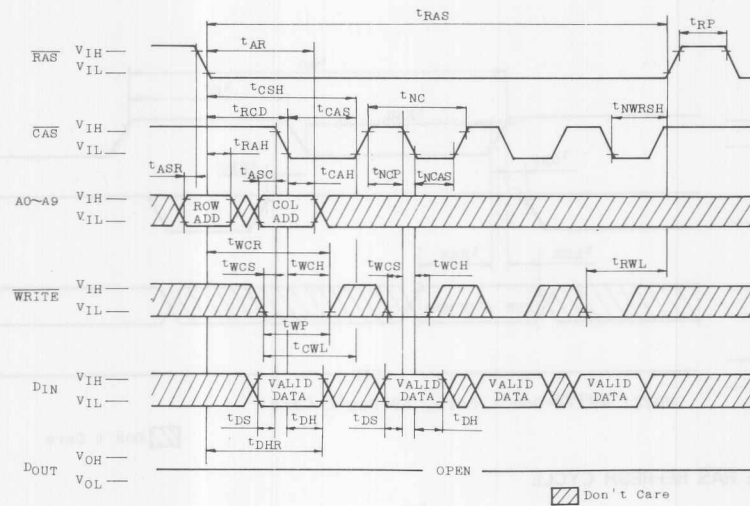
● READ-WRITE/READ-MODIFY-WRITE CYCLE



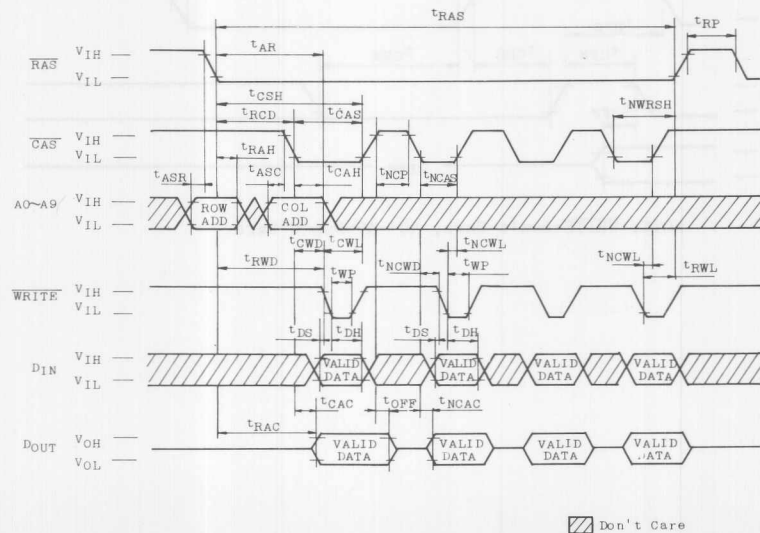
● NIBBLE MODE READ CYCLE



● NIBBLE MODE WRITE CYCLE



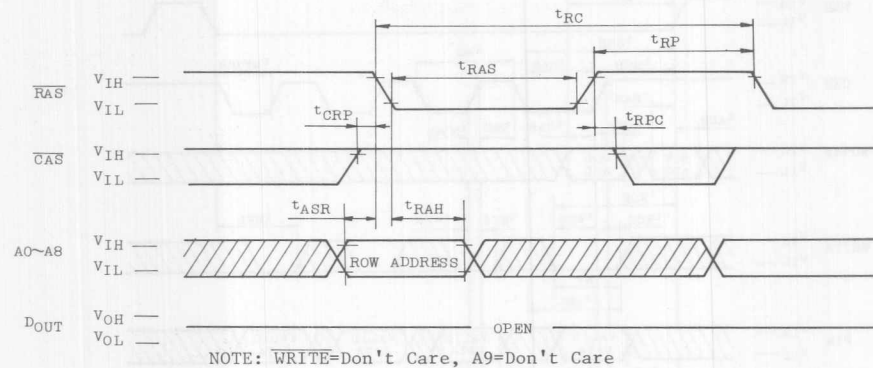
● NIBBLE MODE READ-WRITE/READ-MODIFY-WRITE CYCLE



TMM411001C-10

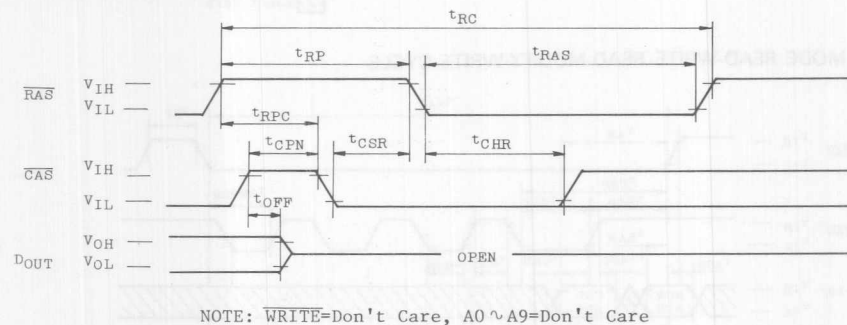
TMM411001C-12

● $\overline{\text{RAS}}$ ONLY REFRESH CYCLE

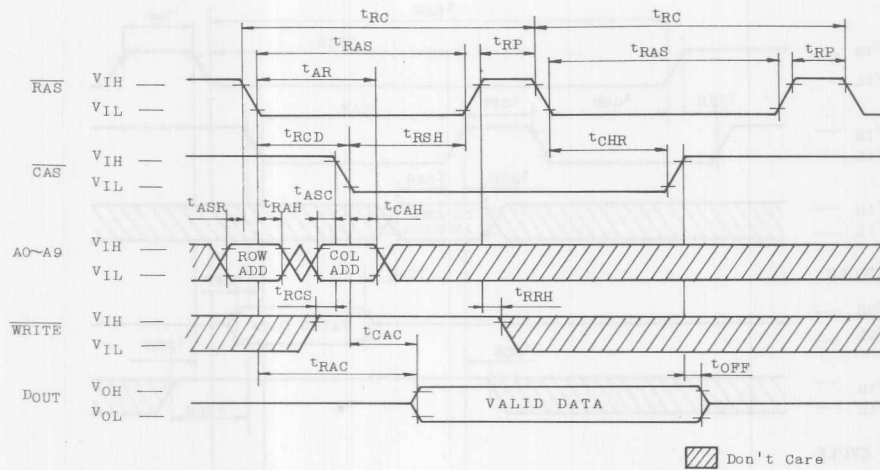


Don't Care

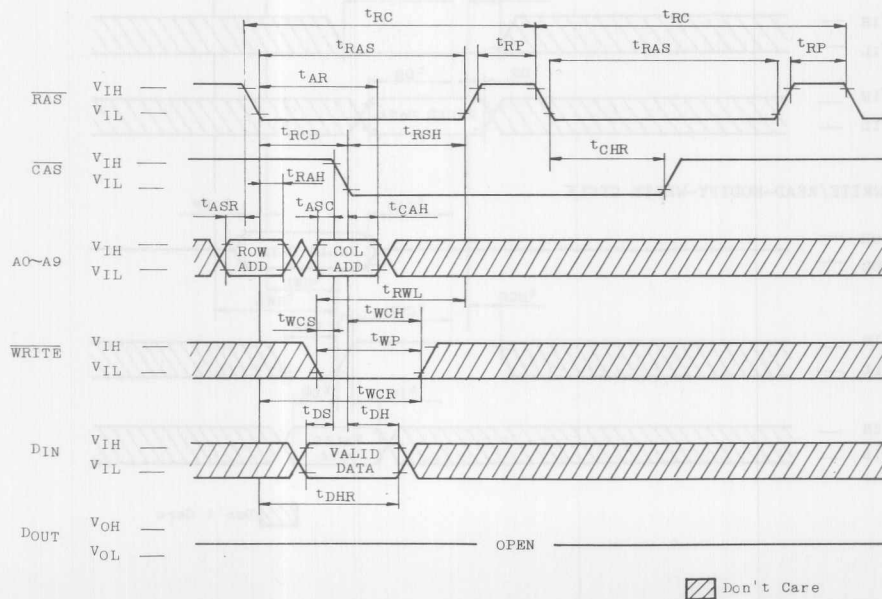
● $\overline{\text{CAS}}$ BEFORE $\overline{\text{RAS}}$ REFRESH CYCLE



● HIDDEN REFRESH CYCLE (READ)



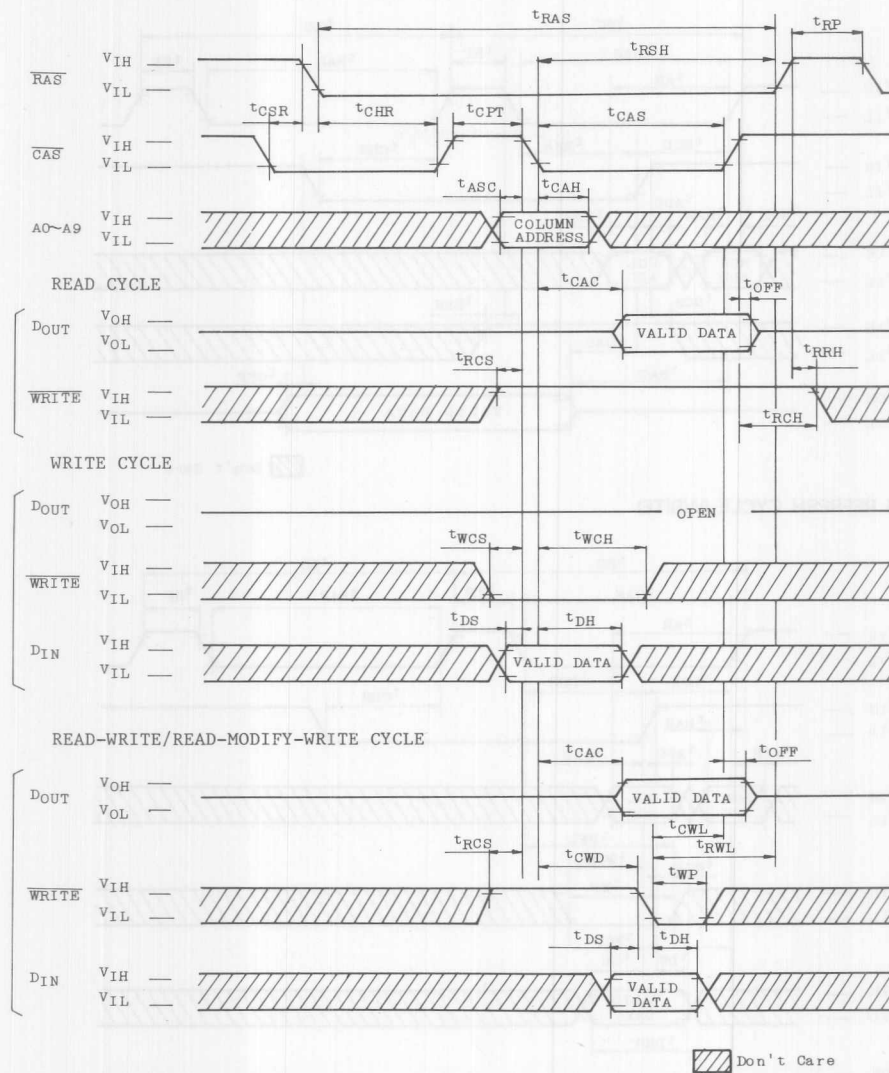
● HIDDEN REFRESH CYCLE (WRITE)



TMM411001C-10

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● $\overline{\text{CAS}}$ BEFORE $\overline{\text{RAS}}$ REFRESH COUNTER TEST CYCLE



APPLICATION INFORMATION

ADDRESSING

The 20 address bits required to decode 1 of the 1,048,576 cell locations within the TMM411001C are multiplexed onto the 10 address inputs and latched into the onchip address latches by externally applying two negative going TLL-level clocks.

The first clock, the Row Address Strobe ($\overline{\text{RAS}}$), latches the 10 row address bits into the chip. The second clock, the Column Address Strobe ($\overline{\text{CAS}}$), subsequently latches the 10 column address bits into the chip. Each of these signals, $\overline{\text{RAS}}$, and $\overline{\text{CAS}}$, triggers a sequence of events which are controlled by different delayed internal clocks.

The two clock chains are linked together logically in such a way that the address multiplexing operation is done outside of the critical path timing sequence for read data access. The later events in the $\overline{\text{CAS}}$ clock sequence are inhibited until the occurrence of a delayed signal derived from the $\overline{\text{RAS}}$ clock chain. This "gated $\overline{\text{CAS}}$ " feature allows the $\overline{\text{CAS}}$ clock to be externally activated as soon as the Row address Hold Time specification (trah) has been satisfied and the address inputs have been changed from Row address to Column address information.

DATA INPUT/OUTPUT

Data to be written into a selected cell is latched into an on-chip register by a combination of $\overline{\text{WRITE}}$ and $\overline{\text{CAS}}$ while $\overline{\text{RAS}}$ is active. The later of the signals ($\overline{\text{WRITE}}$ or $\overline{\text{CAS}}$) to make its negative transition is the strobe for the Data In (D_{IN}) register. This permits several options in the write cycle timing. In a write cycle, if the $\overline{\text{WRITE}}$ input is brought low (active) prior to $\overline{\text{CAS}}$, the D_{IN} is strobed by $\overline{\text{CAS}}$ and the set-up and hold times are referenced to $\overline{\text{CAS}}$. If the input data is not available at $\overline{\text{CAS}}$ time or if it is desired that the cycle be a read-write cycle, the $\overline{\text{WRITE}}$ signal will be delayed until after $\overline{\text{CAS}}$ has made its negative transition. In this "delayed write cycle" the data input set-up and hold times are referenced to the negative edge of $\overline{\text{WRITE}}$ rather than $\overline{\text{CAS}}$. (To illustrate this feature, D_{IN} is referenced to $\overline{\text{WRITE}}$ in the timing diagrams depicting the read-write and nibble mode write cycles while the "early write" cycle diagram shows D_{IN} referenced to $\overline{\text{CAS}}$).

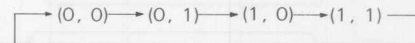
Data is retrieved from the memory in a read cycle by maintaining $\overline{\text{WRITE}}$ in the inactive or high state throughout the portion of the memory cycle in which $\overline{\text{CAS}}$ is active (low). Data read from the selected cell will be available at the output within the specified access time.

DATA OUTPUT CONTROL

The normal condition of the Data Output (D_{out}) of the TMM411001C is the high impedance (open circuit) state. This is to say, anytime $\overline{\text{CAS}}$ is at a high level, the D_{out} pin will be floating. The only time the output will turn on and contain either a logic 0 or logic 1 is at access time during a read cycle. D_{out} will remain valid from access time until $\overline{\text{CAS}}$ is taken back to the inactive (high level) condition.

NIBBLE MODE

Nibble mode operation allows faster successive data operation on 4 bits. The first of 4 bits is accessed in the usual manner with read data coming out at tcac time. By keeping $\overline{\text{RAS}}$ low, $\overline{\text{CAS}}$ can be cycled up and then down, to read or write the next three pages at high data rate (faster than tcac). Row and column addresses need only be supplied for the first access of the cycles. From then on, the falling edge of $\overline{\text{CAS}}$ will activate the next bit. After four bits have been accessed, the next bit will be the same as the first bit accessed (wrap-around method).



Pin one (A_9) determines the starting point of the circular 4 bits nibble. Row A_9 and column A_9 provide the two binary bits needed to select one of four bits. From then on, successive bits come out in a binary fashion; $00 \rightarrow 01 \rightarrow 10 \rightarrow 11$ with A_9 row being the least significant address.

A nibble cycle can be a read, write, or late write cycle. Any combinations of reads and writes or late writes will be allowed. In addition, the circular wrap-around will continue for as long as $\overline{\text{RAS}}$ is kept low.

RAS ONLY REFRESH

Refresh of the dynamic cell matrix is accomplished by performing a memory cycle at each of the 512 row address ($\text{A}_0 \sim \text{A}_8$) within each 8 millisecond time interval. Although any normal memory cycle will perform the refresh operation, this function is most easily accomplished with "RAS-only" cycles, $\overline{\text{RAS}}$ only refresh results in a substantial reduction in operating power. This reduction in power is reflected in the Icc3 specification.

TMM411001C-10

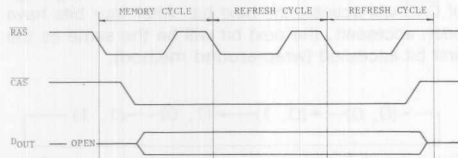
TMM411001C-12

CAS BEFORE RAS REFRESH

$\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ refreshing available on the TMM411001C offers an alternate refresh method. If $\overline{\text{CAS}}$ is held on low for the specified period (t_{CSR}) before $\overline{\text{RAS}}$ goes to low, on chip refresh control clock generators and the refresh address counter are enabled, and an internal refresh operation takes place. After the refresh operation is performed, the refresh address counter is automatically incremented in preparation for the next $\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ refresh operation.

HIDDEN REFRESH

An optional feature of the TMM411001C is that refresh cycles may be performed while maintaining valid data at the output pin. This is referred to as Hidden Refresh. Hidden Refresh is performed by holding $\overline{\text{CAS}}$ at V_{IL} and taking $\overline{\text{RAS}}$ high and after a specified precharge period (t_{RP}), executing a $\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ refresh cycle. (see Figure below)



This feature allows a refresh cycle to be "hidden" among data cycles without affecting the data availability.

CAS BEFORE RAS REFRESH COUNTER TEST

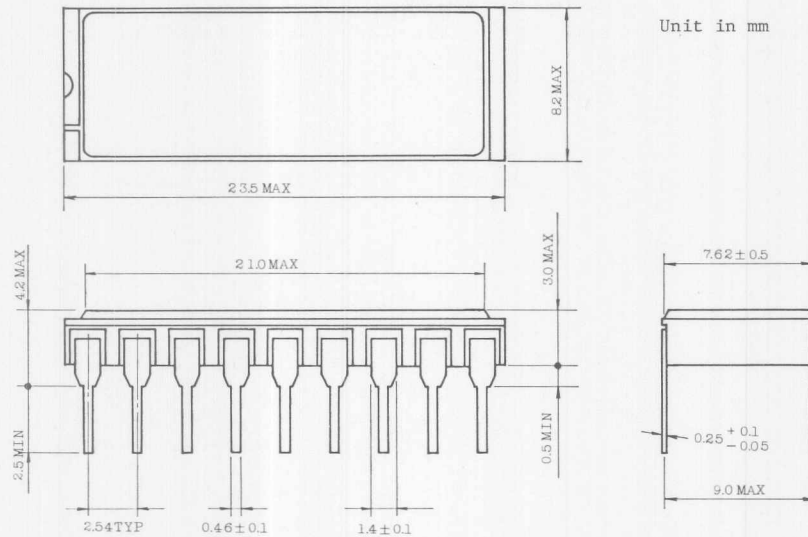
The internal refresh operation of TMM411001C can be tested by $\overline{\text{CAS}}$ BEFORE $\overline{\text{RAS}}$ REFRESH COUNTER TEST. This cycle performs READ/WRITE operation taking the internal counter address as row address and the input address as column address.

The test is performed after a minimum of 8 $\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ cycles as initialization cycles. The test procedure is as follows.

- ① Write "0" into all the memory cells at normal write mode.
- ② Select one certain column address and read "0" out and write "1" in each cell by performing $\overline{\text{CAS}}$ BEFORE $\overline{\text{RAS}}$ REFRESH COUNTER TEST (READ-WRITE CYCLE). Repeat this operation 512 times.
- ③ Check "1" out of 512 bits at normal read mode, which was written at ②.
- ④ Using the same column as ②, read "1" out and write "0" in each cell performing $\overline{\text{CAS}}$ BEFORE $\overline{\text{RAS}}$ REFRESH COUNTER TEST. Repeat this operation 512 times.
- ⑤ Check "0" out of 512 bits at normal read mode, which was written at ④.
- ⑥ Perform the above ① to ⑤ the complement data.

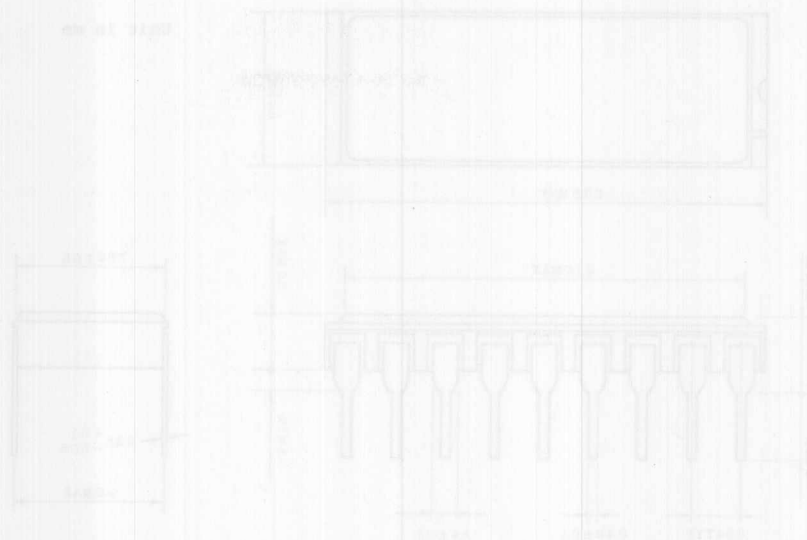
TMM411001C-10 TMM411001C-12

OUTLINE DRAWINGS



NOTE : Each lead pitch is 2.54mm. All leads are located within 0.25mm of their true longitudinal position with respect to No. 1 and No. 18 leads. All dimensions are in millimeters.

TMM411001C-10 TMM411001C-12



Note : Toshiba does not assume any responsibility for use of any circuitry described ; no circuit patent licenses are implied, and Toshiba reserves the right, at any time without notice, to change said circuitry.
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CMOS Dynamic Random Access Memories

REINHOLD A. ZSOGNA, GEORGETOWN UNIVERSITY, GEORGETOWN, G.D. 25010/60

TOSHIBA MOS MEMORY PRODUCTS

1,048,576 WORD × 1 BIT DYNAMIC RAM
SILICON GATE CMOS

TC511000C-10
TC511000C-12

PRELIMINARY

DESCRIPTION

The TC511000C is the new generation dynamic RAM organized 1,048,576 words by 1 bit. The TC511000C utilizes TOSHIBA's CMOS Silicon gate process technology as well as advanced circuit techniques to provide wide operating margins, both internally and to the system user. Multiplexed address inputs permit the TC511000C to be pack-

aged in a standard 18 pin ceramic DIP. This package size provides high system bit densities and is compatible with widely available automated testing and insertion equipment. System oriented features include single power supply of $5V \pm 10\%$ tolerance, direct interfacing capability with high performance logic families such as Schottky TTL.

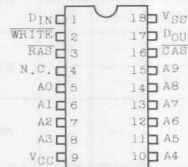
FEATURES

- 1,048,576 words by 1 bit organization
- Fast access time and cycle time

| | TC511000C-10 | TC511000C-12 |
|-------------------------------------|--------------|--------------|
| t_{RAC} RAS Access Time | 100ns | 120ns |
| t_{AA} Column Address Access Time | 55ns | 65ns |
| t_{CAC} CAS Access Time | 20ns | 25ns |
| t_{RC} Cycle Time | 190ns | 220ns |
| t_{PC} Fast Page Mode Cycle Time | 70ns | 85ns |

- Single power supply of $5V \pm 10\%$ with a built-in V_{BB} generator
- Low Power
330mW Operating (MAX.) (TC511000C-10)
275mW Operating (MAX.) (TC511000C-12)
5.5mW Standby (MAX.).
- Industry standard 18 pin ceramic DIP
- Output unlatched at cycle end allows two-dimensional chip selection
- Common I/O capability using "EARLY WRITE" operation
- Read-Modify-Write, \overline{CAS} before \overline{RAS} refresh, RAS-only refresh, Hidden refresh, and Fast Page Mode capability
- All inputs and output TTL compatible
- 512 refresh cycles/8ms

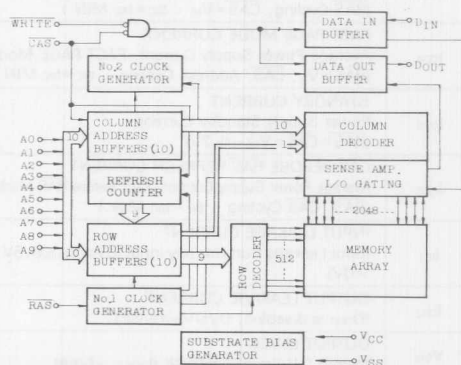
PIN CONNECTION (TOP VIEW)



PIN NAMES

| | |
|------------------|-----------------------|
| $A_0 \sim A_9$ | Address Inputs |
| RAS | Row Address Strobe |
| DIN | Data In |
| DOUT | Data Out |
| \overline{CAS} | Column Address Strobe |
| WRITE | Read/Write Input |
| V_{CC} | Power (+5V) |
| V_{SS} | Ground |
| N. C. | No Connection |

BLOCK DIAGRAM



TC511000C-10

TC511000C-12

ABSOLUTE MAXIMUM RATINGS

| ITEM | SYMBOL | RATING | UNITS | NOTES |
|------------------------------|--------------|---------------------|--------|-------|
| Input Voltage | V_{IN} | -1~7 | V | 1 |
| Output Voltage | V_{OUT} | -1 ~ $V_{CC} + 0.5$ | V | 1 |
| Power Supply Voltage | V_{CC} | -1~7 | V | 1 |
| Operating Temperature | T_{OPR} | 0~70 | °C | 1 |
| Storage Temperature | T_{STG} | -55~150 | °C | 1 |
| Soldering Temperature·Time | T_{SOLDER} | 260·10 | °C·sec | 1 |
| Power Dissipation | P_D | 1 | W | 1 |
| Short Circuit Output Current | I_{OUT} | 50 | mA | 1 |

RECOMMENDED DC OPERATING CONDITIONS (Ta=0~70°C)

| SYMBOL | PARAMETER | MIN. | TYP. | MAX. | UNIT | NOTES |
|----------|--------------------|------|------|------|------|-------|
| V_{CC} | Supply Voltage | 4.5 | 5.0 | 5.5 | V | 2 |
| V_{IH} | Input High Voltage | 2.4 | — | 6.5 | V | 2 |
| V_{IL} | Input Low Voltage | -1.0 | — | 0.8 | V | 2 |

DC ELECTRICAL CHARACTERISTICS (V_{CC}=5V±10%, Ta=0~70°C)

| SYMBOL | PARAMETER | | MIN. | MAX. | UNITS | NOTES |
|------------|---|--------------|------|------|---------|-------|
| I_{CC1} | OPERATING CURRENT Average Power Supply Operating Current (RAS, CAS, Address Cycling : $t_{RC}=t_{RC}$ MIN.) | TC511000C-10 | — | 60 | mA | 3,4 |
| | | TC511000C-12 | — | 50 | | |
| I_{CC2} | STANDBY CURRENT Power Supply Standby Current (RAS=CAS= V_{IH}) | | — | 3 | mA | |
| I_{CC3} | RAS ONLY REFRESH CURRENT Average Power Supply Current, RAS Only Mode (RAS Cycling, CAS= V_{IH} : $t_{RC}=t_{RC}$ MIN.) | TC511000C-10 | — | 50 | mA | 3 |
| | | TC511000C-12 | — | 40 | | |
| I_{CC4} | FAST PAGE MODE CURRENT Average Power Supply Current, FAST PAGE Mode (RAS= V_{IL} , CAS, Address Cycling : $t_{PC}=t_{PC}$ MIN.) | TC511000C-10 | — | 40 | mA | 3,4 |
| | | TC511000C-12 | — | 30 | | |
| I_{CC5} | STANDBY CURRENT Power Supply Standby Current, (RAS=CAS= $V_{CC}-0.2V$) | | — | 1 | mA | |
| I_{CC6} | CAS BEFORE RAS REFRESH CURRENT Average Power Supply Current, CAS Before RAS Mode (RAS, CAS Cycling : $t_{RC}=t_{RC}$ MIN.) | TC511000C-10 | — | 50 | mA | 3 |
| | | TC511000C-12 | — | 40 | | |
| $I_{I(L)}$ | INPUT LEAKAGE CURRENT Input Leakage Current, any input ($0V \leq V_{IN} \leq 6.5V$, All Other Pins Not Under Test = 0V) | | -10 | 10 | μA | |
| $I_{O(L)}$ | OUTPUT LEAKAGE CURRENT (Dout is disabled, $0V \leq V_{OUT} \leq V_{CC}$) | | -10 | 10 | μA | |
| V_{OH} | OUTPUT LEVEL Output "H" Level VOLTAGE ($I_{OUT} = -5mA$) | | 2.4 | — | V | |
| V_{OL} | OUTPUT LEVEL Output "L" Level VOLTAGE ($I_{OUT} = 4.2mA$) | | — | 0.4 | V | |

TC511000C-10

TC511000C-12

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

(V_{CC}=5V±10%, Ta=0~70°C) (Notes 5, 6, 7)

| SYMBOL | PARAMETER | TC511000C-10 | | TC511000C-12 | | UNITS | NOTES |
|------------------|--|--------------|---------|--------------|---------|-------|-------|
| | | MIN. | MAX. | MIN. | MAX. | | |
| t _{RC} | Random Read or Write Cycle Time | 190 | — | 220 | — | ns | |
| t _{RWC} | Read-Write Cycle Time | 235 | — | 270 | — | ns | |
| t _{PC} | Fast Page Mode Cycle Time | 70 | — | 85 | — | ns | |
| t _{RAC} | Access Time from RAS | — | 100 | — | 120 | ns | 8,13 |
| t _{CAC} | Access Time from CAS | — | 20 | — | 25 | ns | 8,13 |
| t _{AA} | Access Time from Column Address | — | 55 | — | 65 | ns | 8,13 |
| t _{ACP} | Access Time from $\overline{\text{CAS}}$ Precharge | — | 65 | — | 80 | ns | 8,14 |
| t _{OFF} | Output Buffer Turn-off Delay | 0 | 30 | 0 | 35 | ns | 9 |
| t _T | Transition Time(Rise and Fall) | 3 | 35 | 3 | 35 | ns | 7 |
| t _{RP} | RAS Precharge Time | 80 | — | 90 | — | ns | |
| t _{RAS} | RAS Pulse Width | 100 | 100,000 | 120 | 100,000 | ns | |
| t _{RS} | RAS Hold Time | 20 | — | 25 | — | ns | |
| t _{CS} | CAS Hold Time | 100 | — | 120 | — | ns | |
| t _{CAS} | CAS Pulse Width | 20 | — | 25 | — | ns | |
| t _{RCD} | RAS to CAS Delay Time | 25 | 50 | 25 | 60 | ns | 13 |
| t _{CRP} | CAS to RAS Precharge Time | 10 | — | 10 | — | ns | |
| t _{CP} | $\overline{\text{CAS}}$ Precharge Time | 10 | 40 | 15 | 50 | ns | 14 |
| t _{ASR} | Row Address Set-Up Time | 0 | — | 0 | — | ns | 13 |
| t _{RAH} | Row Address Hold Time | 15 | — | 15 | — | ns | |
| t _{ASC} | Column Address Set-Up Time | 0 | 30 | 0 | 35 | ns | 13 |
| t _{CAH} | Column Address Hold Time | 20 | — | 25 | — | ns | |
| t _{AR} | Column Address Hold Time referenced to $\overline{\text{RAS}}$ | 70 | — | 85 | — | ns | |
| t _{RAL} | Column Address to RAS Lead Time | 55 | — | 65 | — | ns | |
| t _{RCS} | Read Command Set-Up Time | 0 | — | 0 | — | ns | |
| t _{RCH} | Read Command Hold Time | 0 | — | 0 | — | ns | 10 |
| t _{RRH} | Read Command Hold Time referenced to RAS | 0 | — | 0 | — | ns | 10 |
| t _{WCH} | Write Command Hold Time | 20 | — | 25 | — | ns | |
| t _{WCR} | Write Command Hold Time referenced to $\overline{\text{RAS}}$ | 70 | — | 85 | — | ns | |
| t _{WP} | Write Command Pulse Width | 20 | — | 25 | — | ns | |
| t _{RWL} | Write Command to RAS Lead Time | 40 | — | 45 | — | ns | |
| t _{CWL} | Write Command to CAS Lead Time | 20 | — | 25 | — | ns | |
| t _{DS} | Data Set-Up Time | 0 | — | 0 | — | ns | 11 |
| t _{DH} | Data Hold Time | 20 | — | 25 | — | ns | 11 |
| t _{DHR} | Data Hold Time referenced to $\overline{\text{RAS}}$ | 70 | — | 85 | — | ns | |
| t _{REF} | Refresh Period | 8 | — | 8 | — | ms | |
| t _{WCS} | Write Command Set-Up Time | 0 | — | 0 | — | ns | 12 |
| t _{CWD} | CAS to WRITE Delay Time | 20 | — | 25 | — | ns | 12 |
| t _{RWD} | RAS to WRITE Delay Time | 100 | — | 120 | — | ns | 12 |
| t _{AWD} | Column Address to WRITE Delay Time | 55 | — | 65 | — | ns | 12 |
| t _{CSR} | CAS Set-Up Time(CAS before $\overline{\text{RAS}}$ Cycle) | 10 | — | 10 | — | ns | |
| t _{CHR} | CAS Hold Time(CAS before $\overline{\text{RAS}}$ cycle) | 30 | — | 30 | — | ns | |
| t _{RPC} | RAS to CAS Precharge Time | 0 | — | 0 | — | ns | |
| t _{CPT} | CAS Precharge Time(CAS before RAS Counter Test Cycle) | 50 | — | 60 | — | ns | |

TC511000C-10

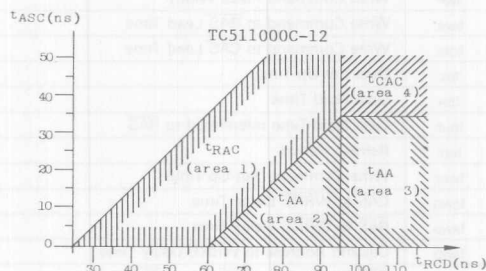
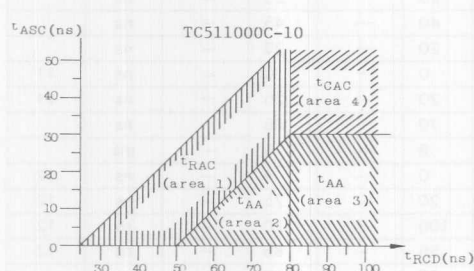
TC511000C-12

CAPACITANCE ($V_{CC}=5V \pm 10\%$, $f=1\text{MHz}$, $T_a=0 \sim 70^\circ\text{C}$)

| SYMBOL | PARAMETER | MIN. | MAX. | UNITS |
|----------|---|------|------|-------|
| C_{I1} | Input Capacitance ($A_0 \sim A_9$, D_{IN}) | — | 6 | pF |
| C_{I2} | Input Capacitance ($\overline{\text{RAS}}$, $\overline{\text{CAS}}$, $\overline{\text{WRITE}}$) | — | 7 | pF |
| C_O | Output Capacitance (D_{OUT}) | — | 7 | pF |

NOTES :

- Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device.
- All voltage are reference to V_{SS} .
- I_{CC1} , I_{CC3} , I_{CC4} , I_{CC6} , depend on cycle rate.
- I_{CC6} , I_{CC4} , depend on output loading. Specified value are obtained with the output open.
- An initial pause of $200\mu\text{s}$ is required after power-up followed by 8 $\overline{\text{RAS}}$ cycles before proper device operation is achieved. In case of using internal refresh counter, a minimum of 8 $\overline{\text{CAS}}$ Before $\overline{\text{RAS}}$ initialization cycles instead of 8 $\overline{\text{RAS}}$ cycles are required.
- AC measurements assume $t_r=5\text{ns}$.
- V_{IH} (min.) and V_{IL} (max.) are reference levels for measuring timing of input signals. Also, transition times are measured between V_{IH} and V_{IL} .
- Measured with a load equivalent to 2 TTL loads and 100pF .
- t_{OFF} (max.) defines the time at which the output achieves the open circuit condition and is not referenced to output voltage levels.
- Either t_{RCH} or t_{RRH} must be satisfied for a read cycle.
- These parameters are referenced to $\overline{\text{CAS}}$ leading edge in early write cycles and to $\overline{\text{WRITE}}$ leading edge in read-write or read-modify-write cycles.
- t_{WCS} , t_{RWD} , t_{CWD} and t_{AWD} are not restrictive operating parameters. They are included the data sheet as electrical characteristics only. If $t_{WCS} \geq t_{WCS}(\text{min.})$, the cycle is an early write cycle and data out pin will remain open circuit (high impedance) through the entire cycle ; If $t_{RWD} \geq t_{RWD}(\text{min.})$, $t_{CWD} \geq t_{CWD}(\text{min.})$ and $t_{AWD} \geq t_{AWD}(\text{min.})$, the cycle is a read-write or read-modify-write cycle and data out will contain data read from the selected cell : If neither of the above sets of conditions is satisfied, the condition of the data out(at access time) is indeterminate.
- Operation within $t_{RCD}(\text{max.})$ and $t_{ASC}(\text{max.})$ limit insure that t_{RAC} , t_{CAC} , t_{AA} can be met.
 $t_{RCD}(\text{max.})$ and $t_{ASC}(\text{max.})$ are specified as the reference points only.
 $[t_{RCD}(\text{max.}) + t_{ASC}(\text{max.})] \geq t_{RCD}$ and $[t_{RCD} - t_{ASC}] \leq t_{RCD}(\text{max.})$ t_{RAC} (area 1)
 $[t_{RCD}(\text{max.}) + t_{ASC}(\text{max.})] \geq t_{RCD}$ and $[t_{RCD} - t_{ASC}] \leq t_{RCD}(\text{max.})$ t_{AA} (area 2)
 $[t_{RCD}(\text{max.}) + t_{ASC}(\text{max.})] \leq t_{RCD}$ and $t_{ASC} \leq t_{ASC}(\text{max.})$ t_{AA} (area 3)
 $[t_{RCD}(\text{max.}) + t_{ASC}(\text{max.})] \leq t_{RCD}$ and $t_{ASC} \geq t_{ASC}(\text{max.})$ t_{CAC} (area 4)



14. Operation within $t_{CP}(\max.)$ limit insure that t_{ACP} , t_{CAC} , t_{AA} can be met in Fast Page Mode Read Cycle.

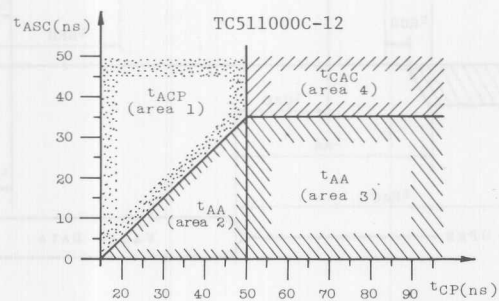
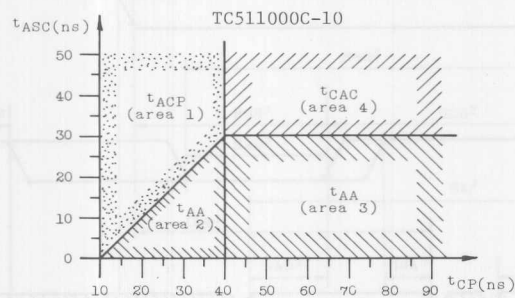
$t_{CP}(\max.)$ is specified as a reference point only.

$t_{CP} \leq t_{CP}(\max.)$ and $t_{ASC} \geq [t_{CP} - t_{CP}(\min.)]$ t_{ACP} (area 1)

$t_{CP} \leq t_{CP}(\max.)$ and $t_{ASC} \leq [t_{CP} - t_{CP}(\min.)]$ t_{AA} (area 2)

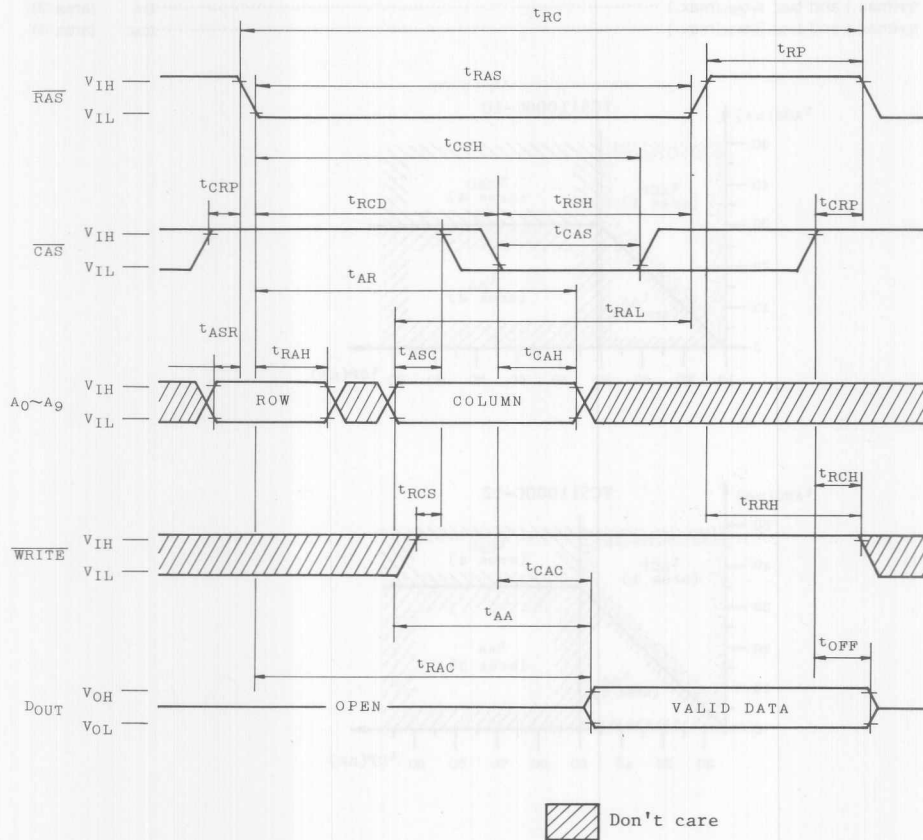
$t_{CP} \geq t_{CP}(\max.)$ and $t_{ASC} \leq t_{ASC}(\max.)$ t_{AA} (area 3)

$t_{CP} \geq t_{CP}(\max.)$ and $t_{ASC} \geq t_{ASC}(\max.)$ t_{CAC} (area 4)

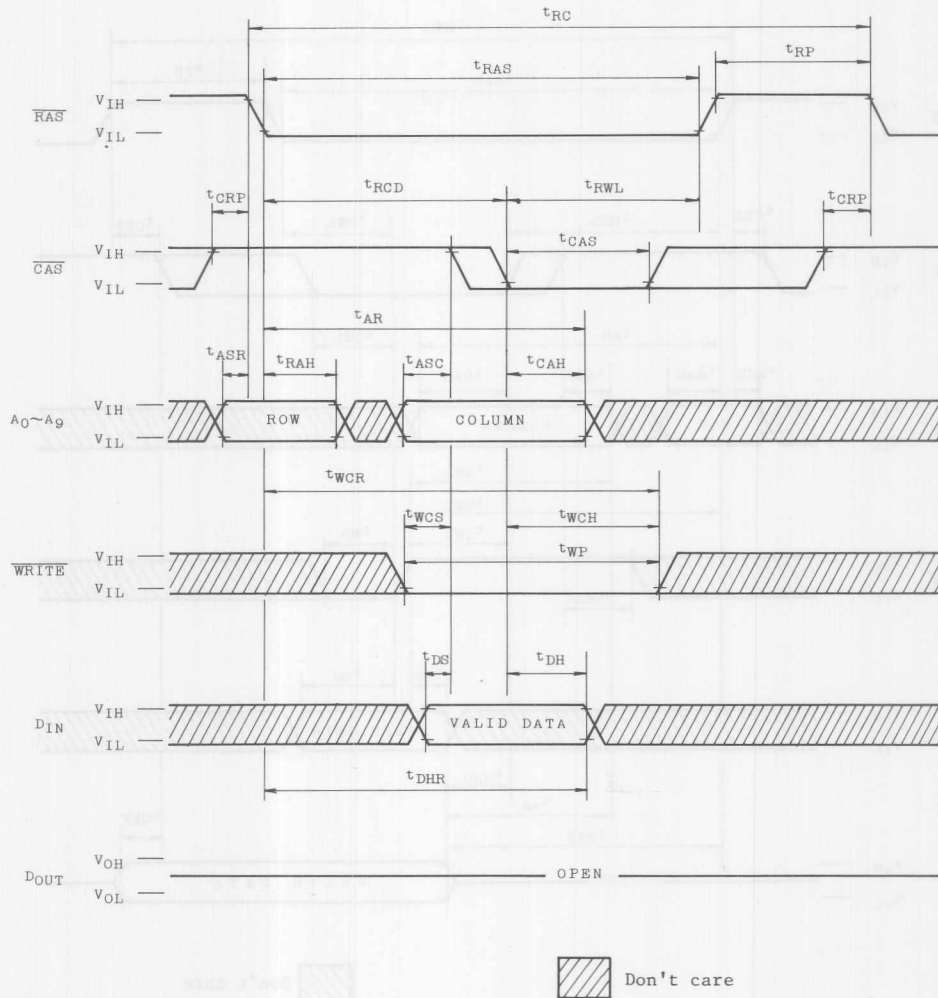


TC511000C-10 TC511000C-12

● READ CYCLE



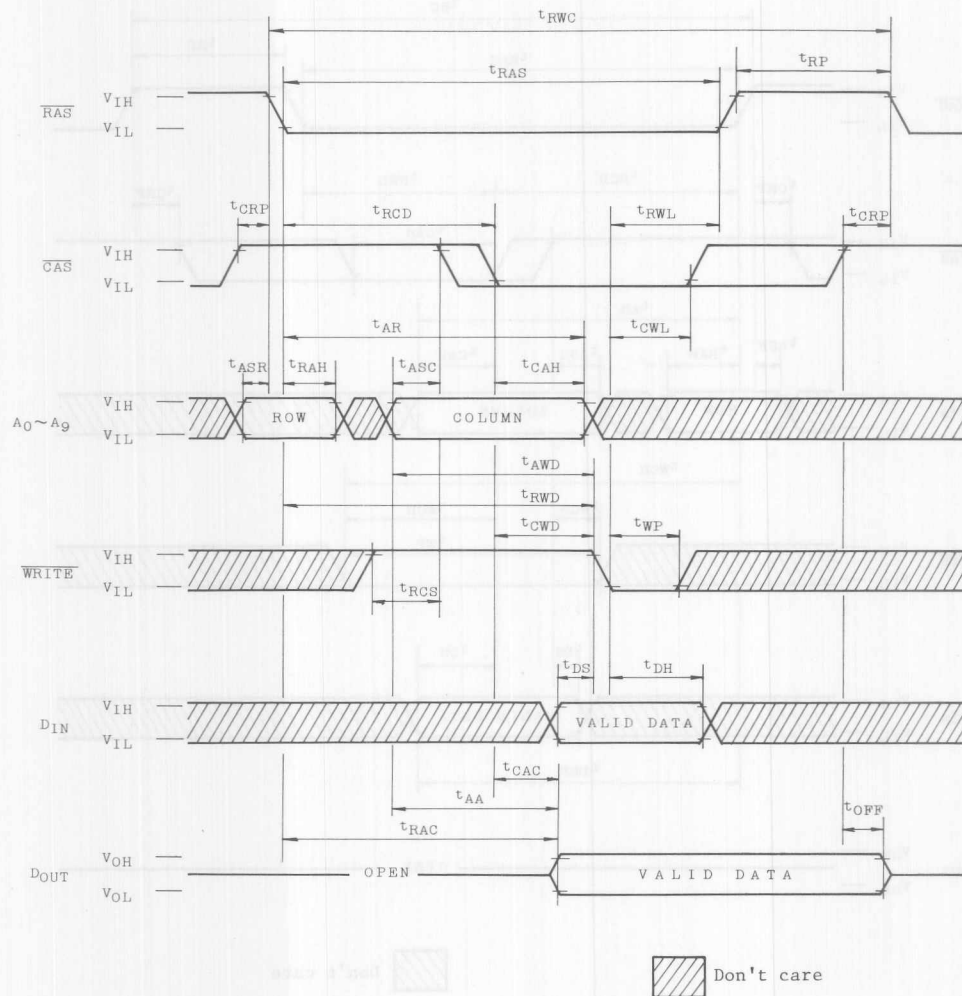
● EARLY WRITE CYCLE



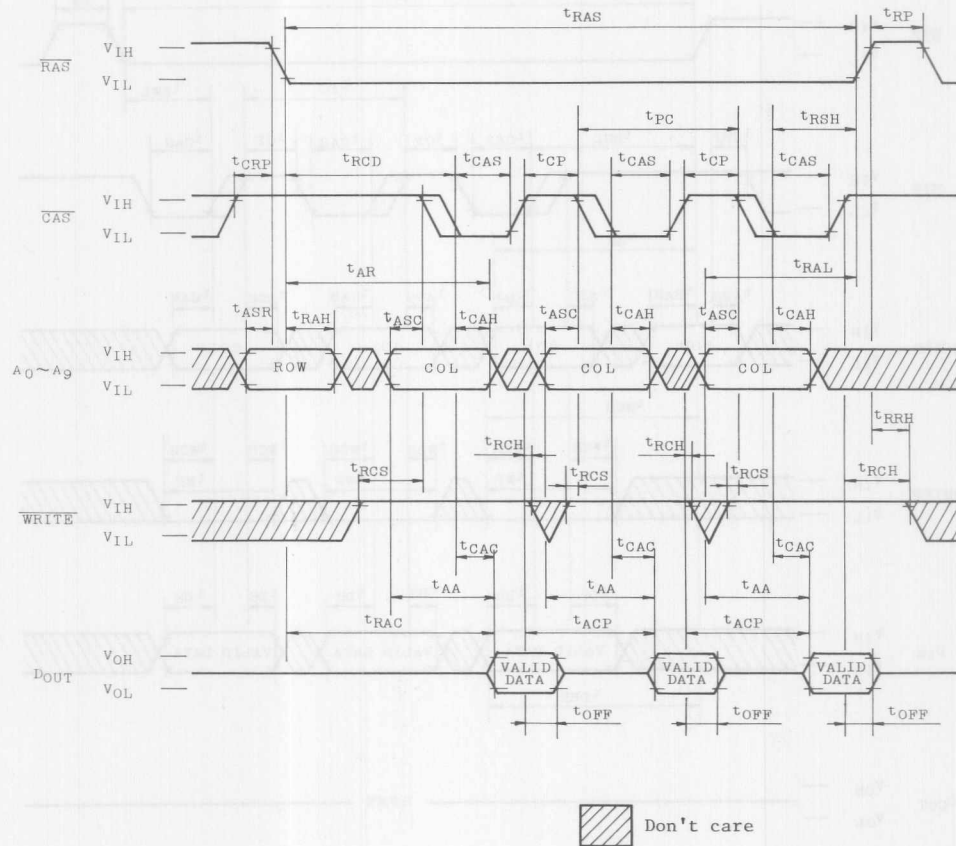
TC511000C-10

TC511000C-12

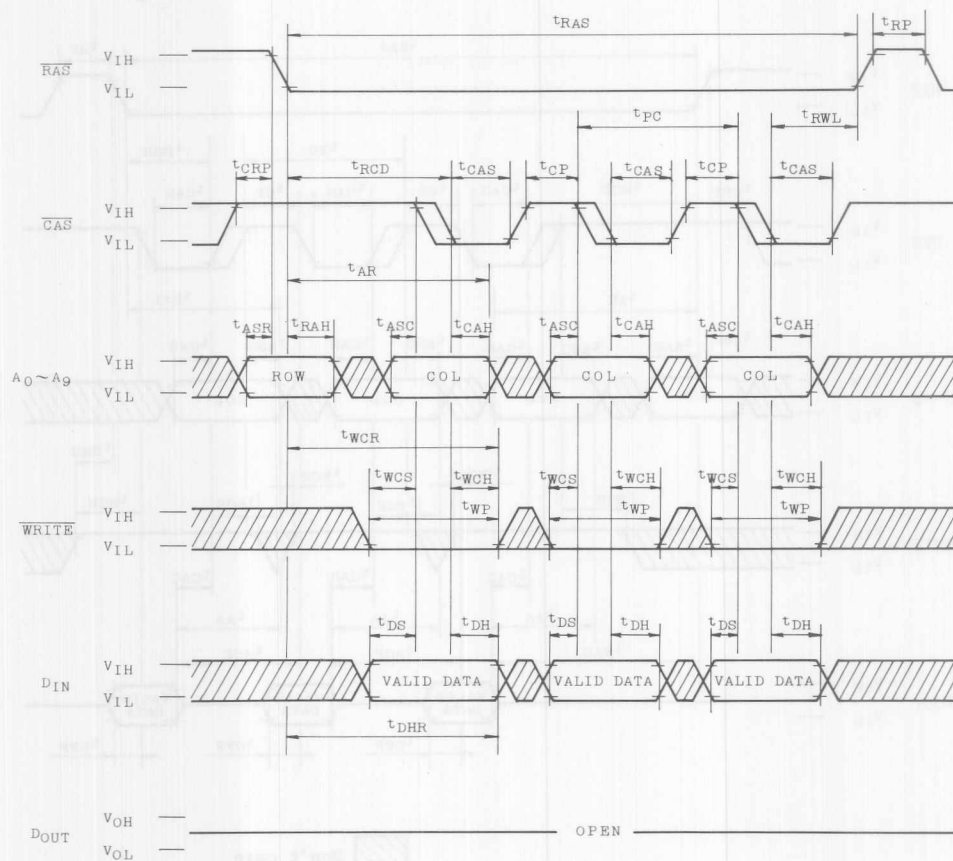
• READ-WRITE/READ-MODIFY-WRITE CYCLE




● FAST PAGE MODE READ CYCLE

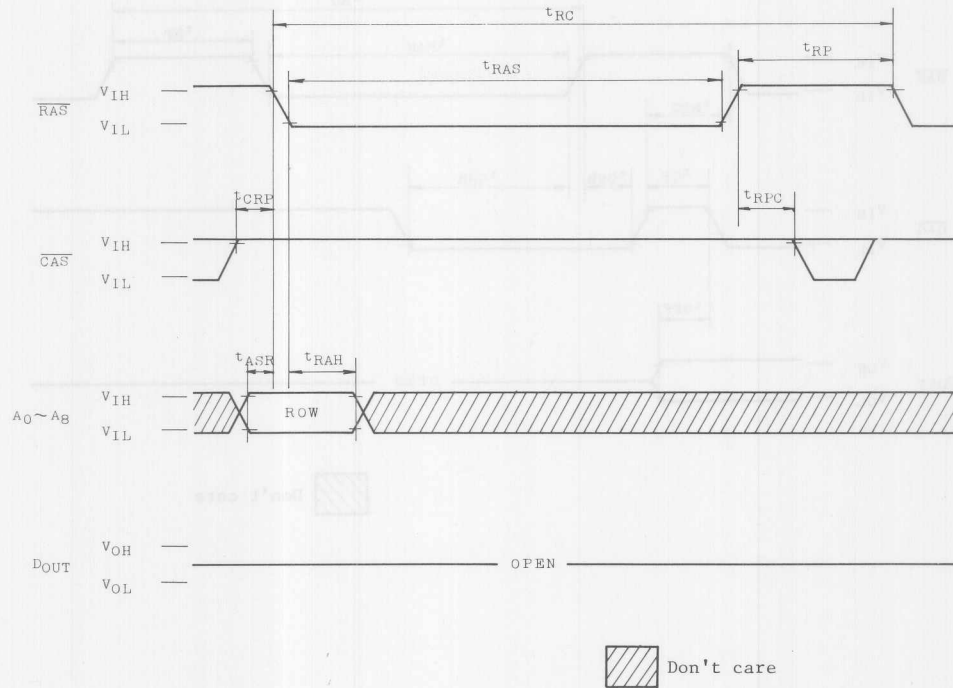


● FAST PAGE MODE WRITE CYCLE



 Don't care

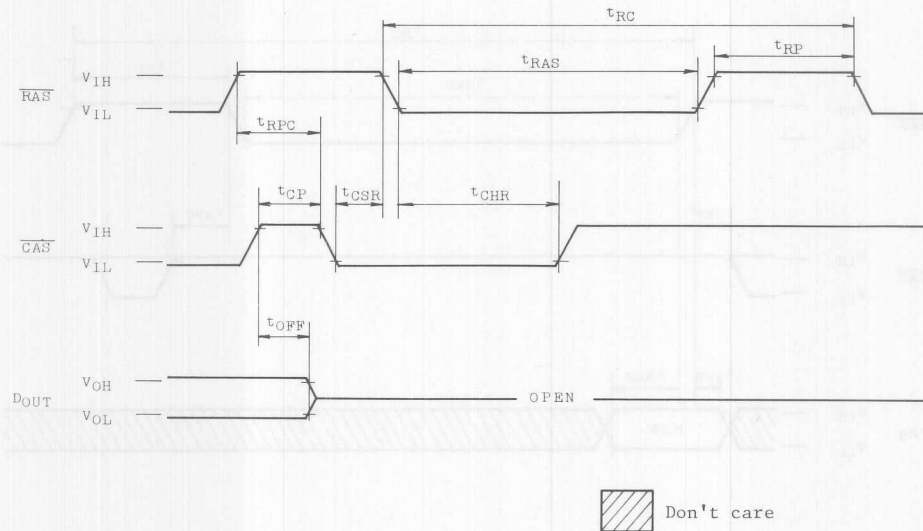
● RAS ONLY REFRESH CYCLE



NOTE : \overline{WRITE} = Don't care, A_9 = Don't care

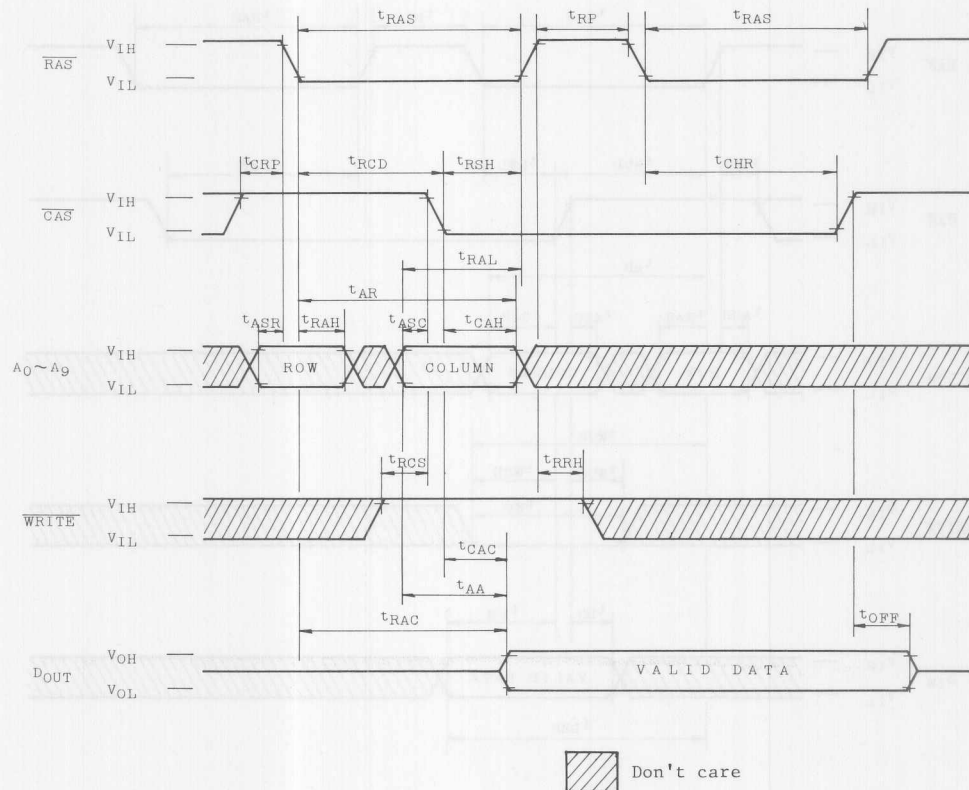
TC511000C-10 TC511000C-12

• $\overline{\text{CAS}}$ BEFORE RAS REFRESH CYCLE



NOTE : $\overline{\text{WRITE}}$ =Don't care, A0~A9=Don't care

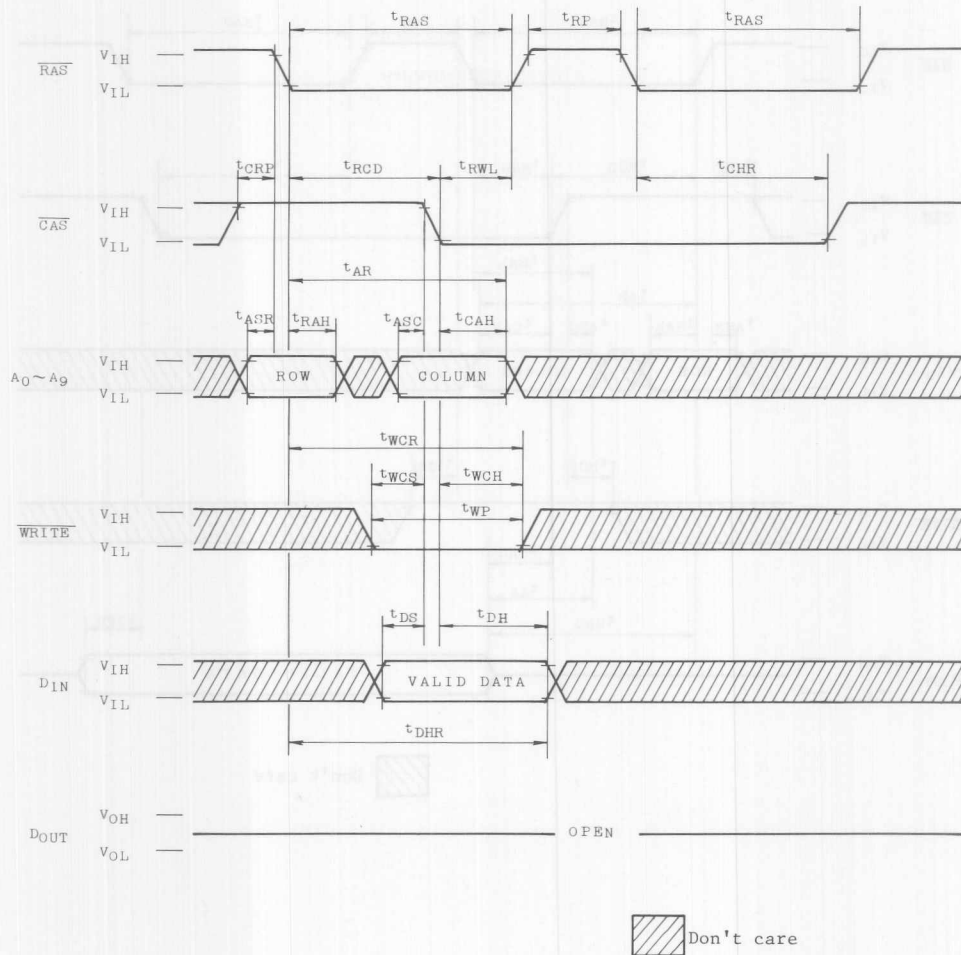
● HIDDEN REFRESH CYCLE (READ)



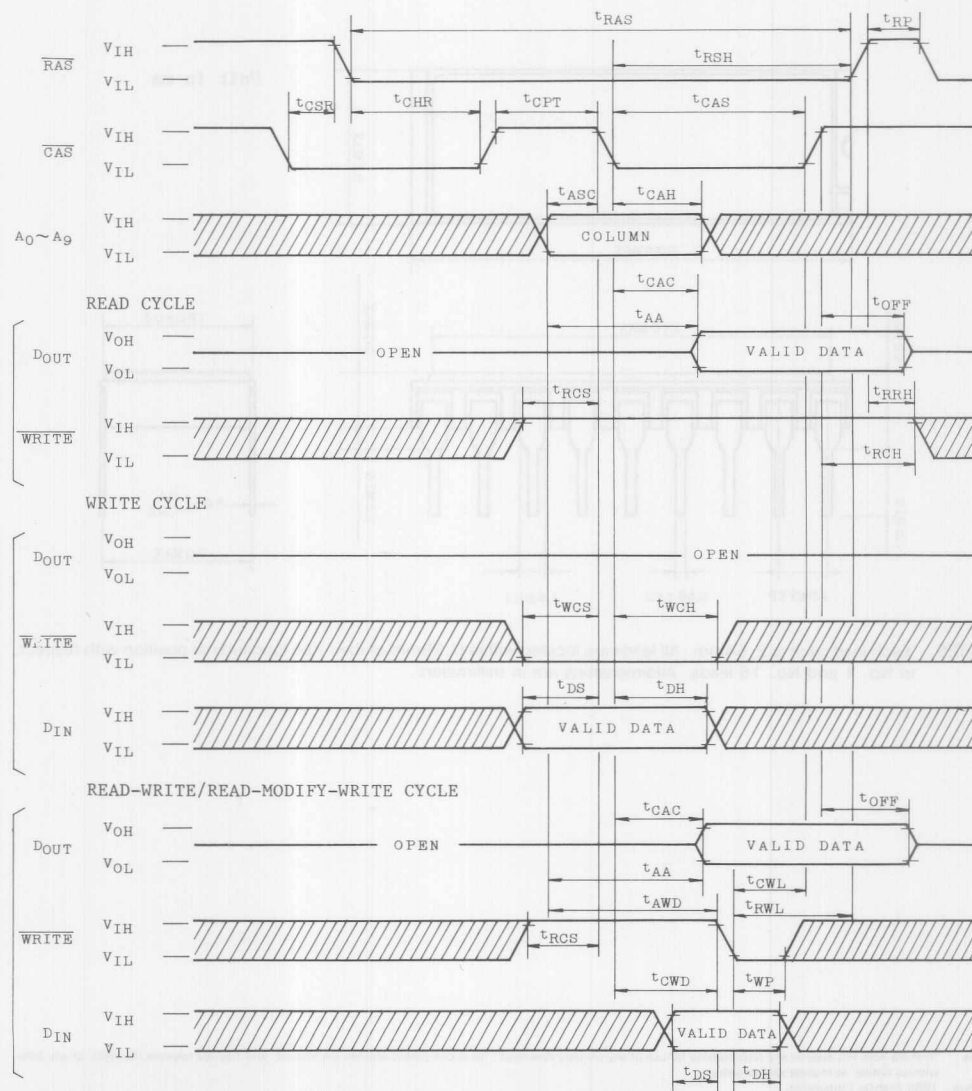
TC511000C-10

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● HIDDEN REFRESH CYCLE (WRITE)

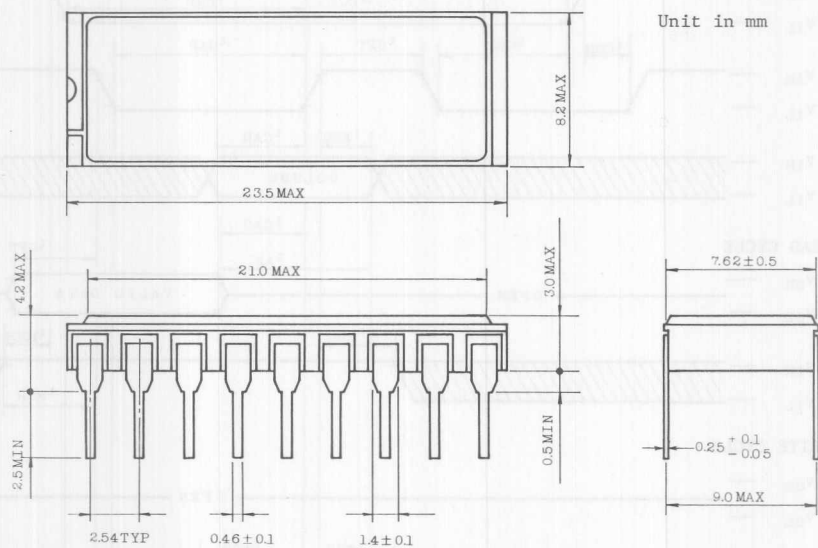


● CAS BEFORE RAS REFRESH COUNTER TEST CYCLE



TC511000C-10 TC511000C-12

● OUTLINE DRAWINGS



NOTES : Each lead pitch is 2.54mm. All leads are located within 0.25mm of their true longitudinal position with respect to No. 1 and No. 16 leads. All dimensions are in millimeters.

Note : Toshiba does not assume any responsibility for use of any circuitry described ; no circuit patent licenses are implied, and Toshiba reserves the right, at any time without notice, to change said circuitry.
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1,048,576 WORD × 1 BIT STATIC COLUMN DYNAMIC RAM
SILICON GATE CMOS

TC511001C-10 TC511001C-12

PRELIMINARY

DESCRIPTION

The TC511001C is the new generation dynamic RAM organized 1,048,576 words by 1 bit. The TC511001C utilizes TOSHIBA's CMOS Silicon gate process technology as well as advanced circuit techniques to provide wide operating margins, both internally and to the system user. Multiplexed address inputs permit the TC511001C to be pack-

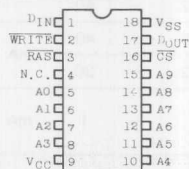
aged in a standard 18 pin ceramic DIP. This package size provides high system bit densities and is compatible with widely available automated testing and insertion equipment. System oriented features include single power supply of $5V \pm 10\%$ tolerance, direct interfacing capability with high performance logic families such as Schottky TTL.

FEATURES

- 1,048,576 words by 1 bit organization
- Fast access time and cycle time

| | TC511001C-10 | TC511001C-12 |
|-----------------------------------|--------------|--------------|
| RAS Access Time | 100ns | 120ns |
| Column Address Access Time | 50ns | 60ns |
| CS Access Time | 20ns | 25ns |
| trc Cycle Time | 190ns | 220ns |
| Static tsc Column Mode Cycle Time | 55ns | 65ns |

PIN CONNECTION (TOP VIEW)

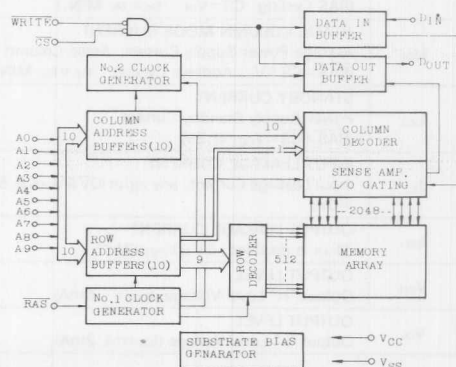


PIN NAMES

| | |
|---------------------------------|--------------------|
| A ₀ ~ A ₉ | Address Inputs |
| RAS | Row Address Strobe |
| DIN | Data In |
| DOUT | Data Out |
| CS | Chip Select Input |
| WRITE | Read/Write Input |
| V _{CC} | Power (+5V) |
| V _{SS} | Ground |
| N. C. | No Connection |

- Single power supply of $5V \pm 10\%$ with a built-in V_{BB} generator
- Low power
330mw Operating (MAX.) (TC511001C-10)
275mW Operating (MAX.) (TC511001C-12)
5.5mW Standby (MAX.)
- Industry standard 18 pin ceramic DIP
- Output unlatched at cycle end allows two-dimensional chip selection
- Common I/O capability
- Read-Modify-Write, RAS-only refresh, and Static Column Mode capability
- All inputs and output TTL compatible
- 512 refresh cycles/8ms

BLOCK DIAGRAM



TC511001C-10

TC511001C-10

| ITEM | SYMBOL | RATING | UNITS | NOTES |
|------------------------------|--------------|-----------------------|--------|-------|
| Input Voltage | V_{IN} | -1~7 | V | 1 |
| Output Voltage | V_{OUT} | -1~ V_{CC} + 0.5 | V | 1 |
| Power Supply Voltage | V_{CC} | -1~7 | V | 1 |
| Operating Temperature | T_{OPR} | 0~70 | °C | 1 |
| Storage Temperature | T_{STG} | -55~150 | °C | 1 |
| Soldering Temperature·Time | T_{SOLDER} | 260·10 | °C·sec | 1 |
| Power Dissipation | P_D | 1 | W | 1 |
| Short Circuit Output Current | I_{OUT} | 50 | mA | 1 |

RECOMMENDED DC OPERATING CONDITIONS (Ta=0~70°C)

| SYMBOL | PARAMETER | MIN. | TYP. | MAX. | UNIT | NOTES |
|----------|--------------------|------|------|------|------|-------|
| V_{CC} | Supply Voltage | 4.5 | 5.0 | 5.5 | V | 2 |
| V_{IH} | Input High Voltage | 2.4 | — | 6.5 | V | 2 |
| V_{IL} | Input Low Voltage | -1.0 | — | 0.8 | V | 2 |

DC ELECTRICAL CHARACTERISTICS (V_{CC}=5V±10%, Ta=0~70°C)

| SYMBOL | PARAMETER | | MIN. | MAX. | UNITS | NOTES |
|-----------|---|--------------|------|------|---------|-------|
| I_{CC1} | OPERATING CURRENT Average Power Supply Operating Current (RAS, CS, Address, Cycling : $t_{RC}=t_{RC}$ MIN.) | TC511001C-10 | — | 60 | mA | 3,4 |
| | | TC511001C-12 | — | 50 | | |
| I_{CC2} | STANDBY CURRENT Power Supply Standby Current (RAS=CS= V_{IH}) | | — | 3 | mA | |
| I_{CC3} | RAS ONLY REFRESH CURRENT Average Power Supply Current, RAS Only Mode (RAS Cycling, CS= V_{IH} : $t_{RC}=t_{RC}$ MIN.) | TC511001C-10 | — | 50 | mA | 3 |
| | | TC511001C-12 | — | 40 | | |
| I_{CC4} | STATIC COLUMN MODE CURRENT Average Power Supply Current, Static Column Mode (RAS=CS= V_{IL} , Address Cycling : $t_{SC}=t_{SC}$ MIN.) | TC511001C-10 | — | 40 | mA | 3,4 |
| | | TC511001C-12 | — | 30 | | |
| I_{CC5} | STANDBY CURRENT Power Supply Standby Current (RAS=CS= $V_{CC}-0.2V$) | | — | 1 | mA | |
| I_{IL} | INPUT LEAKAGE CURRENT Input Leakage Current, any input ($0V \leq V_{IN} \leq 6.5V$, All Other Pins Not Under Test = 0V) | | -10 | 10 | μA | |
| I_{OL} | OUTPUT LEAKAGE CURRENT (D_{OUT} is disabled, $0V \leq V_{OUT} \leq V_{CC}$) | | -10 | 10 | μA | |
| V_{OH} | OUTPUT LEVEL Output "H" Level Voltage ($I_{OUT} = -5mA$) | | 2.4 | — | V | |
| V_{OL} | OUTPUT LEVEL Output "L" Level Voltage ($I_{OUT} = 4.2mA$) | | — | 0.4 | V | |

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

(V_{CC}=5V±10%, T_a=0~70°C) (Notes 5, 6, 7)

| SYMBOL | PARAMETER | TC511001C-10 | | TC511001C-12 | | UNIT | NOTES |
|-------------------|--|--------------|---------|--------------|---------|------|-------|
| | | MIN. | MAX. | MIN. | MAX. | | |
| t _{RC} | Random Read or Write Cycle Time | 190 | — | 220 | — | ns | |
| t _{SC} | Static Column Mode Cycle Time | 55 | — | 65 | — | ns | |
| t _{SRW} | Static Column Mode Read Write Cycle Time | 110 | — | 130 | — | ns | |
| t _T | Transition Time(Rise and Fall) | 3 | 35 | 3 | 35 | ns | 7 |
| t _{RAC} | Access Time from RAS | — | 100 | — | 120 | ns | 8,10 |
| t _{ROH} | Output Data Hold Time from RAS | 0 | — | 0 | — | ns | |
| t _{ROZ} | Output Data Disable Time from RAS | — | 30 | — | 35 | ns | 11 |
| t _{AA} | Access Time from Column Address | — | 50 | — | 60 | ns | 9,10 |
| t _{AOH} | Output Data Hold Time from Column Address | 5 | — | 5 | — | ns | |
| t _{ACS} | Access Time from CS | — | 20 | — | 25 | ns | 10 |
| t _{SOH} | Output Data Hold Time from CS | 0 | — | 0 | — | ns | |
| t _{SOZ} | Output Data Disable Time from CS | — | 30 | — | 35 | ns | 11 |
| t _{OW} | Output Data Enable Time from WRITE | — | 30 | — | 35 | ns | |
| t _{ALW} | Access Time from Last Write | — | 105 | — | 125 | ns | 12 |
| t _{WOH} | Output Data Hold Time from WRITE | 0 | — | 0 | — | ns | |
| t _{RP} | RAS Precharge Time | 80 | — | 90 | — | ns | |
| t _{RAS} | RAS Pulse Width | 100 | 100,000 | 120 | 100,000 | ns | |
| t _{SP} | CS Pulse Width | 20 | — | 25 | — | ns | |
| t _{SI} | CS Inactive Time | 10 | — | 15 | — | ns | |
| t _{RTL} | CS to RAS Lead Time(Read Cycle) | 20 | — | 25 | — | ns | |
| t _{SR} | CS to RAS Set-Up Time(Output Data Disable) | 10 | — | 10 | — | ns | |
| t _{ZRH} | RAS to CS Hold Time(Output Data Disable) | 0 | — | 0 | — | ns | |
| t _{ASR} | Row Address Set-Up Time | 0 | — | 0 | — | ns | |
| t _{RAH} | Row Address Hold Time | 15 | — | 15 | — | ns | |
| t _{RAD} | RAS to Column Address Delay Time | 20 | 50 | 20 | 60 | ns | 13 |
| t _{AR} | Column Address Hold Time Reference to RAS | 100 | — | 120 | — | ns | |
| t _{RAL} | Column Address to RAS Lead Time(Read Cycle) | 50 | — | 60 | — | ns | |
| t _{AHR} | Column Address Hold Time Reference to RAS Rise | 10 | — | 15 | — | ns | 14 |
| t _{LWAD} | Last Write to Column Address Delay Time | — | 55 | — | 65 | ns | 15 |
| t _{AHLW} | Last Write to Column Address Hold Time | 105 | — | 125 | — | ns | |
| t _{RRS} | Read Command Set-Up Time Reference to RAS | 0 | — | 0 | — | ns | 16 |
| t _{RC} | Read Command Set-Up Time Reference to CS | 0 | — | 0 | — | ns | 16 |
| t _{RRH} | Read Command Hold Time Reference to RAS | 0 | — | 0 | — | ns | 17 |
| t _{RCH} | Read Command Hold Time Reference to CS | 0 | — | 0 | — | ns | 17 |
| t _{WP} | WRITE Pulse Width | 20 | — | 25 | — | ns | |
| t _{WI} | WRITE Inactive Time | 10 | — | 15 | — | ns | |
| t _{RWL} | Write Command to RAS Lead Time | 40 | — | 45 | — | ns | |
| t _{RWD} | RAS to WRITE Delay Time(Read-Write Cycle) | 100 | — | 120 | — | ns | 18 |
| t _{AWD} | Column Address to WRITE Delay Time(Read-Write Cycle) | 50 | — | 60 | — | ns | 18 |
| t _{WCR} | Write Command Hold Time Reference to RAS | 70 | — | 85 | — | ns | |

TC511001C-10

TC511001C-12

| SYMBOL | PARAMETER | TC511001C-10 | | TC511001C-12 | | UNITS | NOTES |
|------------------|--|--------------|------|--------------|------|-------|-------|
| | | MIN. | MAX. | MIN. | MAX. | | |
| t _{WS} | Write Command Set-Up Time(Output Data Disable) | 0 | — | 0 | — | ns | 18 |
| t _{WH} | Write Command Hold Time(Output Data Disable) | 0 | — | 0 | — | ns | 18 |
| t _{ASW} | Write Address Set-Up Time | 0 | — | 0 | — | ns | |
| t _{AHW} | Write Address Hold Time | 20 | — | 25 | — | ns | |
| t _{AWR} | Write Address Hold Time Reference to RAS | 70 | — | 85 | — | ns | |
| t _{DS} | Data-In Set-Up Time | 0 | — | 0 | — | ns | |
| t _{DH} | Data-In Hold Time | 20 | — | 25 | — | ns | |
| t _{DHR} | Data-In Hold Time Reference to RAS | 70 | — | 85 | — | ns | |
| t _{REF} | Refresh Period | — | 8 | — | 8 | ms | |

CAPACITANCE (V_{CC}=5V±10%, f=1MHz, Ta=0~70°C)

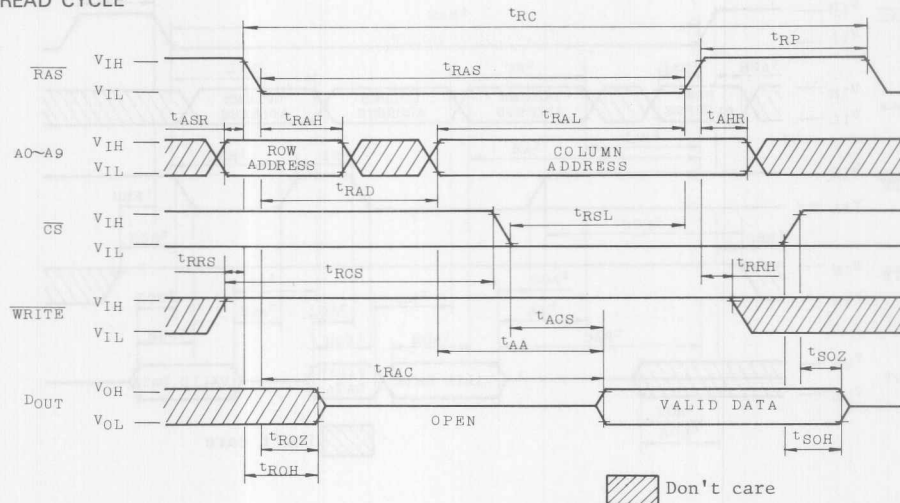
| SYMBOL | PARAMETER | MIN. | MAX. | UNIT |
|-----------------|---|------|------|------|
| C _{I1} | Input Capacitance (A ₀ ~A ₉ , D _{IN}) | — | 6 | pF |
| C _{I2} | Input Capacitance (RAS, CS, WRITE) | — | 7 | pF |
| C _O | Output Capacitance (D _{OUT}) | — | 7 | pF |

NOTES :

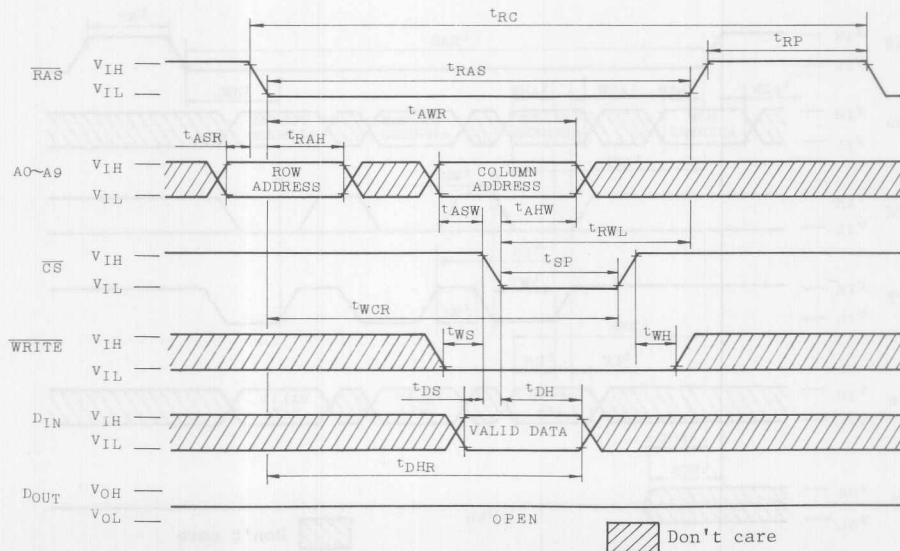
- Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device.
- All voltage are referenced to V_{SS}.
- I_{CC1}, I_{CC3}, I_{CC4} depend on cycle rate.
- I_{CC1}, I_{CC4} depend on output loading. Specified values are obtained with the output open.
- An initial pause of 200μs is required after power-up followed by any 8 RAS cycles before proper device operation is achieved.
- AC measurements assume t_r=5ns.
- V_{IH}(min.) and V_{IL}(max.) are reference levels for measuring timing of input signals. Also, transition times are measured between V_{IH} and V_{IL}.
- Assumes that t_{RAD} ≤ t_{RAD}(max.). If t_{RAD} is greater than the maximum recommended value shown in this table, t_{TRAC} will increase by the amount that t_{RAD} exceeds the value shown.
- Assumes that t_{RAD} ≥ t_{RAD}(max.).
- Measured with a load equivalent to 2 TTL loads and 100pF.
- t_{ROZ} and t_{SOZ} define the time at which the output achieves the open circuit condition and is not referenced to output voltage levels.
- Assumes that t_{LWAD} ≤ t_{LWAD}(max.). If t_{LWAD} is greater than the maximum recommended value shown in this table, t_{ALW} will increase by the amount that t_{LWAD} exceeds the value shown.
- Operation within the t_{RAD}(max.) limit insures that t_{TRAC}(max.) can be met. t_{RAD}(max.) is specified as a reference point only : If t_{RAD} is greater than the specified t_{RAD}(max.) limit, then access time is controlled exclusively by t_{TAA}.
- t_{AHR} is the condition to latch column address when RAS has risen up.
- Operation within the t_{LWAD}(max.) limit insures that t_{ALW}(max.) can be met. t_{LWAD}(max.) is specified as a reference point only : If t_{LWAD} is greater than the specified t_{LWAD}(max.) limit, then access time is controlled exclusively by t_{TAA}.
- Either t_{RCS} or t_{RRS} must be satisfied for a read cycle.
- Either t_{RCH} or t_{RRH} must be satisfied for a read cycle.
- t_{WS}, t_{WH}, t_{RWD} and t_{AWD} are not restrictive operating parameters.
They are included in the data sheet as electrical characteristics only. If t_{WS} ≥ t_{WS}(min.) and t_{WH} ≥ t_{WH}(min.), the data out pin will remain open circuit (high impedance) through the entire cycles ; If t_{RWD} ≥ t_{RWD}(min.) and t_{AWD} ≥ t_{AWD}(min.), the cycle is a read-write cycle and the data out will contain data read from the selected cell : If neither of the above sets of conditions is satisfied, the condition of the data out (at access time) is indeterminate.

TIMING WAVEFORMS

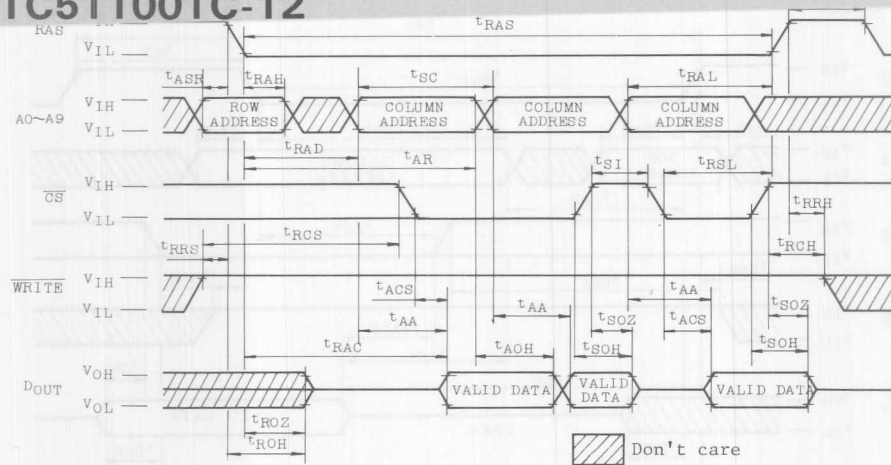
• READ CYCLE



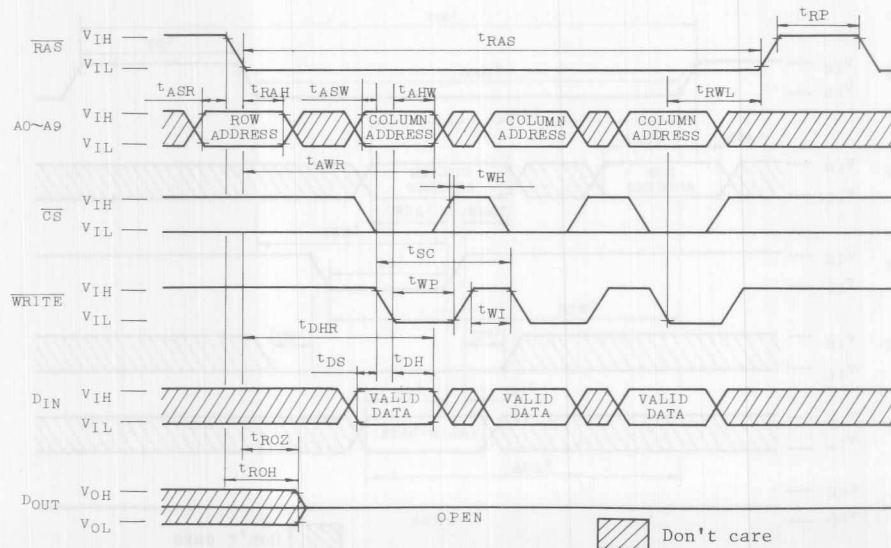
• WRITE CYCLE



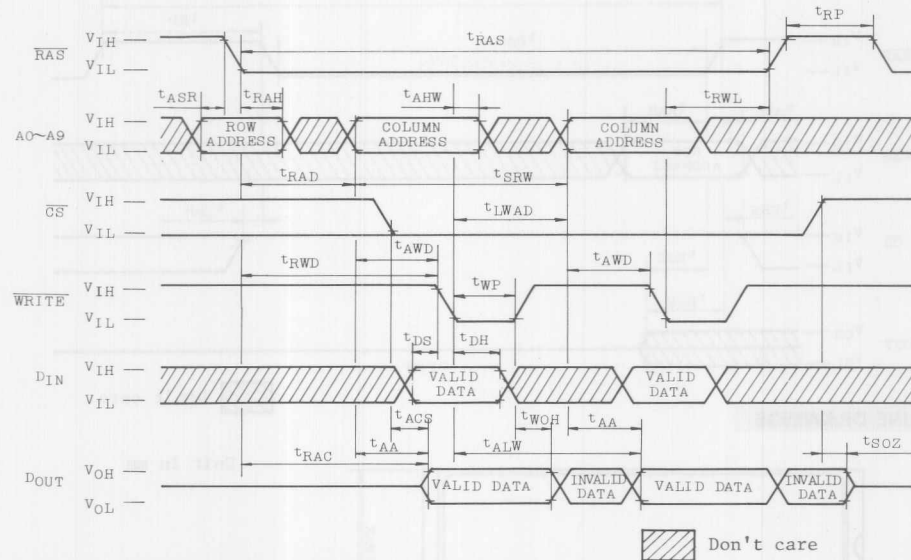
TC511001C-10 TC511001C-12



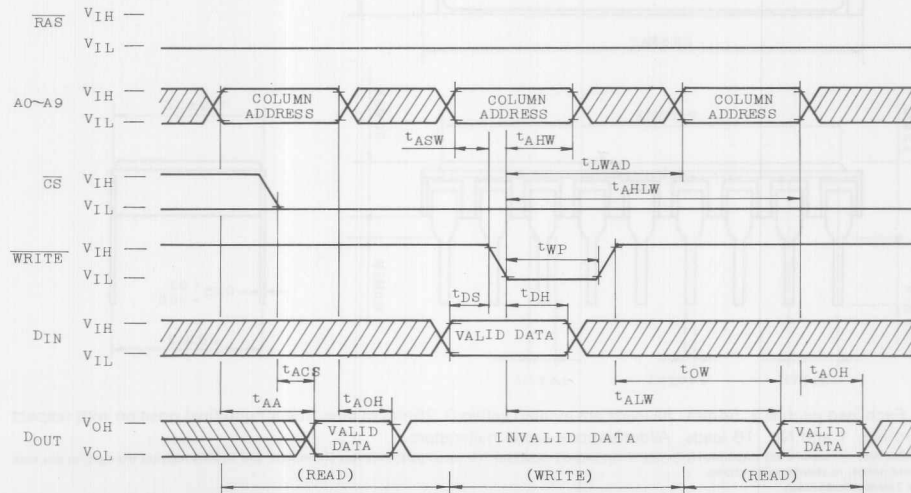
• STATIC COLUMN MODE WRITE CYCLE



● STATIC COLUMN MODE READ-WRITE CYCLE

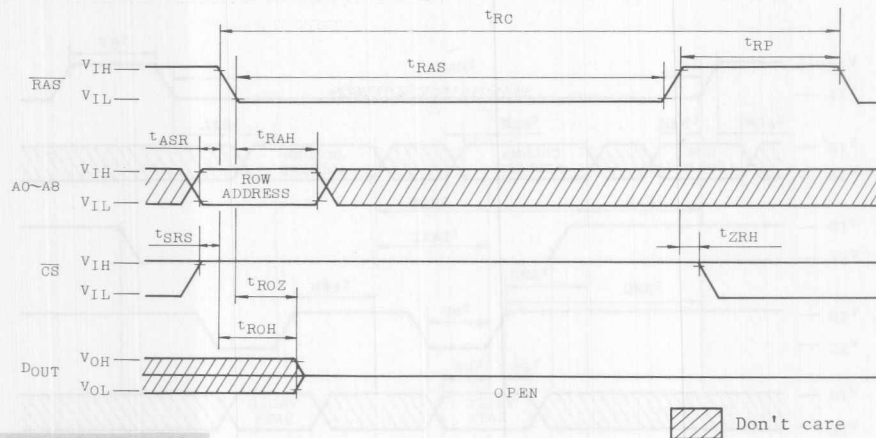


● STATIC COLUMN MODE READ/WRITE MIXED CYCLE

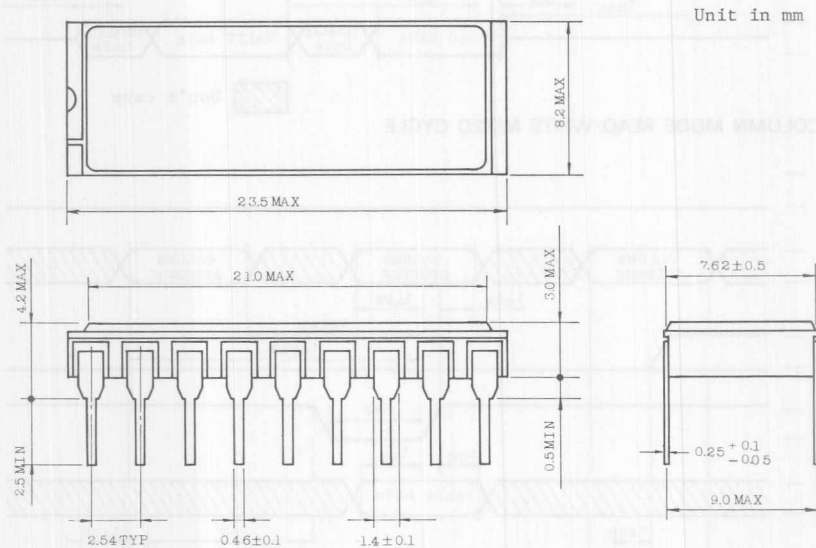


TC511001C-10 TC511001C-12

● RAS ONLY REFRESH CYCLE



OUTLINE DRAWINGS

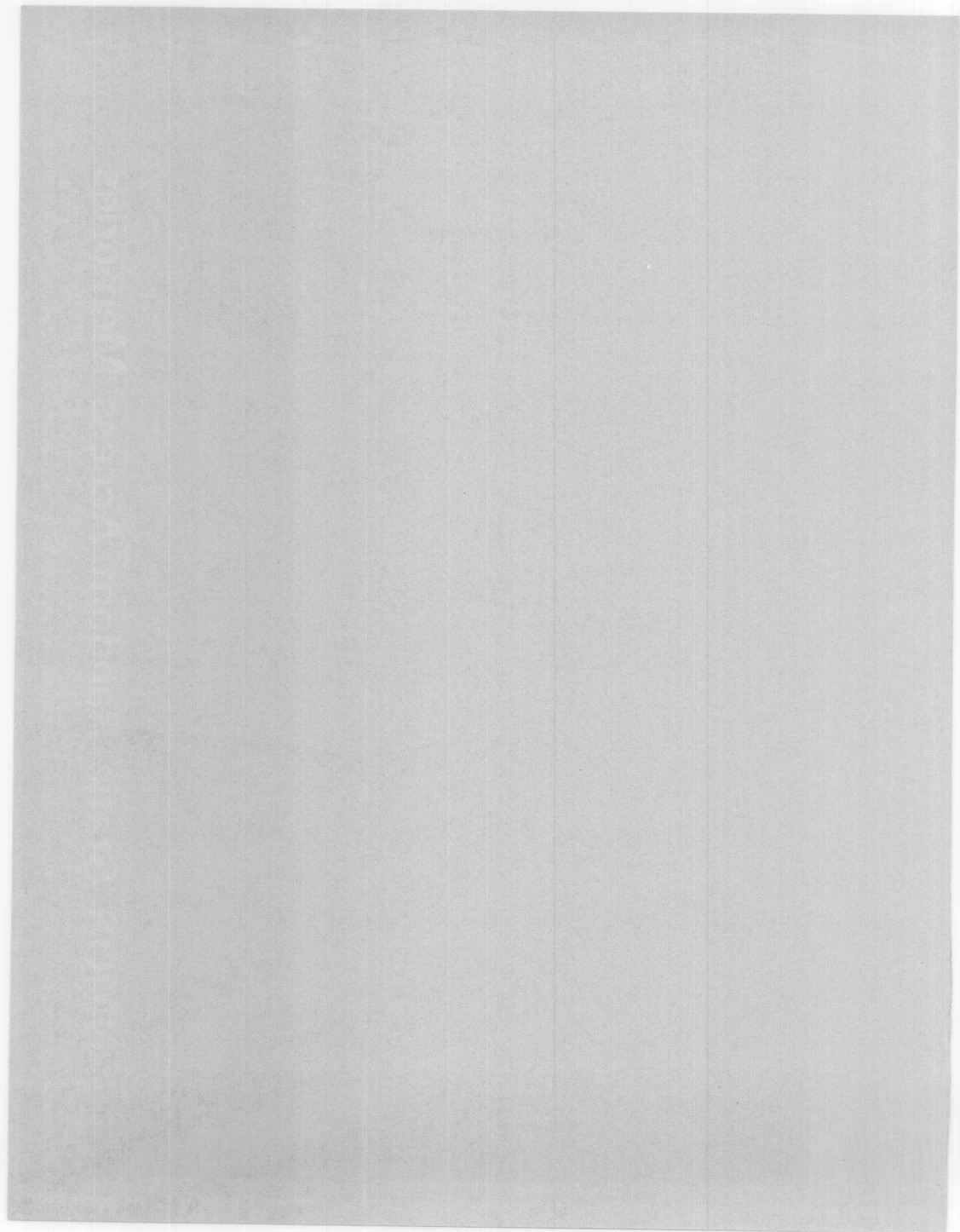


NOTES : Each lead pitch is 2.54mm. All leads are located within 0.25mm of their true longitudinal position with respect to No. 1 and No. 18 leads. All dimensions are in millimeters.

Note : Toshiba does not assume any responsibility for use of any circuitry described ; no circuit patent licenses are implied, and Toshiba reserves the right, at any time without notice, to change said circuitry.

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NMOS Static Random Access Memories



TOSHIBA MOS MEMORY PRODUCTS

2,048 WORD \times 8 BIT STATIC RAM

TMM2015AP-90, TMM2015AP-12
TMM2015AP-10, TMM2015AP-15

DESCRIPTION

The TMM2015AP is a 16,384 bits high speed and low power static random access memory organized as 2,048 words by 8 bits and operates from a single 5V supply. Toshiba's high performance device technology provides both high speed and low power features with a maximum access time of 90ns/100ns/120ns/150ns and maximum operating current of 80mA/65mA/65mA/65mA. When \overline{CS} is a logical

high, the device is placed in a low power standby mode in which maximum standby current is 7mA. Thus the TMM2015AP is most suitable for use in microcomputer peripheral memory where the low power applications are required. The TMM2015AP is fabricated with ion implanted N channel silicon gate MOS technology for high performance and high reliability.

FEATURES

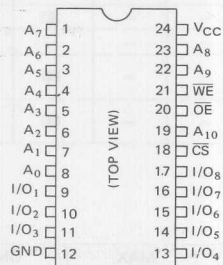
- Access Time and Current

| Parameter Part Number | Access Time (Max.) | Operating Current (Max.) | Standby Current (Max.) |
|--------------------------|-----------------------|--------------------------------|------------------------------|
| TMM2015AP-90 | 90ns | 80mA | 7mA |
| TMM2015AP-10 | 100ns | 65mA | 7mA |
| TMM2015AP-12 | 120ns | 65mA | 7mA |
| TMM2015AP-15 | 150ns | 65mA | 7mA |

- High Density Assembly Capability:
0.3 inch package
(24 pins plastic DIP)

- Single 5V Power Supply
- Fully Static Operation
- Power Down Feature: \overline{CS}
- Output Buffer Control: \overline{OE}
- Three State Outputs
- All Inputs and Outputs: Directly TTL Compatible
- Inputs Protected: All inputs have protection against static charge.

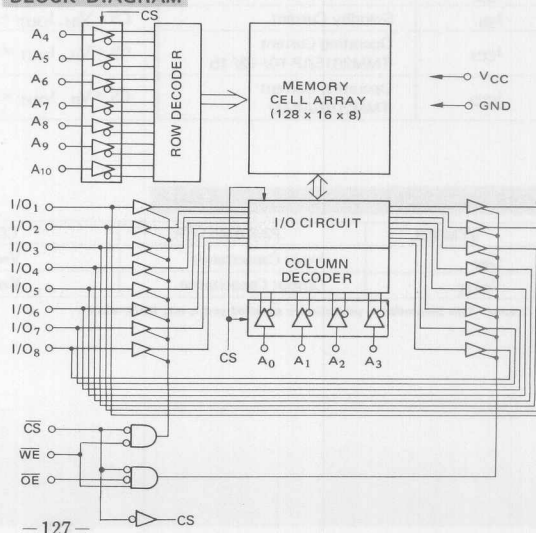
PIN CONNECTION



PIN NAMES

| SYMBOL | NAME |
|--------------------|-----------------------|
| $A_0 \sim A_3$ | Column Address Inputs |
| $A_4 \sim A_{10}$ | Row Address Inputs |
| \overline{CS} | Chip Select Input |
| \overline{WE} | Write Enable Input |
| $I/O_1 \sim I/O_8$ | Data Input/Output |
| \overline{OE} | Output Enable Input |
| V_{CC} | Power (5V) |
| GND | Ground |

BLOCK DIAGRAM



TMM2015AP-90, TMM2015AP-12

TMM2015AP-10, TMM2015AP-15

| | | | |
|-------------------|--|------------|----------|
| V_{IN}, V_{OUT} | Input/Output Voltage | -0.5 ~ 7.0 | V |
| $T_{OPR.}$ | Operating Temperature | 0 ~ 70 | °C |
| $T_{STG.}$ | Storage Temperature | -55 ~ 150 | °C |
| $T_{SOLDER.}$ | Soldering Temperature • Time | 260 • 10 | °C • sec |
| P_D | Power Dissipation ($T_a = 70^\circ\text{C}$) | 0.7 | W |

D.C. RECOMMENDED OPERATING CONDITIONS ($T_a = 0 \sim 70^\circ\text{C}$)

| SYMBOL | PARAMETER | MIN. | TYP. | MAX. | UNIT |
|----------|--------------------|------|------|--------------|------|
| V_{IH} | Input High Voltage | 2.0 | — | $V_{CC}+1.0$ | V |
| V_{IL} | Input Low Voltage | -0.5 | — | 0.8 | V |
| V_{CC} | Supply Voltage | 4.5 | 5.0 | 5.5 | V |

D.C. CHARACTERISTICS ($T_a = 0 \sim 70^\circ\text{C}$, $V_{CC} = 5.0\text{V} \pm 10\%$)

| SYMBOL | PARAMETER | CONDITIONS | MIN. | TYP. | MAX. | UNIT |
|-----------|---|---|------|------|------|---------------|
| I_{IL} | Input Leakage Current | $V_{IN} = 0\text{V} \sim 5.5\text{V}$ | -10 | — | 10 | μA |
| V_{OH} | Output High Voltage | $I_{OUT} = -1.0\text{mA}$ | 2.4 | — | — | V |
| V_{OL} | Output Low Voltage | $I_{OUT} = 2.1\text{mA}$ | — | — | 0.4 | V |
| I_{LO} | Output Leakage Current | $\overline{CS} = V_{IH}$ or $\overline{WE} = V_{IL}$ or $\overline{OE} = V_{IH}$, $V_{OUT} = 0\text{V} \sim 5.5\text{V}$ | -10 | — | 10 | μA |
| I_{SBP} | Peak Power-on Current | $\overline{CS} = V_{CC}$, $I_{OUT} = 0\text{mA}$ | — | — | 30 | mA |
| I_{SB} | Standby Current | $\overline{CS} = V_{IH}$, $I_{OUT} = 0\text{mA}$ | — | — | 7 | mA |
| I_{CC1} | Operating Current TMM2015AP-10/-12/-15 | $\overline{CS} = V_{IL}$, $I_{OUT} = 0\text{mA}$ | — | — | 65 | mA |
| I_{CC2} | Operating Current TMM2015AP-90 | $\overline{CS} = V_{IL}$, $I_{OUT} = 0\text{mA}$ | — | — | 80 | mA |

CAPACITANCE* ($T_a = 25^\circ\text{C}$, $f = 1.0\text{MHz}$)

| SYMBOL | PARAMETER | CONDITIONS | MAX. | UNIT |
|-----------|--------------------|----------------------|------|------|
| C_{IN} | Input Capacitance | $V_{IN} = 0\text{V}$ | 5 | pF |
| C_{OUT} | Output Capacitance | $V_{IN} = 0\text{V}$ | 10 | pF |

* Note: This parameter is periodically sampled and is not 100% tested.

TMM2015AP-90, TMM2015AP-12 TMM2015AP-10, TMM2015AP-15

A.C. CHARACTERISTICS (Ta = 0 ~ 70°C, Vcc = 5V ± 10%)

READ CYCLE

| SYMBOL | PARAMETER | TMM2015AP-90 | | TMM2015AP-10 | | TMM2015AP-12 | | TMM2015AP-15 | | UNIT |
|------------------|---|--------------|------|--------------|------|--------------|------|--------------|------|------|
| | | MIN. | MAX. | MIN. | MAX. | MIN. | MAX. | MIN. | MAX. | |
| t _{RC} | Read Cycle Time | 90 | — | 100 | — | 120 | — | 150 | — | ns |
| t _{ACC} | Address Access Time | — | 90 | — | 100 | — | 120 | — | 150 | ns |
| t _{CO} | Chip Select Access Time | — | 90 | — | 100 | — | 120 | — | 150 | ns |
| t _{OE} | Output Enable Time | — | 35 | — | 35 | — | 50 | — | 55 | ns |
| t _{OH} | Output Data Hold Time from Address Change | 10 | — | 10 | — | 10 | — | 10 | — | ns |
| t _{CLZ} | CS to Output in Low-Z | 10 | — | 10 | — | 10 | — | 10 | — | ns |
| t _{CHZ} | CS to Output in High-Z | — | 40 | — | 40 | — | 40 | — | 55 | ns |
| t _{OLZ} | OE to Output in Low-Z | 5 | — | 5 | — | 5 | — | 5 | — | ns |
| t _{OHZ} | OE to Output in High-Z | — | 35 | — | 35 | — | 35 | — | 50 | ns |
| t _{PU} | Chip Selection to Power Up Time | 0 | — | 0 | — | 0 | — | 0 | — | ns |
| t _{PD} | Chip Deselection to Power Down Time | — | 50 | — | 50 | — | 60 | — | 60 | ns |

WRITE CYCLE

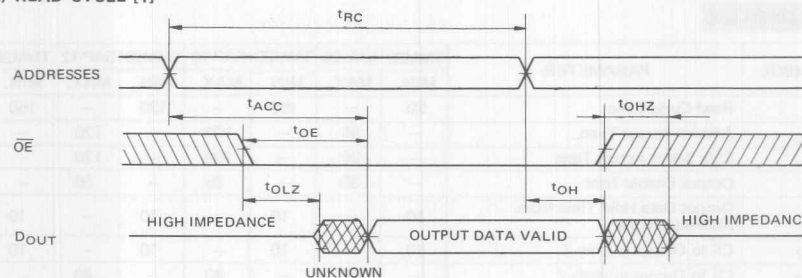
| SYMBOL | PARAMETER | TMM2015AP-90 | | TMM2015AP-10 | | TMM2015AP-12 | | TMM2015AP-15 | | UNIT |
|------------------|--------------------------------|--------------|------|--------------|------|--------------|------|--------------|------|------|
| | | MIN. | MAX. | MIN. | MAX. | MIN. | MAX. | MIN. | MAX. | |
| t _{WC} | Write Cycle Time | 90 | — | 100 | — | 120 | — | 150 | — | ns |
| t _{CW} | Chip Selection to End of Write | 70 | — | 80 | — | 100 | — | 120 | — | ns |
| t _{AS} | Address Set up Time | 20 | — | 20 | — | 20 | — | 20 | — | ns |
| t _{WP} | Write Pulse Width | 60 | — | 70 | — | 85 | — | 100 | — | ns |
| t _{WR} | Write Recovery Time | 0 | — | 0 | — | 0 | — | 0 | — | ns |
| t _{DS} | Data Set up Time | 35 | — | 40 | — | 50 | — | 60 | — | ns |
| t _{DH} | Data Hold Time | 0 | — | 0 | — | 0 | — | 0 | — | ns |
| t _{WLZ} | WE to Output in Low-Z | 5 | — | 5 | — | 5 | — | 5 | — | ns |
| t _{WHZ} | WE to Output in High-Z | — | 25 | — | 30 | — | 35 | — | 50 | ns |

A.C. TEST CONDITIONS

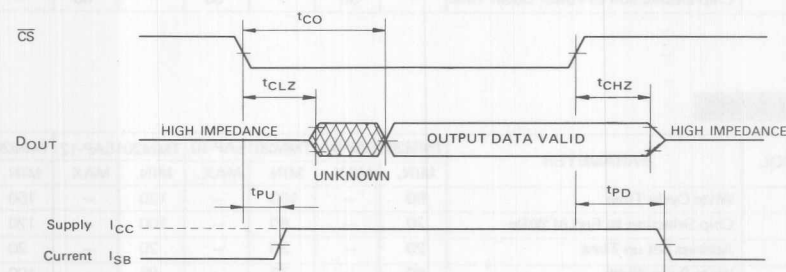
| | |
|-----------------------------------|-------------------------------------|
| Input Pulse Levels | 0 ~ 3.5V |
| Input Rise and Fall Time | 10 ns |
| Input and Output Reference Levels | 1.5V |
| Output Load | 1 TTL Gate & C _L = 100pF |

TIMING WAVEFORMS

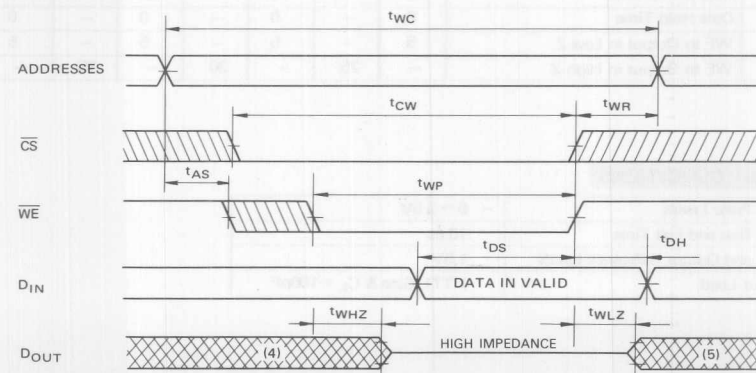
(A) READ CYCLE [1] ⁽¹⁾

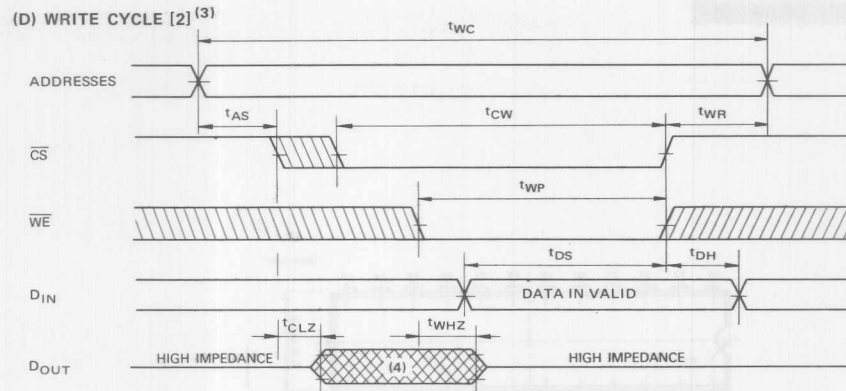


(B) READ CYCLE [2] ⁽¹⁾⁽²⁾



(C) WRITE CYCLE [1] ⁽³⁾





- Note: (1) The \overline{WE} is high for read cycle.
Device is continuously selected, $\overline{CS} = V_{IL}$ in read cycle [1].
- (2) All addresses are valid prior to or simultaneously with \overline{CS} transitions.
- (3) A write occurs during the overlap of low \overline{CS} and low \overline{WE} .
The t_{CW} is specified as the time from the chip selection to end of write in write cycle, and the t_{WP} is specified as the overlap time of low \overline{CS} and low \overline{WE} .
 \overline{OE} is allowed to be low or high level in write cycle.
If the \overline{OE} is high, the output buffers remain in a high impedance state in this period.
- (4) If the \overline{CS} low transition occurs simultaneously with or latter to the \overline{WE} low transition, the output buffers remain in a high impedance state in this period.
- (5) If the \overline{CS} high transition occurs simultaneously with \overline{WE} high transition, the output buffers remain in a high impedance state in this period.

These parameters are specified as follows and measured by using the load shown in Fig. 1.

- (A) t_{CLZ} , t_{OLZ} , t_{WLZ} Output Enable Time
(B) t_{CHZ} , t_{OHZ} , t_{WHZ} Output Disable Time

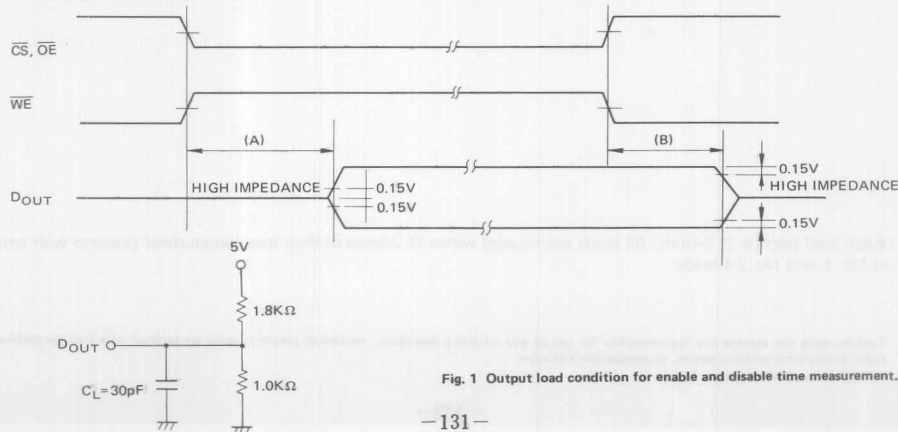
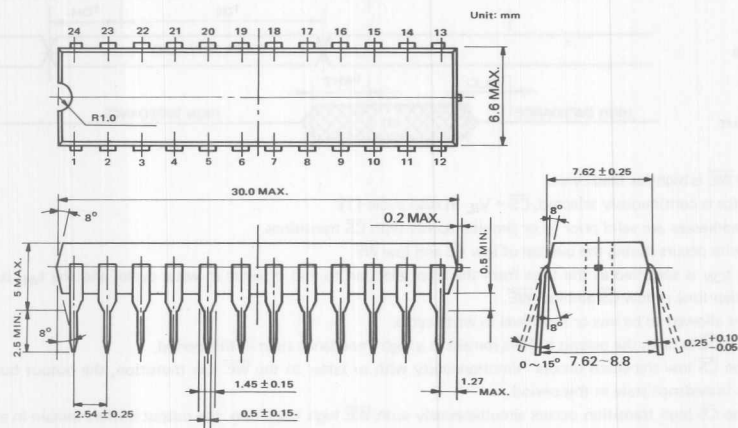


Fig. 1 Output load condition for enable and disable time measurement.



Note : Each lead pitch is 2.54mm. All leads are located within 0.25mm of their true longitudinal position with respect to No. 1 and No. 24 leads.

Note: Toshiba does not assume any responsibility for use of any circuitry described; no circuit patent licenses are implied, and Toshiba reserves the right, at any time without notice, to change said circuitry.

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TOSHIBA MOS MEMORY PRODUCTS

2,048 WORD × 8 BIT STATIC RAM **TMM2015BP-90, TMM2015BP-12**
 SILICON MONOLITHIC
 N-CHANNEL SILICON GATE MOS PROCESS **TMM2015BP-10, TMM2015BP-15**

DESCRIPTION

The TMM2015BP is a 16,384 bits high speed and low power static random access memory organized as 2,048 words by 8 bits and operates from a single 5V supply. Toshiba's high performance device technology provides both high speed and low power features with a maximum access time of 90ns/100ns/120ns/150ns and maximum operating current of 50mA. When \overline{CS} is a logical high, the device

is placed in a low power standby mode in which maximum standby current is 5mA. Thus the TMM2015BP is most suitable for use in microcomputer peripheral memory where the low power applications are required. The TMM2015BP is fabricated with ion implanted N channel silicon gate MOS technology for high performance and high reliability.

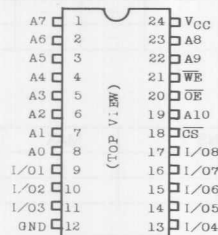
FEATURES

- Access Time and Current

| Part Number | Parameter | Access Time (Max.) | Operating Current (Max.) | Standby Current (Max.) |
|--------------|-----------|--------------------|--------------------------|------------------------|
| TMM2015BP-90 | | 90ns | 50mA | 5mA |
| TMM2015BP-10 | | 100ns | 50mA | 5mA |
| TMM2015BP-12 | | 120ns | 50mA | 5mA |
| TMM2015BP-15 | | 150ns | 50mA | 5mA |

- High Density Assembly Capability:
0.3 inch width package (24pin plastic DIP)

PIN CONNECTION

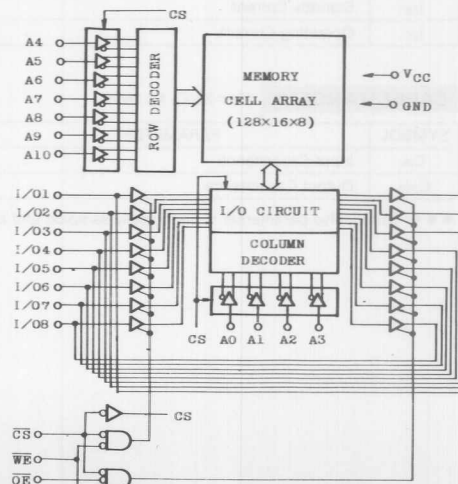


PIN NAMES

| | |
|------------------------------------|-----------------------|
| A ₀ ~A ₃ | Column Address Inputs |
| A ₄ ~A ₁₀ | Row Address Inputs |
| \overline{CS} | Chip Select Input |
| WE | Write Enable Input |
| I/O ₀ ~I/O ₈ | Data Input/Output |
| \overline{OE} | Output Enable Input |
| V _{CC} | Power (5V) |
| GND | Ground |

- Single 5V power Supply
- Fully Static Operation
- Power Down Feature: \overline{CS}
- Output Buffer Control: \overline{OE}
- Three State Outputs
- All Inputs and Outputs: Directly TTL Compatible
- Inputs Protected: All inputs have protection against static charge.

BLOCK DIAGRAM



TMM2015BP-90, TMM2015BP-12 TMM2015BP-10, TMM2015BP-15

MAXIMUM RATINGS

| SYMBOL | ITEM | RATING | UNIT |
|------------------------------------|------------------------------|-----------|--------|
| V _{CC} | Power Supply Voltage | -0.5~7.0 | V |
| V _{IN} , V _{OUT} | Input/Output Voltage | -0.5*~7.0 | V |
| T _{OPR} | Operating Temperature | 0~70 | °C |
| T _{STG} | Storage Temperature | -55~150 | °C |
| T _{SOLDER} | Soldering Temperature · Time | 260 · 10 | °C·sec |
| P _D | Power Dissipation (Ta=70°C) | 0.7 | W |

* -3.0V at Pulse width 50ns

D. C. RECOMMENDED OPERATING CONDITIONS (Ta=0~70°C)

| SYMBOL | PARAMETER | MIN. | TYP. | MAX. | UNIT |
|-----------------|----------------------|--------|------|----------------------|------|
| V _{IH} | Input High Voltage | 2.0 | — | V _{CC} +1.0 | V |
| V _{IL} | Input Low Voltage | -0.5** | — | 0.8 | V |
| V _{CC} | Power Supply Voltage | 4.5 | 5.0 | 5.5 | V |

** -3.0V at Pulse width 50ns

D. C. CHARACTERISTICS (Ta=0~70°C, V_{CC}=5V±10%)

| SYMBOL | PARAMETER | CONDITIONS | MIN. | TYP. | MAX. | UNIT |
|------------------|------------------------|--|------|------|------|------|
| I _{IL} | Input Leakage Current | V _{IN} =0V~5.5V | -10 | — | 10 | μA |
| V _{OH} | Output High Voltage | I _{OUT} =-1.0mA | 2.4 | — | — | V |
| V _{OL} | Output Low Voltage | I _{OUT} =4.0mA | — | — | 0.4 | V |
| I _{LO} | Output Leakage Current | CS=V _{IH} or WE=V _{IL} or OE=V _{IH} , V _{OUT} =0V~5.5V | -10 | — | 10 | μA |
| I _{SBP} | Peak Power-on Current | CS=V _{CC} , I _{OUT} =0mA | — | — | 10 | mA |
| I _{SB} | Standby Current | CS=V _{IH} , I _{OUT} =0mA | — | — | 5 | mA |
| I _{CC} | Operating Current | CS=V _{IL} , I _{OUT} =0mA | — | — | 50 | mA |

CAPACITANCE*** (Ta=25°C, f=1MHz)

| SYMBOL | PARAMETER | CONDITIONS | MAX. | UNIT |
|------------------|--------------------|----------------------|------|------|
| C _{IN} | Input Capacitance | V _{IN} =0V | 5 | pF |
| C _{OUT} | Output Capacitance | V _{OUT} =0V | 10 | pF |

*** Note : This parameter is periodically sampled and is not 100% tested.

TMM2015BP-90, TMM2015BP-12 TMM2015BP-10, TMM2015BP-15

A. C. CHARACTERISTICS (Ta=0~70°C, Vcc=5V±10%)

Read Cycle

| SYMBOL | PARAMETER | TMM2015BP-90 | | TMM2015BP-10 | | TMM2015BP-12 | | TMM2015BP-15 | | UNIT |
|------------------|---|--------------|------|--------------|------|--------------|------|--------------|------|------|
| | | MIN. | MAX. | MIN. | MAX. | MIN. | MAX. | MIN. | MAX. | |
| t _{RC} | Read Cycle Time | 90 | — | 100 | — | 120 | — | 150 | — | ns |
| t _{ACC} | Address Access Time | — | 90 | — | 100 | — | 120 | — | 150 | |
| t _{CO} | Chip Select Access Time | — | 90 | — | 100 | — | 120 | — | 150 | |
| t _{OE} | Output Enable Time | — | 35 | — | 35 | — | 50 | — | 55 | |
| t _{OH} | Output Data Hold Time from Address Change | 10 | — | 10 | — | 10 | — | 10 | — | |
| t _{CLZ} | \overline{CS} to Output in Low-Z | 15 | — | 15 | — | 15 | — | 15 | — | |
| t _{CHZ} | \overline{CS} to Output in High-Z | — | 40 | — | 40 | — | 40 | — | 55 | |
| t _{OLZ} | \overline{OE} to Output in Low-Z | 5 | — | 5 | — | 5 | — | 5 | — | |
| t _{OHZ} | \overline{OE} to Output in High-Z | — | 35 | — | 35 | — | 35 | — | 50 | |
| t _{PU} | Chip Selection to power Up Time | 0 | — | 0 | — | 0 | — | 0 | — | |
| t _{PD} | Chip Deselection to Power Down Time | — | 50 | — | 50 | — | 60 | — | 60 | |

Write Cycle

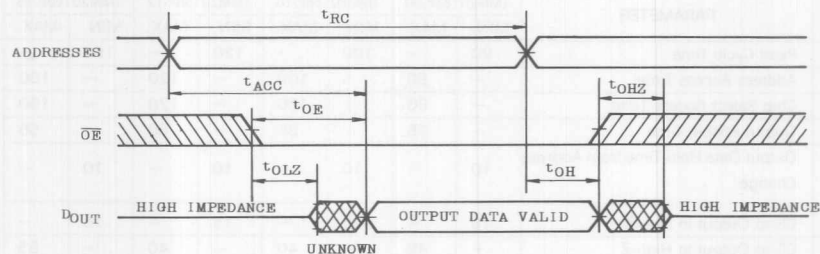
| SYMBOL | PARAMETER | TMM2015BP-90 | | TMM2015BP-10 | | TMM2015BP-12 | | TMM2015BP-15 | | UNIT |
|------------------|-------------------------------------|--------------|------|--------------|------|--------------|------|--------------|------|------|
| | | MIN. | MAX. | MIN. | MAX. | MIN. | MAX. | MIN. | MAX. | |
| t _{WC} | Write Cycle Time | 90 | — | 100 | — | 120 | — | 150 | — | ns |
| t _{CW} | Chip Selection to End of Write | 60 | — | 70 | — | 85 | — | 100 | — | |
| t _{AS} | Address Set Up Time | 20 | — | 20 | — | 20 | — | 20 | — | |
| t _{WP} | Write Pulse Width | 55 | — | 65 | — | 80 | — | 100 | — | |
| t _{WR} | Write Recovery Time | 0 | — | 0 | — | 0 | — | 0 | — | |
| t _{DS} | Data Set Up Time | 30 | — | 35 | — | 45 | — | 50 | — | |
| t _{DH} | Data Hold Time | 0 | — | 0 | — | 0 | — | 0 | — | |
| t _{WLZ} | \overline{WE} to Output in Low-Z | 5 | — | 5 | — | 5 | — | 5 | — | |
| t _{WHZ} | \overline{WE} to Output in High-Z | — | 25 | — | 30 | — | 35 | — | 50 | |

A. C. TEST CONDITIONS

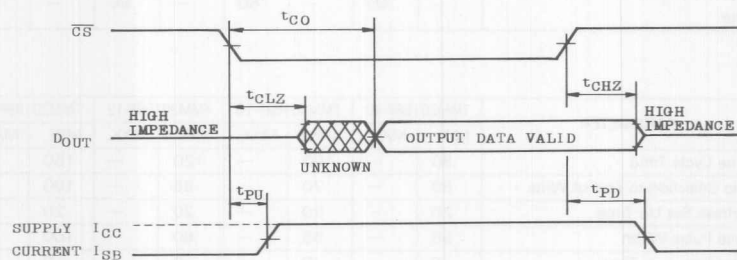
| | |
|--|------------------------------------|
| Input Pulse Levels | 0~3.5V |
| Input Rise and Fall Time | 10ns |
| Input and Output Timing Reference Levels | 1.5V |
| Output Load | 1 TTL Gate & C _L =100pF |

TMM2015BP-90, TMM2015BP-12

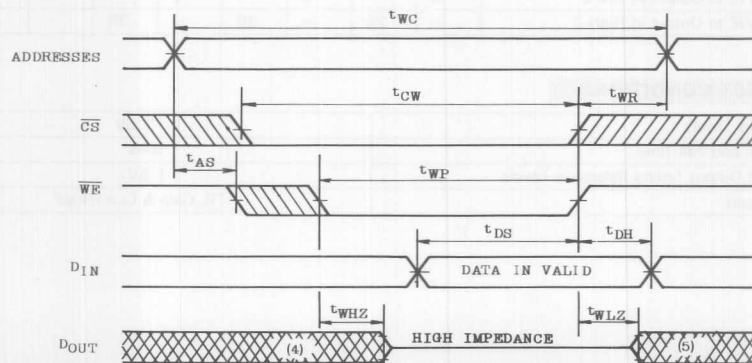
• (A) READ CYCLE [1] (1)



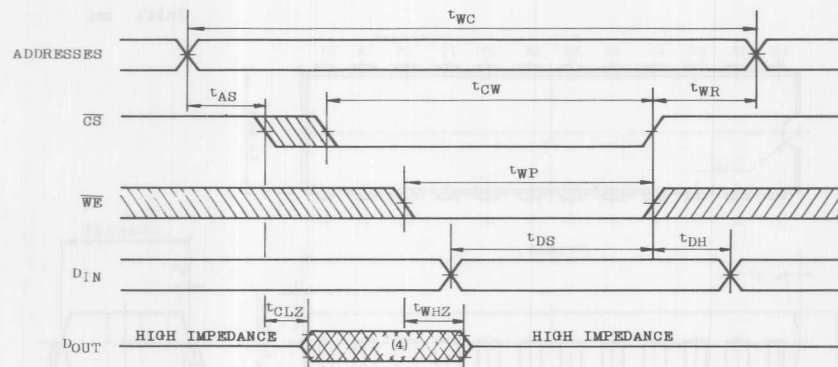
• (B) READ CYCLE [2] (1), (2)



• (C) WRITE CYCLE [1] (3)



• (D) WRITE CYCLE (2) (3)



NOTES:

- (1) The \overline{WE} is high for read cycle.
Device is continuously selected, $\overline{CS} = V_{IL}$ in read cycle (1)
- (2) All addresses are valid prior to or simultaneously with \overline{CS} transitions.
- (3) A write occurs during the overlap of low \overline{CS} and low \overline{WE} .
The t_{CW} is specified as the time from the chip selection to end of write in write cycle, and the t_{WP} is specified as the overlap time of low \overline{CS} and low \overline{WE} .
 \overline{OE} is allowed to be low or high level in write cycle.
If the \overline{OE} is high, the output buffers remain in a high impedance state in this period.
- (4) If the \overline{CS} low transition occurs simultaneously with or latter to the \overline{WE} low transition, the output buffers remain in a high impedance state in this period.
- (5) If the \overline{CS} high transition occurs simultaneously with \overline{WE} high transition, the output buffers remain in a high impedance state in this period.

These parameters are specified as follows and measured by using the load shown in Fig. 1.

(A) t_{CLZ} , t_{OLZ} , t_{WLZ} Output Enable Time

(B) t_{CHZ} , t_{OHZ} , t_{WHZ} Output Disable Time

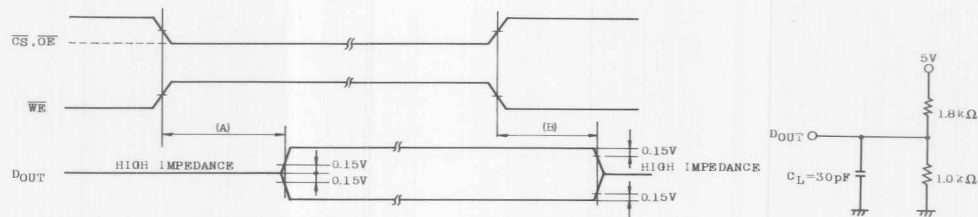
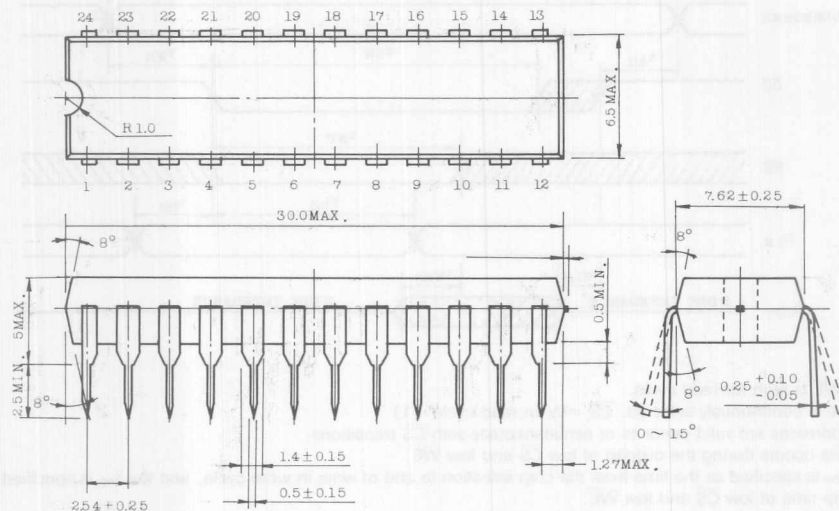


Fig. 1 Output load condition for enable disable time measurement.

TMM2015BP-90, TMM2015BP-12 TMM2015BP-10, TMM2015BP-15

OUTLINE DRAWINGS

Unit: mm



NOTES : Each lead pitch is 2.54mm. All leads are located within 0.25mm of their true longitudinal position with respect to No.1 and No.24 leads.

Note : Toshiba does not assume any responsibility for use of any circuitry described ; no circuit patent licenses are implied, and Toshiba reserves the right, at any time without notice, to change said circuitry.
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TOSHIBA MOS MEMORY PRODUCTS

2,048 WORD × 8 BIT STATIC RAM

TMM2016AP-90, TMM2016AP-12
TMM2016AP-10, TMM2016AP-15

DESCRIPTION

The TMM2016AP is a 16,384 bits high speed and low power static random access memory organized as 2,048 words by 8 bits and operates from a single 5V supply. Toshiba's high performance device technology provides both high speed and low power features with a maximum access time of 90ns/100ns/120ns/150ns and maximum operating current of 80mA/65mA/65mA/65mA. When \overline{CS} is a logical

high, the device is placed in a low power standby mode in which maximum standby current is 7mA. Thus the TMM2016AP is most suitable for use in microcomputer peripheral memory where the low power applications are required. The TMM2016AP is fabricated with ion implanted N channel silicon gate MOS technology for high performance and high reliability.

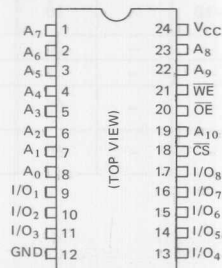
FEATURES

- Access Time and Current

| Parameter Part Number | Access Time (Max.) | Operating Current (Max.) | Standby Current (Max.) |
|--------------------------|-----------------------|--------------------------------|------------------------------|
| TMM2016AP-90 | 90ns | 80mA | 7mA |
| TMM2016AP-10 | 100ns | 65mA | 7mA |
| TMM2016AP-12 | 120ns | 65mA | 7mA |
| TMM2016AP-15 | 150ns | 65mA | 7mA |

- Single 5V Power Supply
- Fully Static Operation
- Power Down Feature: \overline{CS}
- Output Buffer Control: \overline{OE}
- Three Stage Outputs
- All Inputs and Outputs: Directly TTL Compatible
- Inputs Protected: All inputs have protection against static charge.

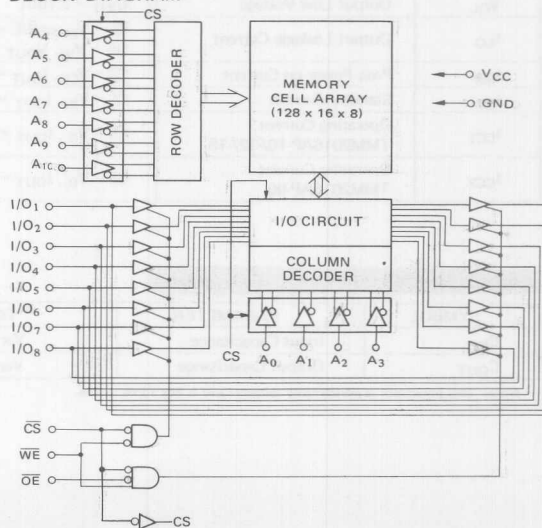
PIN CONNECTION



PIN NAMES

| SYMBOL | NAME |
|--------------------|-----------------------|
| $A_0 \sim A_3$ | Column Address Inputs |
| $A_4 \sim A_{10}$ | Row Address Inputs |
| \overline{CS} | Chip Select Input |
| \overline{WE} | Write Enable Input |
| $I/O_1 \sim I/O_8$ | Data Input/Output |
| \overline{OE} | Output Enable Input |
| V_{CC} | Power (5V) |
| GND | Ground |

BLOCK DIAGRAM



TMM2016AP-90, TMM2016AP-12 **TMM2016AP-10, TMM2016AP-15**

| SYMBOL | PARAMETER | MIN. | TYP. | MAX. | UNIT |
|-------------------|--|------|------|------|----------|
| V_{CC} | Power Supply Voltage | -0.5 | 7.0 | | V |
| V_{IN}, V_{OUT} | Input/Output Voltage | -0.5 | 7.0 | | V |
| $T_{OPR.}$ | Operating Temperature | 0 | 70 | | °C |
| $T_{STG.}$ | Storage Temperature | -55 | 150 | | °C |
| $T_{SOLDER.}$ | Soldering Temperature • Time | 260 | 10 | | °C • sec |
| P_D | Power Dissipation ($T_a = 70^{\circ}\text{C}$) | 1.0 | | | W |

D.C. RECOMMENDED OPERATING CONDITIONS ($T_a = 0 \sim 70^{\circ}\text{C}$)

| SYMBOL | PARAMETER | MIN. | TYP. | MAX. | UNIT |
|----------|--------------------|------|------|--------------|------|
| V_{IH} | Input High Voltage | 2.0 | — | $V_{CC}+1.0$ | V |
| V_{IL} | Input Low Voltage | -0.5 | — | 0.8 | V |
| V_{CC} | Supply Voltage | 4.5 | 5.0 | 5.5 | V |

D.C. CHARACTERISTICS ($T_a = 0 \sim 70^{\circ}\text{C}, V_{CC} = 5.0\text{V} \pm 10\%$)

| SYMBOL | PARAMETER | CONDITIONS | MIN. | TYP. | MAX. | UNIT |
|-----------|---|--|------|------|------|---------------|
| I_{IL} | Input Leakage Current | $V_{IN} = 0\text{V} \sim 5.5\text{V}$ | -10 | — | 10 | μA |
| V_{OH} | Output High Voltage | $I_{OUT} = -1.0\text{mA}$ | 2.4 | — | — | V |
| V_{OL} | Output Low Voltage | $I_{OUT} = 2.1\text{mA}$ | — | — | 0.4 | V |
| I_{LO} | Output Leakage Current | $\overline{CS} = V_{IH}$ or $\overline{WE} = V_{IL}$ or $\overline{OE} = V_{IH}, V_{OUT} = 0\text{V} \sim 5.5\text{V}$ | -10 | — | 10 | μA |
| I_{SBP} | Peak Power-on Current | $\overline{CS} = V_{CC}, I_{OUT} = 0\text{mA}$ | — | — | 30 | mA |
| I_{SB} | Standby Current | $\overline{CS} = V_{IH}, I_{OUT} = 0\text{mA}$ | — | — | 7 | mA |
| I_{CC1} | Operating Current TMM2016AP-10/-12/-15 | $\overline{CS} = V_{IL}, I_{OUT} = 0\text{mA}$ | — | — | 65 | mA |
| I_{CC2} | Operating Current TMM2016AP-90 | $\overline{CS} = V_{IL}, I_{OUT} = 0\text{mA}$ | — | — | 80 | mA |

CAPACITANCE* ($T_a = 25^{\circ}\text{C}, f = 1.0\text{ MHz}$)

| SYMBOL | PARAMETER | CONDITIONS | MAX. | UNIT |
|-----------|--------------------|----------------------|------|------|
| C_{IN} | Input Capacitance | $V_{IN} = 0\text{V}$ | 5 | pF |
| C_{OUT} | Output Capacitance | $V_{IN} = 0\text{V}$ | 10 | pF |

* Note: This parameter is periodically sampled and is not 100% tested.

TMM2016AP-90, TMM2016AP-12 TMM2016AP-10, TMM2016AP-15

A.C. CHARACTERISTICS (T_a = 0 ~ 70°C, V_{CC} = 5V ± 10%)

READ CYCLE

| SYMBOL | PARAMETER | TMM2016AP-90 | | TMM2016AP-10 | | TMM2016AP-12 | | TMM2016AP-15 | | UNIT |
|------------------|---|--------------|------|--------------|------|--------------|------|--------------|------|------|
| | | MIN. | MAX. | MIN. | MAX. | MIN. | MAX. | MIN. | MAX. | |
| t _{RC} | Read Cycle Time | 90 | — | 100 | — | 120 | — | 150 | — | ns |
| t _{ACC} | Address Access Time | — | 90 | — | 100 | — | 120 | — | 150 | ns |
| t _{CO} | Chip Select Access Time | — | 90 | — | 100 | — | 120 | — | 150 | ns |
| t _{OE} | Output Enable Time | — | 35 | — | 35 | — | 50 | — | 55 | ns |
| t _{OH} | Output Data Hold Time from Address Change | 10 | — | 10 | — | 10 | — | 10 | — | ns |
| t _{CLZ} | CS to Output in Low-Z | 10 | — | 10 | — | 10 | — | 10 | — | ns |
| t _{CHZ} | CS to Output in High-Z | — | 40 | — | 40 | — | 40 | — | 55 | ns |
| t _{OLZ} | OE to Output in Low-Z | 5 | — | 5 | — | 5 | — | 5 | — | ns |
| t _{OHZ} | OE to Output in High-Z | — | 35 | — | 35 | — | 35 | — | 50 | ns |
| t _{PU} | Chip Selection to Power Up Time | 0 | — | 0 | — | 0 | — | 0 | — | ns |
| t _{PD} | Chip Deselection to Power Down Time | — | 50 | — | 50 | — | 60 | — | 60 | ns |

WRITE CYCLE

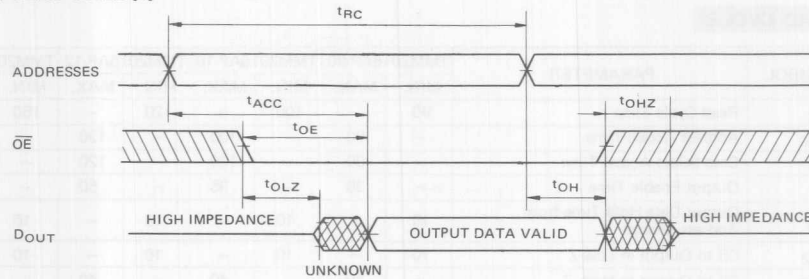
| SYMBOL | PARAMETER | TMM2016AP-90 | | TMM2016AP-10 | | TMM2016AP-12 | | TMM2016AP-15 | | UNIT |
|------------------|--------------------------------|--------------|------|--------------|------|--------------|------|--------------|------|------|
| | | MIN. | MAX. | MIN. | MAX. | MIN. | MAX. | MIN. | MAX. | |
| t _{WC} | Write Cycle Time | 90 | — | 100 | — | 120 | — | 150 | — | ns |
| t _{CW} | Chip Selection to End of Write | 70 | — | 80 | — | 100 | — | 120 | — | ns |
| t _{AS} | Address Set up Time | 20 | — | 20 | — | 20 | — | 20 | — | ns |
| t _{WP} | Write Pulse Width | 60 | — | 70 | — | 85 | — | 100 | — | ns |
| t _{WR} | Write Recovery Time | 0 | — | 0 | — | 0 | — | 0 | — | ns |
| t _{DS} | Data Set up Time | 35 | — | 40 | — | 50 | — | 60 | — | ns |
| t _{DH} | Data Hold Time | 0 | — | 0 | — | 0 | — | 0 | — | ns |
| t _{WLZ} | WE to Output in Low-Z | 5 | — | 5 | — | 5 | — | 5 | — | ns |
| t _{WHZ} | WE to Output in High-Z | — | 25 | — | 30 | — | 35 | — | 50 | ns |

A.C. TEST CONDITIONS

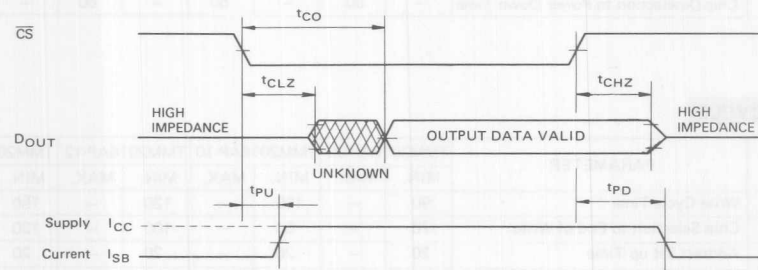
| | |
|-----------------------------------|-------------------------------------|
| Input Pulse Levels | 0 ~ 3.5V |
| Input Rise and Fall Time | 10 ns |
| Input and Output Reference Levels | 1.5V |
| Output Load | 1 TTL Gate & C _L = 100pF |

TIMING WAVEFORMS

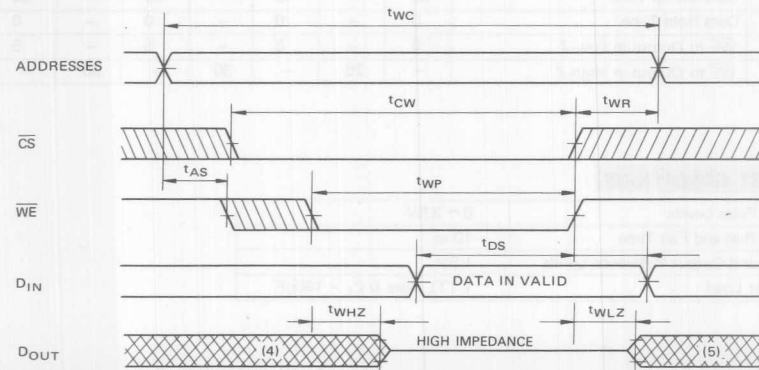
(A) READ CYCLE [1] ⁽¹⁾

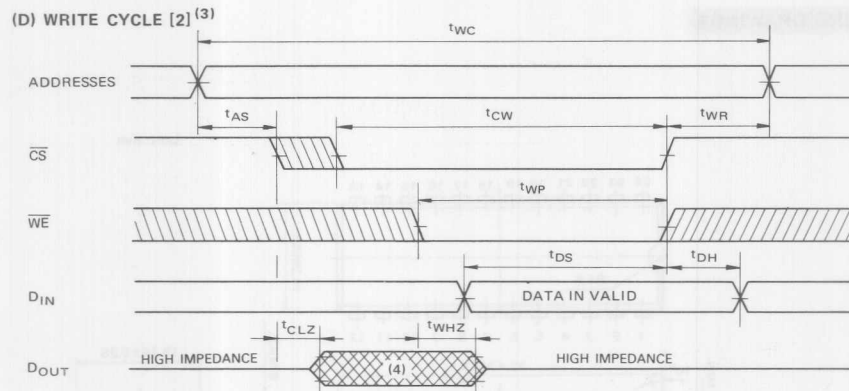


(B) READ CYCLE [2] ⁽¹⁾⁽²⁾



(C) WRITE CYCLE [1] ⁽³⁾





Note: (1) The \overline{WE} is high for read cycle.

Device is continuously selected, $\overline{CS} = V_{IL}$ in read cycle [1].

(2) All addresses are valid prior to or simultaneously with \overline{CS} transitions.

(3) A write occurs during the overlap of low \overline{CS} and low \overline{WE} .

The t_{CW} is specified as the time from the chip selection to end of write in write cycle, and the t_{WP} is specified as the overlap time of low \overline{CS} and low \overline{WE} .

\overline{OE} is allowed to be low or high level in write cycle.

If the \overline{OE} is high, the output buffers remain in a high impedance state in this period.

(4) If the \overline{CS} low transition occurs simultaneously with or latter to the \overline{WE} low transition, the output buffers remain in a high impedance state in this period.

(5) If the \overline{CS} high transition occurs simultaneously with \overline{WE} high transition, the output buffers remain in a high impedance state in this period.

These parameters are specified as follows and measured by using the load shown in Fig. 1.

(A) t_{CLZ} , t_{OLZ} , t_{WLZ} Output Enable Time

(B) t_{CHZ} , t_{OHZ} , t_{WHZ} Output Disable Time

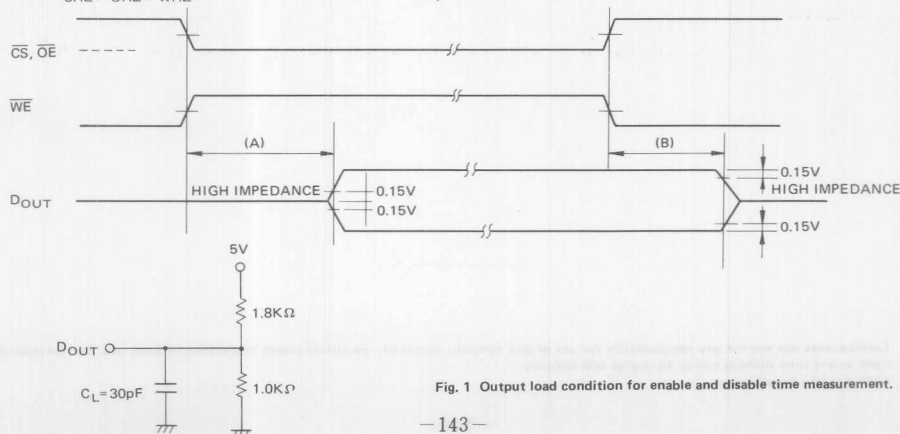
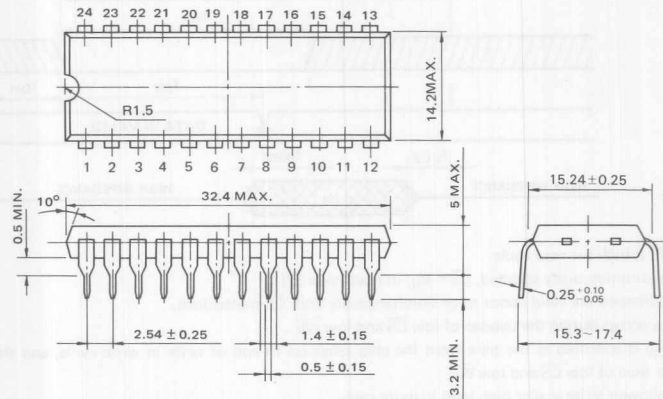


Fig. 1 Output load condition for enable and disable time measurement.

TMM2016AP-90, TMM2016AP-12 TMM2016AP-10, TMM2016AP-15

OUTLINE DRAWINGS

Unit: mm



Note : Each lead pitch is 2.54mm. All leads are located within 0.25mm of their true longitudinal position with respect to No.1 and No.24 leads.

Note: Toshiba does not assume any responsibility for use of any circuitry described; no circuit patent licenses are implied, and Toshiba reserves the right, at any time without notice, to change said circuitry.
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TOSHIBA MOS MEMORY PRODUCTS

2,048 WORD \times 8 BIT STATIC RAM TMM2016BP-90, TMM2016BP-12
SILICON MONOLITHIC
N-CHANNEL SILICON GATE MOS PROCESS TMM2016BP-10, TMM2016BP-15

DESCRIPTION

The TMM2016BP is a 16,384 bits high speed and low power static random access memory organized as 2,048 words by 8 bits and operates from a single 5V supply. Toshiba's high performance device technology provides both high speed and low power features with a maximum access time of 90ns/100ns/120ns/150ns and maximum operating current of 50mA. When \overline{CS} is logical high, the device is

placed in a low power standby mode in which maximum standby current is 5mA. Thus the TMM2016BP is most suitable for use in microcomputer peripheral memory where the low power applications are required. The TMM2016BP is fabricated with ion implanted N channel silicon gate MOS technology for high performance and high reliability.

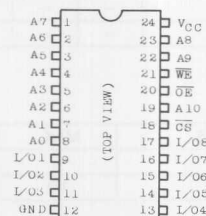
FEATURES

- Access Time and Current

| Part Number | Parameter | Access Time (Max.) | Operating Current (Max.) | Standby Current (Max.) |
|--------------|-----------|--------------------|--------------------------|------------------------|
| TMM2016BP-90 | | 90ns | 50mA | 5mA |
| TMM2016BP-10 | | 100ns | 50mA | 5mA |
| TMM2016BP-12 | | 120ns | 50mA | 5mA |
| TMM2016BP-15 | | 150ns | 50mA | 5mA |

- Single 5V Power Supply
- Fully Static Operation
- Power Down Feature: \overline{CS}
- Output Buffer Control: \overline{OE}
- Three State Outputs
- All Inputs and Outputs: Directly TTL Compatible
- Inputs Protected: All inputs have protection against static charge.

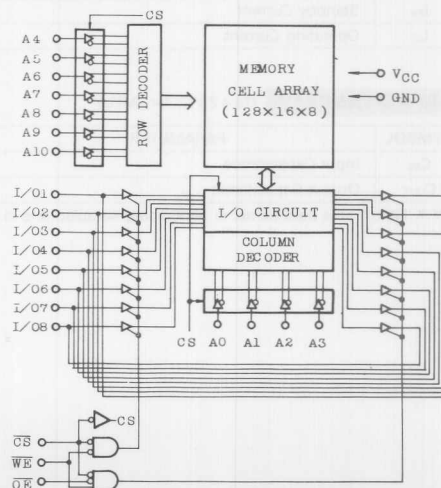
PIN CONNECTION



PIN NAMES

| | |
|------------------------------------|-----------------------|
| A ₀ –A ₃ | Column Address Inputs |
| A ₄ –A ₁₀ | Row Address Inputs |
| \overline{CS} | Chip Select Input |
| \overline{WE} | Write Enable Input |
| I/O ₁ –I/O ₈ | Data Input/Output |
| \overline{OE} | Output Enable Input |
| V _{CC} | Power (5V) |
| GND | Ground |

BLOCK DIAGRAM



TMM2016BP-90, TMM2016BP-12 TMM2016BP-10, TMM2016BP-15

MAXIMUM RATINGS

| SYMBOL | ITEM | RATING | UNIT |
|------------------------------------|------------------------------|----------|--------|
| V _{CC} | Power Supply Voltage | -0.5~7.0 | V |
| V _{IN} , V _{OUT} | Input/Output Voltage | -0.5~7.0 | V |
| T _{OPR} | Operating Temperature | 0~70 | °C |
| T _{STG} | Storage Temperature | -55~150 | °C |
| T _{SOLDER} | Soldering Temperature · Time | 260 · 10 | °C·sec |
| P _D | Power Dissipation (Ta=70°C) | 1.0 | W |

* -3.0V at Pulse width 50ns

D.C. RECOMMENDED OPERATING CONDITIONS (Ta=0~70°C)

| SYMBOL | PARAMETER | MIN. | TYP. | MAX. | UNIT |
|-----------------|----------------------|--------|------|----------------------|------|
| V _{IH} | Input High Voltage | 2.0 | — | V _{CC} +1.0 | V |
| V _{IL} | Input Low Voltage | -0.5** | — | 0.8 | V |
| V _{CC} | Power Supply Voltage | 4.5 | 5.0 | 5.5 | V |

** -3.0V at Pulse width 50ns

D. C. CHARACTERISTICS (Ta=0~70°C, V_{CC}=5V±10%)

| SYMBOL | PARAMETER | CONDITIONS | MIN. | TYP. | MAX. | UNIT |
|------------------|------------------------|--|------|------|------|------|
| I _{IL} | Input Leakage Current | V _{IN} =0V~5.5V | -10 | — | 10 | μA |
| V _{OH} | Output High Voltage | I _{OUT} =-1.0mA | 2.4 | — | — | V |
| V _{OL} | Output Low Voltage | I _{OUT} =4.0mA | — | — | 0.4 | V |
| I _{LO} | Output Leakage Current | CS=V _{IH} or WE=V _{IL} or OE=V _{IH} , V _{OUT} =0V~5.5V | -10 | — | 10 | μA |
| I _{SBP} | Peak Power-on Current | CS=V _{CC} , I _{OUT} =0mA | — | — | 10 | mA |
| I _{SB} | Standby Current | CS=V _{IH} , I _{OUT} =0mA | — | — | 5 | mA |
| I _{CC} | Operating Current | CS=V _{IL} , I _{OUT} =0mA | — | — | 50 | mA |

CAPACITANCE*** (Ta=25°C, f=1MHz)

| SYMBOL | PARAMETER | CONDITIONS | MAX. | UNIT |
|------------------|--------------------|----------------------|------|------|
| C _{IN} | Input Capacitance | V _{IN} =0V | 5 | pF |
| C _{OUT} | Output Capacitance | V _{OUT} =0V | 10 | pF |

*** Note : This parameter is periodically sampled and is not 100% tested.

TMM2016BP-90, TMM2016BP-12 TMM2016BP-10, TMM2016BP-15

A. C. CHARACTERISTICS

(Ta=0~70°C, Vcc=5V±10%)

Read Cycle

| SYMBOL | PARAMETER | TMM2016BP-90 | | TMM2016BP-10 | | TMM2016BP-12 | | TMM2016BP-15 | | UNIT |
|------------------|---|--------------|------|--------------|------|--------------|------|--------------|------|------|
| | | MIN. | MAX. | MIN. | MAX. | MIN. | MAX. | MIN. | MAX. | |
| t _{RC} | Read Cycle Time | 90 | — | 100 | — | 120 | — | 150 | — | ns |
| t _{ACC} | Address Access Time | — | 90 | — | 100 | — | 120 | — | 150 | |
| t _{CO} | Chip Select Access Time | — | 90 | — | 100 | — | 120 | — | 150 | |
| t _{OE} | Output Enable Time | — | 35 | — | 35 | — | 50 | — | 55 | |
| t _{OH} | Output Data Hold Time from Address Change | 10 | — | 10 | — | 10 | — | 10 | — | |
| t _{CLZ} | \overline{CS} to Output in Low-Z | 15 | — | 15 | — | 15 | — | 15 | — | |
| t _{CHZ} | \overline{CS} to Output in High-Z | — | 40 | — | 40 | — | 40 | — | 55 | |
| t _{OLZ} | \overline{OE} to Output in Low-Z | 5 | — | 5 | — | 5 | — | 5 | — | |
| t _{OHZ} | \overline{OE} to Output in High-Z | — | 35 | — | 35 | — | 35 | — | 50 | |
| t _{PU} | Chip Selection to power Up Time | 0 | — | 0 | — | 0 | — | 0 | — | |
| t _{PD} | Chip Deselection to Power Down Time | — | 50 | — | 50 | — | 60 | — | 60 | |

Write Cycle

| SYMBOL | PARAMETER | TMM2016BP-90 | | TMM2016BP-10 | | TMM2016BP-12 | | TMM2016BP-15 | | UNIT |
|------------------|-------------------------------------|--------------|------|--------------|------|--------------|------|--------------|------|------|
| | | MIN. | MAX. | MIN. | MAX. | MIN. | MAX. | MIN. | MAX. | |
| t _{WC} | Write Cycle Time | 90 | — | 100 | — | 120 | — | 150 | — | ns |
| t _{CW} | Chip Selection to End of Write | 60 | — | 70 | — | 85 | — | 100 | — | |
| t _{AS} | Address Set Up Time | 20 | — | 20 | — | 20 | — | 20 | — | |
| t _{WP} | Write Pulse Width | 55 | — | 65 | — | 80 | — | 100 | — | |
| t _{WR} | Write Recovery Time | 0 | — | 0 | — | 0 | — | 0 | — | |
| t _{DS} | Data Set Up Time | 30 | — | 35 | — | 45 | — | 50 | — | |
| t _{DH} | Data Hold Time | 0 | — | 0 | — | 0 | — | 0 | — | |
| t _{WLZ} | \overline{WE} to Output in Low-Z | 5 | — | 5 | — | 5 | — | 5 | — | |
| t _{WHZ} | \overline{WE} to Output in High-Z | — | 25 | — | 30 | — | 35 | — | 50 | |

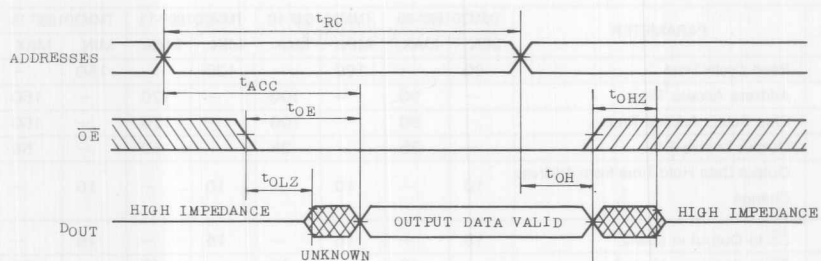
A. C. TEST CONDITIONS

| | |
|--|------------------------------------|
| Input Pulse Levels | 0~3.5V |
| Input Rise and Fall Time | 10ns |
| Input and Output Timing Reference Levels | 1.5V |
| Output Load | 1 TTL Gate & C _L =100pF |

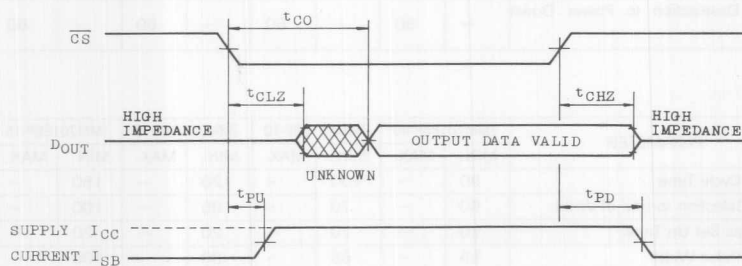
TMM2016BP-90, TMM2016BP-12 TMM2016BP-10, TMM2016BP-15

TIMING WAVEFORMS

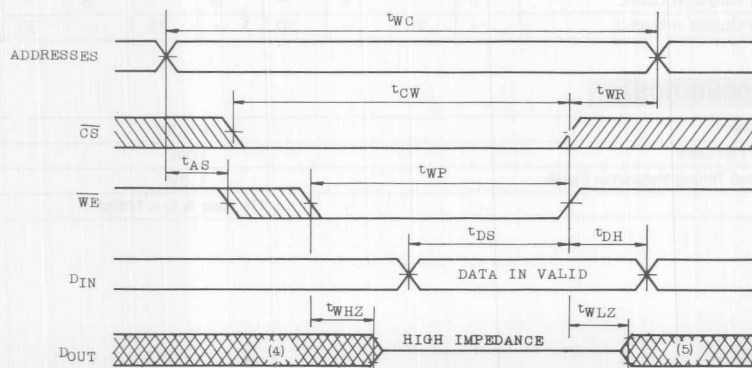
• (A) READ CYCLE [1] (1)



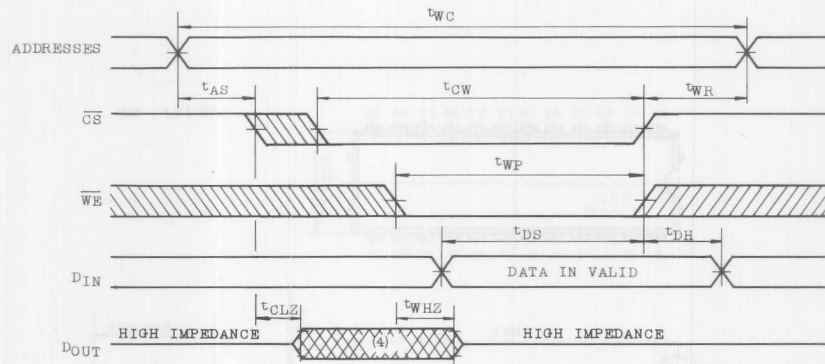
• (B) READ CYCLE [2] (1), (2)



• (C) WRITE CYCLE [1] (3)



● (D) WRITE CYCLE (2) (3)



NOTES:

- (1) The \overline{WE} is high for read cycle.
Device is continuously selected, $\overline{CS} = V_{IL}$ in read cycle (1).
- (2) All addresses are valid prior to or simultaneously with \overline{CS} transitions.
- (3) A write occurs during the overlap of low \overline{CS} and low \overline{WE} .
The t_{CW} is specified as the time from the chip selection to end of write in write cycle, and the t_{WP} is specified as the overlap time of low \overline{CS} and low \overline{WE} .
 \overline{OE} is allowed to be low or high level in write cycle.
If the \overline{OE} is high, the output buffers remain in a high impedance state in this period.
- (4) If the \overline{CS} low transition occurs simultaneously with or latter to the \overline{WE} low transition, the output buffers remain in a high impedance state in this period.
- (5) If the \overline{CS} high transition occurs simultaneously with \overline{WE} high transition, the output buffers remain in a high impedance state in this period.

These parameters are specified as follows and measured by using the load shown in Fig. 1.

(A) $t_{CLZ}, t_{OLZ}, t_{WLZ}$ Output Enable Time

(B) $t_{CHZ}, t_{OHZ}, t_{WHZ}$ Output Disable Time

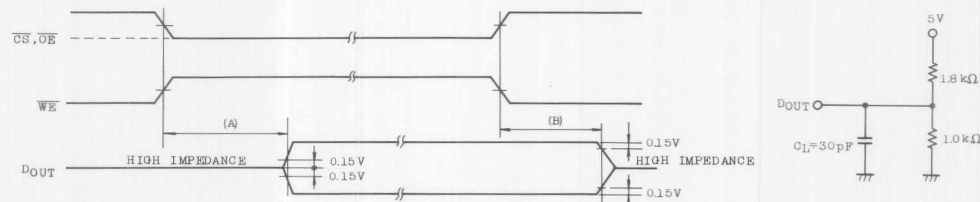
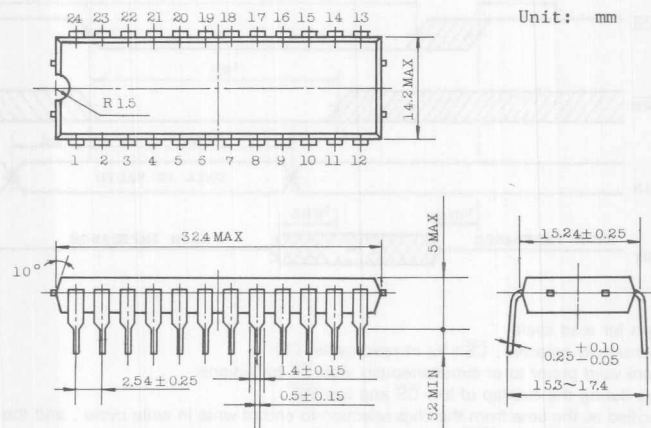


Fig. 1 Output load condition for enable disable time measurement.

TMM2016BP-90, TMM2016BP-12 TMM2016BP-10, TMM2016BP-15

OUTLINE DRAWINGS



NOTES : Each lead pitch is 2.54mm. All leads are located within 0.25mm of their true longitudinal position with respect to No.1 and No.24 leads.

Note : Toshiba does not assume any responsibility for use of any circuitry described ; no circuit patent licenses are implied, and Toshiba reserves the right, at any time without notice, to change said circuitry.
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TOSHIBA MOS MEMORY PRODUCTS

2,048 WORD \times 8 BIT STATIC RAM
SILICON MONOLITHIC
N-CHANNEL SILICON GATE MOS PROCESS

TMM2018D-35, TMM2018D-45
TMM2018D-55

DESCRIPTION

The TMM2018D is a 16,384 bits high speed and low power static random access memory organized as 2,048 words by 8 bits and operates from a single 5V supply. Toshiba's high performance device technology provides both high speed and low power features with a maximum access time of 35ns/45ns/55ns and maximum operating current of 150mA. When \overline{CS} goes high, the device is deselected and placed in a low power standby mode in which

maximum standby current is 20mA.

Thus the TMM2018D is most suitable for use in cache memory and high speed storage. The TMM2018D is offered in 24 pin standard cerdip package with 0.3 inch width for high density assembly.

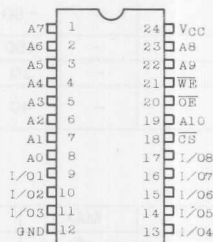
The TMM2018D is fabricated with ion implanted N channel silicon gate MOS technology for high performance and high reliability.

FEATURES

- Fast access time
t_{acc}=35ns : TMM2018D-35
t_{acc}=45ns : TMM2018D-45
t_{acc}=55ns : TMM2018D-55
- Low power dissipation
I_{cc}=150mA
I_{sb}=20mA
- Single 5V power supply
- Fully static operation

- All inputs and outputs
Directly TTL Compatible
- Power down feature : $\overline{CS}=V_{IH}$
- Output buffer control : \overline{OE}
- Three state outputs
- Inputs protected : All inputs protection against static charge.
- Package : 24 pin standard cerdip, 0.3 inch width

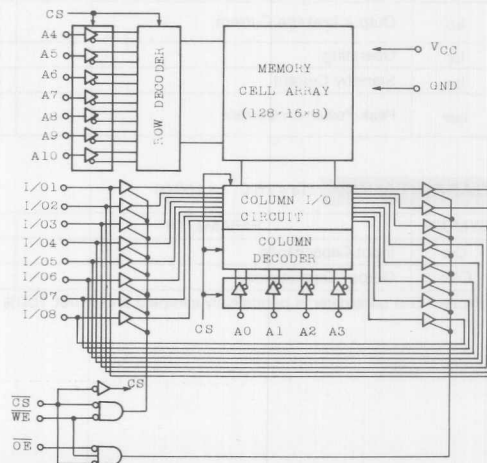
PIN CONNECTION (TOP VIEW)



PIN NAMES

| | |
|------------------------------------|---------------------|
| A ₀ ~A ₁₀ | Address Inputs |
| I/O ₁ ~I/O ₈ | Data Input/Output |
| \overline{CS} | Chip Select Input |
| \overline{WE} | Write Enable Input |
| \overline{OE} | Output Enable Input |
| V _{cc} | Power (+5V) |
| GND | Ground |

BLOCK DIAGRAM



TMM2018D-35, TMM2018D-45 TMM2018D-55

| | | RATING | UNIT |
|---------------------|------------------------------|----------|--------|
| V _{CC} | Power Supply Voltage | -3.5~7.0 | V |
| V _{IN} | Input Voltage | -3.5~7.0 | V |
| V _{I/O} | Input/Output Voltage | -3.5~7.0 | V |
| T _{OPR} | Operating Temperature | 0~70 | °C |
| T _{STG} | Storage Temperature | -55~150 | °C |
| T _{SOLDER} | Soldering Temperature · Time | 260 · 10 | °C·sec |
| P _D | Power Dissipation | 0.9 | W |
| I _{OUT} | D. C. Output Current | 20 | mA |

D. C. RECOMMENDED OPERATING CONDITIONS

| SYMBOL | PARAMETER | MIN. | TYP. | MAX. | UNIT |
|-----------------|----------------------|-------|------|----------------------|------|
| V _{IH} | Input High Voltage | 2.0 | — | V _{CC} +1.0 | V |
| V _{IL} | Input Low Voltage | -3.0* | — | 0.8 | V |
| V _{CC} | Power Supply Voltage | 4.5 | 5.0 | 5.5 | V |

* Pulse Width : 10ns, DC : -0.5V(Min.)

D. C. CHARACTERISTICS

(Ta=0~70°C, V_{CC}=5V±10%)

| SYMBOL | PARAMETER | CONDITIONS | MIN. | MAX. | UNIT |
|------------------|------------------------|---|------|------|------|
| I _{IL} | Input Current | V _{IN} =0~V _{CC} | — | ±10 | μA |
| V _{OH} | Output High Voltage | I _{OH} =-4.0mA | 2.4 | — | V |
| V _{OL} | Output Low Voltage | I _{OL} =8.0mA | — | 0.4 | V |
| I _{LO} | Output Leakage Current | V _{OUT} =0~V _{CC} CS=V _{IH} | — | ±50 | μA |
| I _{CC} | Operating | CS=V _{IL} | — | 150 | mA |
| I _{SB} | Standby Current | CS=V _{IH} | — | 20 | mA |
| I _{SBP} | Peak Power-on Current | CS=V _{CC} V _{CC} =0~5.5V | — | 40 | mA |

CAPACITANCE* (Ta=25°C, f=1MHz)

| SYMBOL | PARAMETER | CONDITIONS | MAX. | UNIT |
|------------------|--------------------|----------------------|------|------|
| C _{IN} | Input Capacitance | V _{IN} =0V | 5 | pF |
| C _{OUT} | Output Capacitance | V _{OUT} =0V | 10 | |

* Note : This parameter is periodically sampled and is not 100% tested.

TMM2018D-35, TMM2018D-45 TMM2018D-55

A. C. CHARACTERISTICS

(Ta=0~70°C, Vcc=5V±10%)

Read Cycle

| SYMBOL | PARAMETER | TMM2018D-35 | | TMM2018D-45 | | TMM2018D-55 | | UNIT |
|------------------|--------------------------------------|-------------|------|-------------|------|-------------|------|------|
| | | MIN. | MAX. | MIN. | MAX. | MIN. | MAX. | |
| t _{RC} | Read Cycle Time | 35 | — | 45 | — | 55 | — | ns |
| t _{ACC} | Address Access Time | — | 35 | — | 45 | — | 55 | |
| t _{CO} | Chip Select Access Time | — | 35 | — | 45 | — | 55 | |
| t _{OE} | Output Enable to Output Valid | — | 20 | — | 20 | — | 25 | |
| t _{CLZ} | Chip Selection to Output in low-Z | — | 5 | — | 5 | — | 5 | |
| t _{CHZ} | Chip Deselection to Output in High-Z | 0 | 20 | 0 | 20 | 0 | 20 | |
| t _{OLZ} | Output Enable to Output in Low-Z | 0 | — | 0 | — | 0 | — | |
| t _{OHZ} | Output Disable to Output in High-Z | 0 | 15 | 0 | 15 | 0 | 20 | |
| t _{OH} | Output Data Hold Time | 5 | — | 5 | — | 5 | — | |
| t _{PU} | Chip Selection to Power Up Time | 0 | — | 0 | — | 0 | — | |
| t _{PD} | Chip Deselection to Power Down Time | — | 30 | — | 30 | — | 30 | |

Write Cycle

| SYMBOL | PARAMETER | TMM2018D-35 | | TMM2018D-45 | | TMM2018D-55 | | UNIT |
|------------------|--------------------------------|-------------|------|-------------|------|-------------|------|------|
| | | MIN. | MAX. | MIN. | MAX. | MIN. | MAX. | |
| t _{WC} | Write Cycle Time | 35 | — | 45 | — | 55 | — | ns |
| t _{CW} | Chip Selection to End of Write | 30 | — | 40 | — | 50 | — | |
| t _{AS} | Address Set Up Time | 0 | — | 0 | — | 0 | — | |
| t _{WP} | Write Pulse Width | 30 | — | 35 | — | 40 | — | |
| t _{WR} | Write Recovery Time | 0 | — | 0 | — | 0 | — | |
| t _{WLZ} | WE to Output in Low-Z | 0 | — | 0 | — | 0 | — | |
| t _{WHZ} | WE to Output in High-Z | 0 | 15 | 0 | 15 | 0 | 20 | |
| t _{DS} | Data Set Up Time | 15 | — | 20 | — | 20 | — | |
| t _{DH} | Data Hold Time | 0 | — | 0 | — | 0 | — | |

A. C. TEST CONDITIONS

| | |
|--|------------|
| Input Pulse Levels | 0~3.5V |
| Input Rise and Fall Times | 5ns |
| Input and Output Timing Reference Levels | 1.5V |
| Output Load | See Fig. 1 |

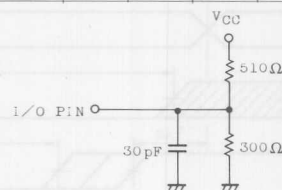
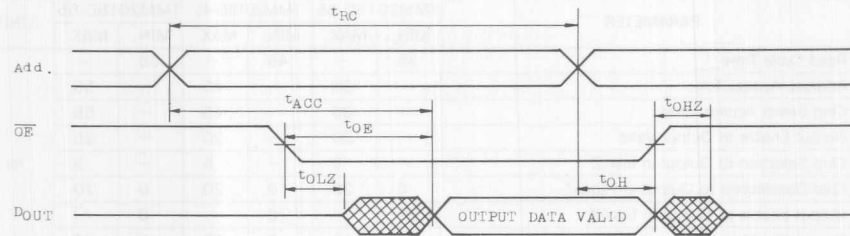


Fig.1 Output Load

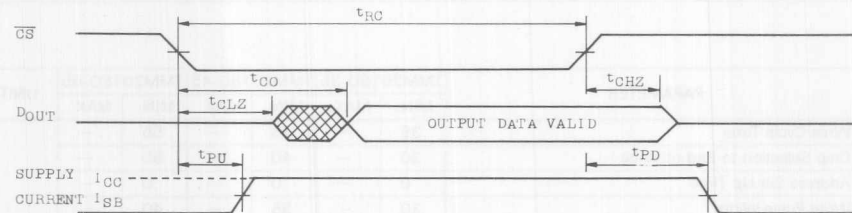
TMM2018D-35, TMM2018D-45 TMM2018D-55

TIMING WAVEFORMS

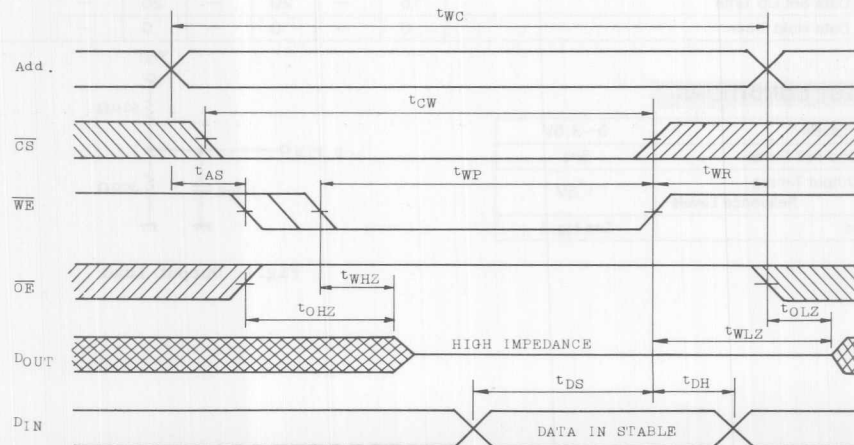
- Read Cycle 1. ($\overline{WE}=V_{IH}$, $\overline{CS}=V_{IL}$)



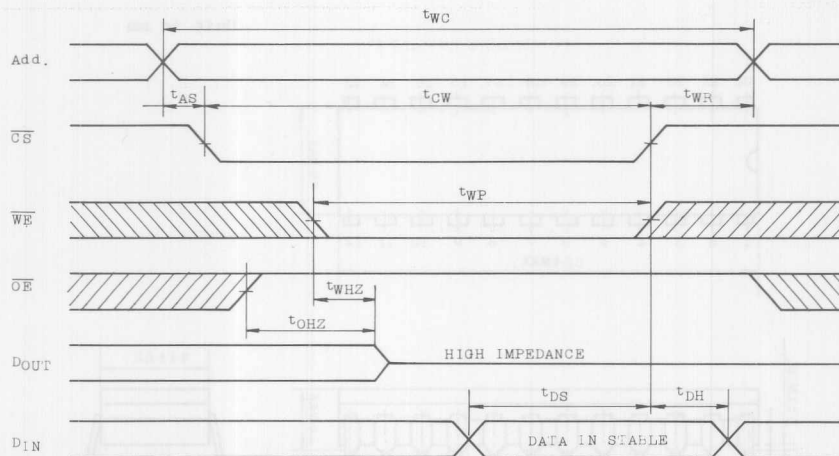
- Read Cycle 2. ($\overline{WE}=V_{IH}$, $\overline{OE}=V_{IL}$)



- Write Cycle 1.



● Write Cycle 2.



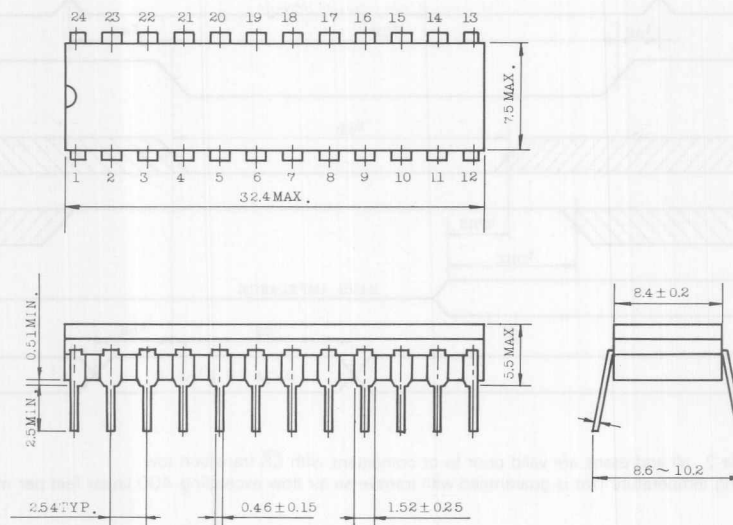
Note :

1. In read cycle 2, all addresses are valid prior to or coincident with \overline{CS} transition low.
2. The operating temperature (T_a) is guaranteed with transverse air flow exceeding 400 linear feet per minute.

TMM2018D-35, TMM2018D-45 TMM2018D-55

OUTLINE DRAWINGS

Unit in mm



Note : Each lead pitch is 2.54mm. All leads are located within 0.25mm of their longitudinal position with respect to No.1 and No.24 leads.

Note : Toshiba does not assume any responsibility for use of any circuitry described ; no circuit patent licenses are implied, and Toshiba reserves the right, at any time without notice, to change said circuitry.
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**TMM2068D-35, TMM2068D-45
TMM2068D-55**

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TMM2068D-35, TMM2068D-45 TMM2068D-55

MAXIMUM RATINGS

| SYMBOL | ITEM | RATING | UNIT |
|---------------------|------------------------------|----------|--------|
| V _{CC} | Power Supply Voltage | -3.5~7.0 | V |
| V _{IN} | Input Voltage | -3.5~7.0 | V |
| V _{I/O} | Input/Output Voltage | -3.5~7.0 | V |
| T _{OPR} | Operating Temperature | 0~70 | °C |
| T _{STRG} | Storage Temperature | -55~150 | °C |
| T _{SOLDER} | Soldering Temperature · Time | 260 · 10 | °C·sec |
| P _D | Power Dissipation | 0.9 | W |
| I _{OUT} | D. C. Output Current | 20 | mA |

D. C. RECOMMENDED OPERATING CONDITIONS

| SYMBOL | PARAMETER | MIN. | TYP. | MAX. | UNIT |
|-----------------|----------------------|-------|------|-----------------------|------|
| V _{IH} | Input High Voltage | 2.0 | — | V _{CC} + 1.0 | V |
| V _{IL} | Input Low Voltage | -3.0* | — | 0.8 | V |
| V _{CC} | Power Supply Voltage | 4.5 | 5.0 | 5.5 | V |

* Pulse Width : 10ns, DC : -0.5V(Min.)

D. C. CHARACTERISTICS (Ta=0~70°C, V_{CC}=5V±10%)

| SYMBOL | PARAMETER | CONDITIONS | MIN. | MAX. | UNIT |
|------------------|------------------------|---|---------------|-----------------|------|
| I _{IL} | Input Leakage Current | V _{IN} =0~V _{CC} | — | ±10 | μA |
| V _{OH} | Output High Voltage | I _{OH} =-4.0mA | 2.4 | — | V |
| V _{OL} | Output Low Voltage | I _{OL} =0.8mA | — | 0.4 | V |
| I _{LO} | Output Leakage Current | V _{OUT} =0~V _{CC} CS=V _{IH} | — | ±50 | μA |
| I _{CC} | Operating Current | CS=V _{IL} | -35 -45/55 | — 150 120 | mA |
| I _{SB} | Standby Current | CS=V _{IH} | — | 20 | mA |
| I _{SBP} | Peak Power-on Current | CS=V _{CC} V _{CC} =0~5.5V | — | 40 | mA |

CAPACITANCE* (Ta=25°C, f=1MHz)

| SYMBOL | PARAMETER | CONDITIONS | MAX. | UNIT |
|------------------|--------------------|----------------------|------|------|
| C _{IN} | Input Capacitance | V _{IN} =0V | 5 | pF |
| C _{OUT} | Output Capacitance | V _{OUT} =0V | 10 | |

* Note : This parameter is periodically sampled and is not 100% tested.

TMM2068D-35, TMM2068D-45 TMM2068D-55

A. C. CHARACTERISTICS (Ta=0~70°C, Vcc=5V±10%)

Read Cycle

| SYMBOL | PARAMETER | TMM2068D-35 | | TMM2068D-45 | | TMM2068D-55 | | UNIT |
|------------------|--------------------------------------|-------------|------|-------------|------|-------------|------|------|
| | | MIN. | MAX. | MIN. | MAX. | MIN. | MAX. | |
| t _{RC} | Read Cycle Time | 35 | — | 45 | — | 55 | — | ns |
| t _{ACC} | Address Access Time | — | 35 | — | 45 | — | 55 | |
| t _{CO} | Chip Select Access Time | — | 35 | — | 45 | — | 55 | |
| t _{CLZ} | Chip Selection to Output in Low-Z | 5 | — | 5 | — | 5 | — | |
| t _{CHZ} | Chip Deselection to Output in High-Z | 0 | 20 | 0 | 20 | 0 | 20 | |
| t _{OH} | Output Data Hold Time | 5 | — | 5 | — | 5 | — | |
| t _{PU} | Chip Selection to Power Up Time | 0 | — | 0 | — | 0 | — | |
| t _{PD} | Chip Deselection to Power Down Time | — | 30 | — | 30 | — | 30 | |

Write Cycle

| SYMBOL | PARAMETER | TMM2068D-35 | | TMM2068D-45 | | TMM2068D-55 | | UNIT |
|------------------|--------------------------------|-------------|------|-------------|------|-------------|------|------|
| | | MIN. | MAX. | MIN. | MAX. | MIN. | MAX. | |
| t _{WC} | Write Cycle Time | 35 | — | 45 | — | 55 | — | ns |
| t _{CW} | Chip Selection to End of Write | 30 | — | 40 | — | 50 | — | |
| t _{AS} | Address Set Up Time | 0 | — | 0 | — | 0 | — | |
| t _{WP} | Write Pulse Width | 30 | — | 35 | — | 40 | — | |
| t _{WR} | Write Recovery Time | 0 | — | 0 | — | 0 | — | |
| t _{WLZ} | WE to Output in Low-Z | 0 | — | 0 | — | 0 | — | |
| t _{WHZ} | WE to Output in High-Z | 0 | 15 | 0 | 15 | 0 | 20 | |
| t _{DS} | Data Set Up Time | 15 | — | 20 | — | 20 | — | |
| t _{DH} | Data Hold Time | 0 | — | 0 | — | 0 | — | |

A. C. TEST CONDITIONS

| | |
|--|------------|
| Input Pulse Levels | 0~3.5V |
| Input Rise and Fall Times | 5ns |
| Input and Output Timing Reference Levels | 1.5V |
| Output Load | See Fig. 1 |

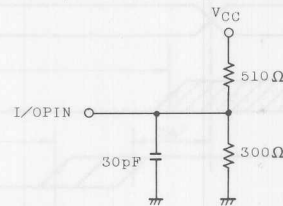


Fig.1 Output Load

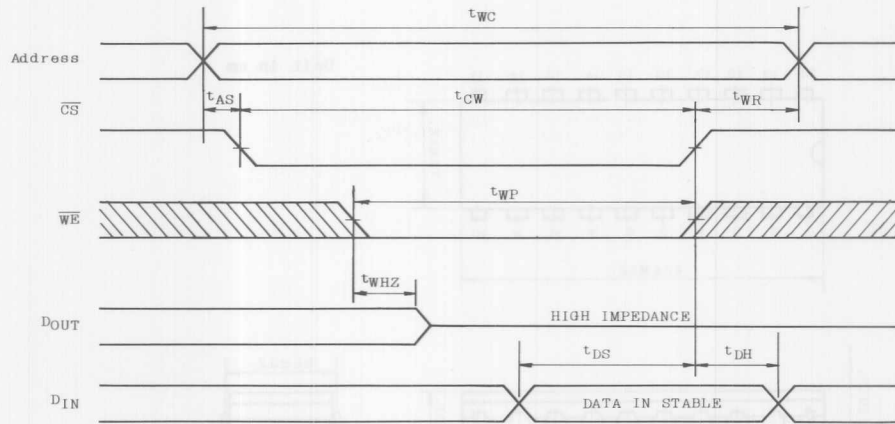
* Note : In all condition, t_{CHZ} max is less than t_{CLZ} min both for a given device and from device to device.

-
- The diagram shows the relationship between the Address bus and the Data Output (DOUT) bus. The Address bus signal is a pulse with a total duration of t_{RC} . The Data Output (DOUT) signal becomes valid at the start of the Address pulse and remains valid for a duration of t_{ACC} after the Address pulse ends. The time from the end of the Address pulse to the DOUT signal becoming invalid is labeled t_{OH} . The DOUT signal is shown as a pulse with a hatched pattern, labeled "OUTPUT DATA VALID".

-

-
- The diagram illustrates the timing relationships for a 256K DRAM. The signals and their timing parameters are as follows:
- Address:** The address bus signal. Timing parameters include t_{WC} (Write Cycle time) and t_{CW} (Column Access time).
 - \overline{CS} (Chip Select):** The chip select signal. Timing parameters include t_{AS} (Access time from \overline{CS} to data) and t_{WR} (Write recovery time).
 - \overline{WE} (Write Enable):** The write enable signal. Timing parameters include t_{WP} (Write pulse width) and t_{WHZ} (Write high impedance time).
 - D_{OUT} (Data Output):** The data output bus. It shows a period of HIGH IMPEDANCE during the write cycle, with timing parameters t_{WLZ} (Write low impedance time) and t_{DS} (Data setup time).
 - D_{IN} (Data Input):** The data input bus. It shows a period of DATA IN STABLE during the write cycle, with timing parameters t_{DH} (Data hold time) and t_{WC} (Write cycle time).

● Write Cycle 2.

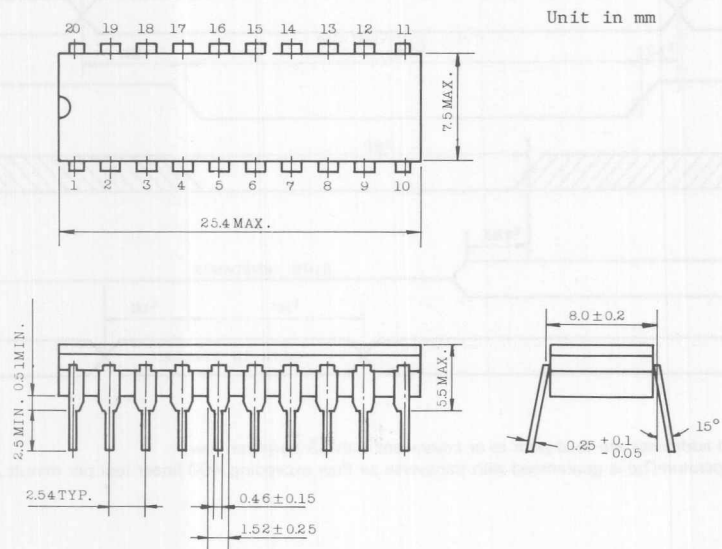


Note :

1. In read cycle 2, all addresses are valid prior to or coincident with \overline{CS} transition low.
2. The operating temperature (T_a) is guaranteed with transverse air flow exceeding 400 linear feet per minute.

TMM2068D-35, TMM2068D-45 TMM2068D-55

OUTLINE DRAWINGS



Note : Each lead pitch is 2.54mm.
All leads are located within 0.25mm of their longitudinal position with respect to No. 1 and No. 20 leads.

Note : Toshiba does not assume any responsibility for use of any circuitry described ; no circuit patent licenses are implied, and Toshiba reserves the right, at any time without notice, to change said circuitry.
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**TMM2078D-35, TMM2078D-45
TMM2078D-55**

PRELIMINARY

The TMM2078D is a 16,384 bits high speed and low power static random access memory organized as 4,096 words by 4 bits and operates from a single 5V supply. Toshiba's high performance device technology provides both high speed and low power features with a maximum access time of 35ns/45ns/55ns and maximum operating current of 150mA/120mA/120mA. When \overline{CS} goes high, the device is deselected and placed in a low power standby mode.

- Fast access time
t_{ACC} = 35ns : TMM2078D-35
t_{ACC} = 45ns : TMM2078D-45
t_{ACC} = 55ns : TMM2078D-55
- Low power dissipation
I_{CC} = 150mA : TMM2078D-35
I_{CC} = 120mA : TMM2078D-45/55
I_{SB} = 20mA
- Single 5V power supply

Thus the TMM2078D is most suitable for use in cache memory and high speed storage. The TMM2078D is offered in a 22 pin standard cerdip package with 0.3 inch width for high density assembly.

The TMM2078D is fabricated with ion implanted N channel silicon gate MOS technology for high performance and high reliability.

| | | | |
|-----------------|----|----|-----------------|
| A7 | 1 | 21 | V _{CC} |
| A6 | 2 | 21 | A8 |
| A5 | 3 | 20 | A9 |
| A4 | 4 | 19 | A10 |
| A3 | 5 | 18 | A11 |
| A2 | 6 | 17 | N.C. |
| A1 | 7 | 16 | 1/01 |
| A0 | 8 | 15 | L/02 |
| \overline{OE} | 9 | 14 | 1/03 |
| \overline{CS} | 10 | 13 | L/04 |
| GND | 11 | 12 | \overline{WE} |

| | |
|------------------------------------|---------------------|
| A ₀ ~A ₁₁ | Address Inputs |
| I/O ₁ ~I/O ₄ | Data Input/Output |
| CS | Chip Select Input |
| WE | Write Enable Input |
| OE | Output Enable Input |
| V _{cc} | Power(+5V) |
| GND | Ground |
| N. C. | No Connection |

TMM2078D-35, TMM2078D-45 TMM2078D-55

| | | | |
|---------------------|------------------------------|----------|--------|
| V _{CC} | Power Supply Voltage | -3.5~7.0 | V |
| V _{IN} | Input Voltage | -3.5~7.0 | V |
| V _{I/O} | Input/Output Voltage | -3.5~7.0 | V |
| T _{OPR} | Operating Temperature | 0~70 | °C |
| T _{STRG} | Storage Temperature | -55~150 | °C |
| T _{SOLDER} | Soldering Temperature · Time | 260 · 10 | °C·sec |
| P _D | Power Dissipation | 0.9 | W |
| I _{OUT} | D. C. Output Current | 20 | mA |

D. C. RECOMMENDED OPERATING CONDITIONS

| SYMBOL | PARAMETER | MIN. | TYP. | MAX. | UNIT |
|-----------------|----------------------|-------|------|----------------------|------|
| V _{IH} | Input High Voltage | 2.0 | — | V _{CC} +1.0 | V |
| V _{IL} | Input Low Voltage | -3.0* | — | 0.8 | V |
| V _{CC} | Power Supply Voltage | 4.5 | 5.0 | 5.5 | V |

* Pulse Width : 10ns, DC : -0.5V(Min.)

D. C. CHARACTERISTICS (Ta=0~70°C, V_{CC}=5V±10%)

| SYMBOL | PARAMETER | CONDITIONS | MIN. | MAX. | UNIT |
|------------------|------------------------|---|---------------|-----------------|------|
| I _{IL} | Input Leakage Current | V _{IN} =0~V _{CC} | — | ±10 | μA |
| V _{OH} | Output High Voltage | I _{OH} =-4.0mA | 2.4 | — | V |
| V _{OL} | Output Low Voltage | I _{OL} =0.8mA | — | 0.4 | V |
| I _{LO} | Output Leakage Current | V _{OUT} =0~V _{CC} CS=V _{IH} | — | ±50 | μA |
| I _{CC} | Operating Current | CS=V _{IL} | -35 -45/55 | — 150 120 | mA |
| I _{SB} | Standby Current | CS=V _{IH} | — | 20 | mA |
| I _{SBP} | Peak Power-on Current | CS=V _{CC} V _{CC} =0~5.5V | — | 40 | mA |

CAPACITANCE* (Ta=25°C, f=1MHz)

| SYMBOL | PARAMETER | CONDITIONS | MAX. | UNIT |
|------------------|--------------------|----------------------|------|------|
| C _{IN} | Input Capacitance | V _{IN} =0V | 5 | pF |
| C _{OUT} | Output Capacitance | V _{OUT} =0V | 10 | |

* Note : This parameter is periodically sampled and is not 100% tested.

TMM2078D-35, TMM2078D-45 TMM2078D-55

A. C. CHARACTERISTICS

(Ta=0~70°C, Vcc=5V±10%)

Read Cycle

| SYMBOL | PARAMETER | TMM2078D-35 | | TMM2078D-45 | | TMM2078D-55 | | UNIT |
|------------------|--------------------------------------|-------------|------|-------------|------|-------------|------|------|
| | | MIN. | MAX. | MIN. | MAX. | MIN. | MAX. | |
| t _{RC} | Read Cycle Time | 35 | — | 45 | — | 55 | — | ns |
| t _{ACC} | Address Access Time | — | 35 | — | 45 | — | 55 | |
| t _{CO} | Chip Select Access Time | — | 35 | — | 45 | — | 55 | |
| t _{OE} | Output Enable to Output Valid | — | 20 | — | 20 | — | 25 | |
| t _{CLZ} | Chip Selection to Output in Low-Z | 5 | — | 5 | — | 5 | — | |
| t _{CHZ} | Chip Deselection to Output in High-Z | 0 | 20 | 0 | 20 | 0 | 20 | |
| t _{OLZ} | Output Enable to Output in Low-Z | 0 | — | 0 | — | 0 | — | |
| t _{OHZ} | Output Disable to Output in High-Z | 0 | 15 | 0 | 15 | 0 | 20 | |
| t _{OH} | Output Data Hold Time | 5 | — | 5 | — | 5 | — | |
| t _{PU} | Chip Selection to Power Up Time | 0 | — | 0 | — | 0 | — | |
| t _{PD} | Chip Deselection to Power Down Time | — | 30 | — | 30 | — | 30 | |

Write Cycle

| SYMBOL | PARAMETER | TMM2078D-35 | | TMM2078D-45 | | TMM2078D-55 | | UNIT |
|------------------|--------------------------------|-------------|------|-------------|------|-------------|------|------|
| | | MIN. | MAX. | MIN. | MAX. | MIN. | MAX. | |
| t _{WC} | Write Cycle Time | 35 | — | 45 | — | 55 | — | ns |
| t _{CW} | Chip Selection to End of Write | 30 | — | 40 | — | 50 | — | |
| t _{AS} | Address Set Up Time | 0 | — | 0 | — | 0 | — | |
| t _{WP} | Write Pulse Width | 30 | — | 35 | — | 40 | — | |
| t _{WR} | Write Recovery Time | 0 | — | 0 | — | 0 | — | |
| t _{WLZ} | WE to Output in Low-Z | 0 | — | 0 | — | 0 | — | |
| t _{WHZ} | WE to Output in High-Z | 0 | 15 | 0 | 15 | 0 | 20 | |
| t _{DS} | Data Set Up Time | 15 | — | 20 | — | 20 | — | |
| t _{DH} | Data Hold Time | 0 | — | 0 | — | 0 | — | |

A. C. TEST CONDITIONS

| | |
|--|------------|
| Input Pulse Levels | 0~3.5V |
| Input Rise and Fall Times | 5ns |
| Input and Output Timing Reference Levels | 1.5V |
| Output Load | See Fig. 1 |

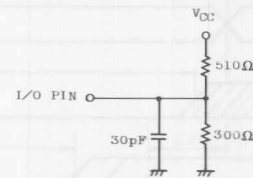


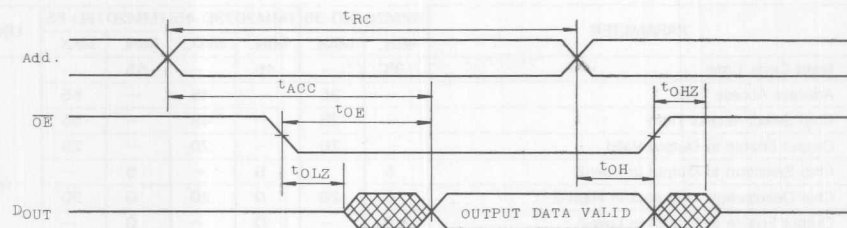
Fig.1 Output Load

* Note : In all condition, t_{CHZ} max is less than t_{CLZ} min both for a given device and from device to device.

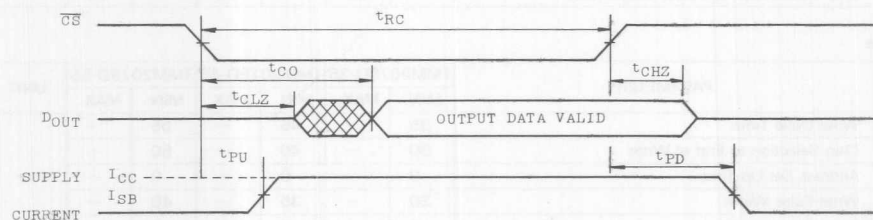
TMM2078D-35, TMM2078D-45 TMM2078D-55

TIMING WAVEFORMS

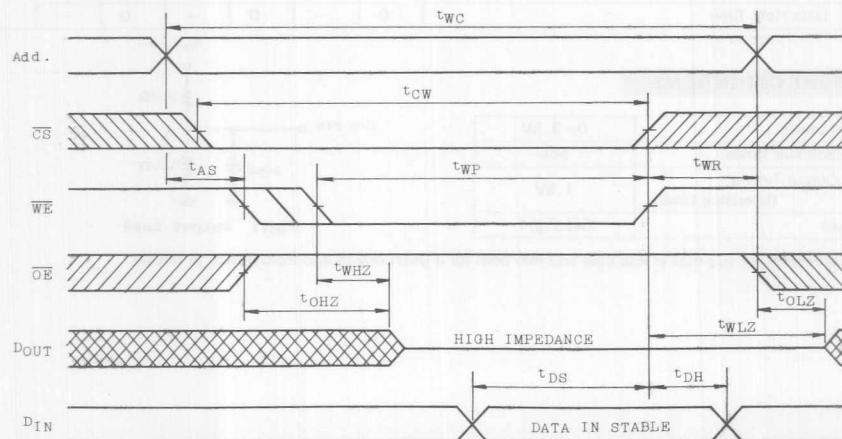
- Read Cycle 1. ($\overline{WE}=V_{IH}$, $\overline{CS}=V_{IL}$)



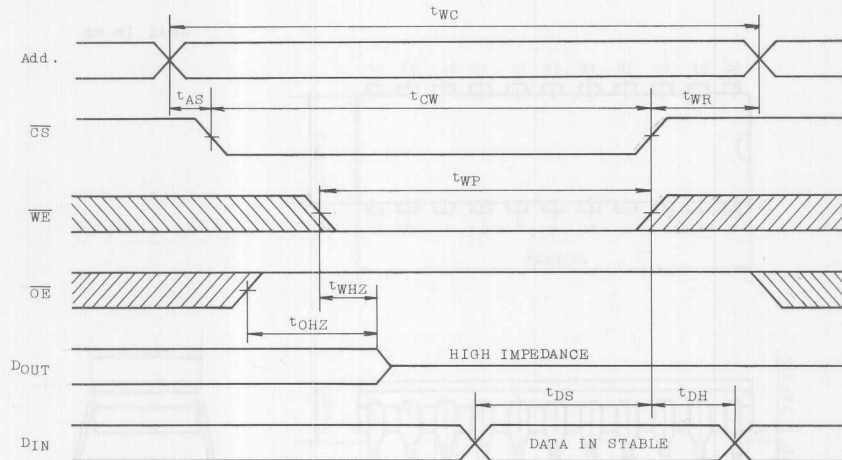
- Read Cycle 2. ($\overline{WE}=V_{IH}$, $\overline{OE}=V_{IL}$)



- Write Cycle 1.



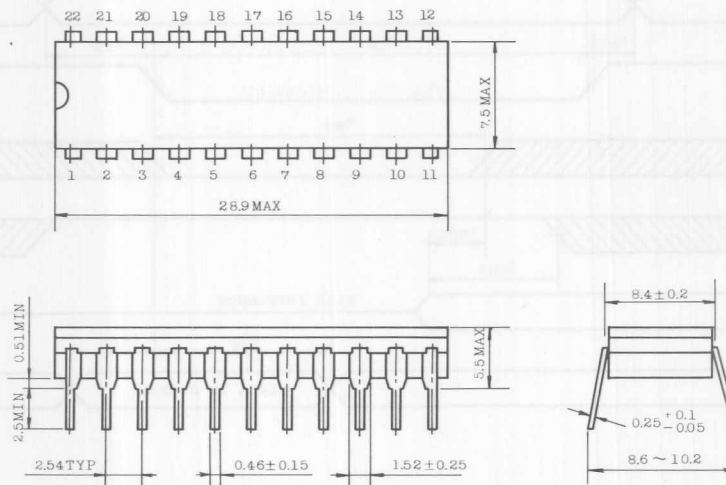
● Write Cycle 2.



Note :

1. In read cycle 2, all addresses are valid prior to or coincident with \overline{CS} transition low.
2. The operating temperature (T_a) is guaranteed with transverse air flow exceeding 400 linear feet per minute.

Unit in mm



Note : Each lead pitch is 2.54mm. All leads are located within 0.25mm of their longitudinal position with respect to No.1 and No.22 Leads.

Note : Toshiba does not assume any responsibility for use of any circuitry described ; no circuit patent licenses are implied, and Toshiba reserves the right, at any time without notice, to change said circuitry.
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TOSHIBA MOS MEMORY PRODUCTS

8,192 WORD \times 8 BIT STATIC RAM
N-CHANNEL SILICON GATE MOS

TMM2063P-10, TMM2063P-12
TMM2063P-15

DESCRIPTION

The TMM2063P is a 65,536 bits high speed and low power static random access memory organized as 8,192 words by 8 bits and operates from a single 5V supply. Toshiba's high performance device technology provides both high speed and low power features with a maximum access time of 100ns/120ns/150ns and maximum operating current of 80mA. When CS_1 is a logical high or CS_2 is a logical low, the device is placed in a low power standby

mode in which maximum standby current is 10mA. Thus the TMM2063P is most suitable for use in microcomputer peripheral memory where the low power applications are required, moreover, suitable for use in high density assembly as 0.3 inch width package is use for. The TMM2063P is fabricated with ion implanted N channel silicon gate MOS technology for high performance and high reliability.

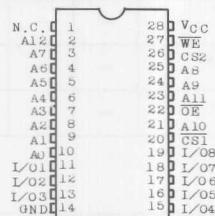
FEATURES

- Access Time and Current

| Part Number | Parameter | Access Time (Max.) | Operating Current (Max.) | Standby Current (Max.) |
|-------------|-----------|--------------------|--------------------------|------------------------|
| TMM2063P-10 | | 100ns | 80mA | 10mA |
| TMM2063P-12 | | 120ns | 80mA | 10mA |
| TMM2063P-15 | | 150ns | 80mA | 10mA |

- High Density Assembly Capability : 0.3 inch width package (28 pin plastic DIP)

PIN CONNECTION

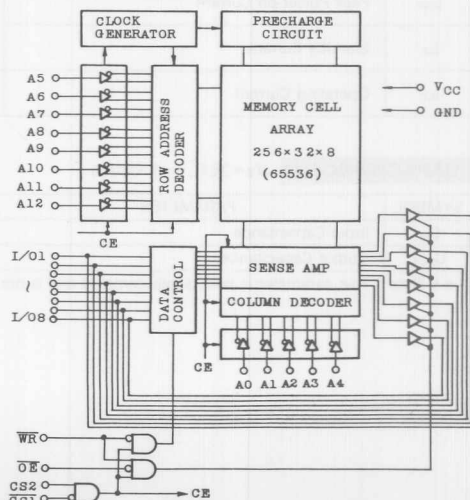


PIN NAMES

| SYMBOL | NAME |
|------------------------------------|-----------------------|
| A ₀ ~A ₄ | Column Address Inputs |
| A ₅ ~A ₁₂ | Row Address Inputs |
| CS ₁ , CS ₂ | Chip Select Inputs |
| WE | Write Enable Input |
| I/O ₁ ~I/O ₈ | Data Input/Output |
| OE | Output Enable Input |
| V _{cc} | Power (+5V) |
| GND | Ground |
| N. C. | No Connection |

- Single 5V Power Supply
- Fully Static Operation
- Power Down Feature : CS_1 , CS_2
- Output Buffer Control : \overline{OE}
- Three State Outputs
- All Inputs and Outputs : Directly TTL Compatible
- Inputs Protected : All inputs have protection against static charge.

BLOCK DIAGRAM



TMM2063P-10, TMM2063P-12 TMM2063P-15

MAXIMUM RATINGS

| SYMBOL | ITEM | RATING | UNIT |
|------------------------------------|------------------------------|----------|--------|
| V _{CC} | Power Supply Voltage | -0.5~7.0 | V |
| V _{IN} , V _{OUT} | Input/Output Voltage | -0.5~7.0 | V |
| T _{OPR} | Operating Temperature | 0~70 | °C |
| T _{STG} | Storage Temperature | -55~150 | °C |
| T _{SOLDER} | Soldering Temperature · Time | 260 · 10 | °C·sec |
| P _D | Power Dissipation (Ta=70°C) | 0.8 | W |

* -3.0V at Pulse width 50ns

D. C. RECOMMENDED OPERATING CONDITIONS (Ta=0~70°C)

| SYMBOL | PARAMETER | MIN. | TYP. | MAX. | UNIT |
|-----------------|--------------------|--------|------|----------------------|------|
| V _{IH} | Input High Voltage | 2.0 | — | V _{CC} +1.0 | V |
| V _{IL} | Input Low Voltage | -0.5** | — | 0.8 | V |
| V _{CC} | Supply Voltage | 4.5 | 5.0 | 5.5 | V |

** -3.0V at Pulse width 50ns

D. C. CHARACTERISTICS (Ta=0~70°C, V_{CC}=5V±10%)

| SYMBOL | PARAMETER | CONDITIONS | MIN. | TYP. | MAX. | UNIT |
|------------------|------------------------|--|------|------|------|------|
| I _{IL} | Input Leakage Current | V _{IN} =0V~5.5V | -10 | — | 10 | μA |
| V _{OH} | Output High Voltage | I _{OUT} =-1.0mA | 2.4 | — | — | V |
| V _{OL} | Output Low Voltage | I _{OUT} =2.1mA | — | — | 0.4 | V |
| I _{LO} | Output Leakage Current | CS ₁ =V _{IH} or CS ₂ =V _{IL} or WE=V _{IL} or OE=V _{IH} , V _{OUT} =0V~5.5V | -10 | — | 10 | μA |
| I _{SBP} | Peak Power-on Current | CS ₁ =V _{CC} , CS ₂ =0V I _{OUT} =0mA | — | — | 20 | mA |
| I _{SB} | Standby Current | CS ₁ =V _{IH} or CS ₂ =V _{IL} , I _{OUT} =0mA | — | — | 10 | mA |
| I _{CC} | Operating Current | CS ₁ =V _{IL} , CS ₂ =V _{IH} , I _{OUT} =0mA | — | — | 80 | mA |

CAPACITANCE*** (Ta=25°C, f=1.0MHz)

| SYMBOL | PARAMETER | CONDITIONS | MAX. | UNIT |
|------------------|--------------------|---------------------|------|------|
| C _{IN} | Input Capacitance | V _{IN} =0V | 5 | pF |
| C _{OUT} | Output Capacitance | V _{IN} =0V | 10 | pF |

*** Note : This parameter is periodically sampled and is not 100% tested.

TMM2063P-10, TMM2063P-12 TMM2063P-15

A. C. CHARACTERISTICS

(Ta=0~70°C, Vcc=5V±10%)

Read Cycle

| SYMBOL | PARAMETER | TMM2063P-10 | | TMM2063P-12 | | TMM2063P-15 | | UNIT |
|------------------|--|-------------|------|-------------|------|-------------|------|------|
| | | MIN. | MAX. | MIN. | MAX. | MIN. | MAX. | |
| t _{RC} | Read Cycle Time | 100 | — | 120 | — | 150 | — | ns |
| t _{ACC} | Address Access Time | — | 100 | — | 120 | — | 150 | |
| t _{CO1} | CS ₁ Access Time | — | 100 | — | 120 | — | 150 | |
| t _{CO2} | CS ₂ Access Time | — | 100 | — | 120 | — | 150 | |
| t _{OE} | OE Access Time | — | 40 | — | 50 | — | 60 | |
| t _{OH} | Output Data Hold Time from Address Change | 10 | — | 10 | — | 10 | — | |
| t _{CLZ} | CS ₁ or CS ₂ to Output in Low-Z | 10 | — | 10 | — | 10 | — | |
| t _{CHZ} | CS ₁ or CS ₂ to Output in High-Z | — | 40 | — | 40 | — | 55 | |
| t _{OLZ} | OE to Output in Low-Z | 5 | — | 5 | — | 5 | — | |
| t _{OHZ} | OE to Output in High-Z | — | 35 | — | 35 | — | 50 | |
| t _{PU} | Chip Selection to Power Up Time | 0 | — | 0 | — | 0 | — | |
| t _{PD} | Chip Deselection to Power Down Time | — | 50 | — | 60 | — | 60 | |

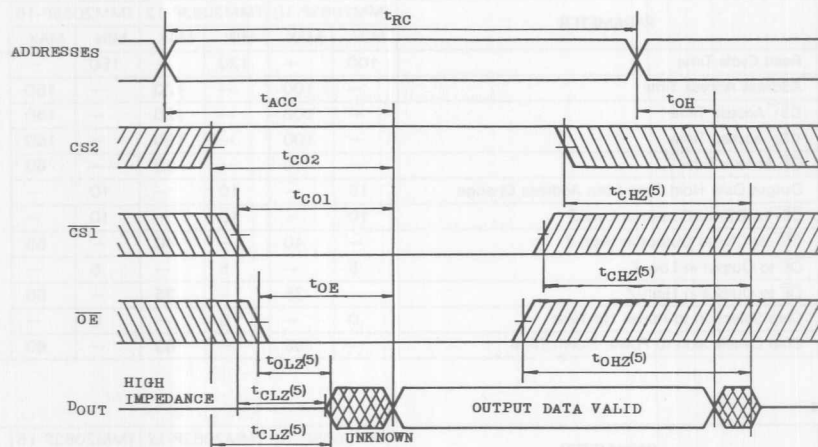
Write Cycle

| SYMBOL | PARAMETER | TMM2063P-10 | | TMM2063P-12 | | TMM2063P-15 | | UNIT |
|------------------|--------------------------------|-------------|------|-------------|------|-------------|------|------|
| | | MIN. | MAX. | MIN. | MAX. | MIN. | MAX. | |
| t _{WC} | Write Cycle Time | 100 | — | 120 | — | 150 | — | ns |
| t _{CW} | Chip Selection to End of Write | 80 | — | 100 | — | 120 | — | |
| t _{AS} | Address Set Up Time | 10 | — | 10 | — | 10 | — | |
| t _{WP} | Write Pulse Width | 70 | — | 85 | — | 100 | — | |
| t _{WR} | Write Recovery Time | 0 | — | 0 | — | 0 | — | |
| t _{DS} | Data Set Up Time | 40 | — | 50 | — | 60 | — | |
| t _{DH} | Data Hold Time | 0 | — | 0 | — | 0 | — | |
| t _{WLZ} | WE to Output in Low-Z | 5 | — | 5 | — | 5 | — | |
| t _{WHZ} | WE to Output in High-Z | — | 30 | — | 35 | — | 40 | |

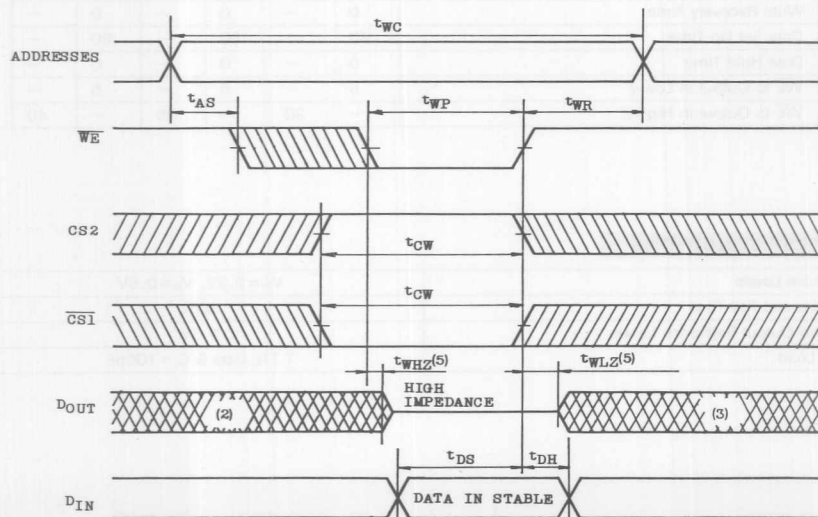
A. C. TEST CONDITIONS

| | |
|-----------------------------------|--|
| Input Pulse Levels | V _{IH} =2.2V, V _{IL} =0.6V |
| Input Rise and Fall Time | 10ns |
| Input and Output Reference Levels | 1.5V |
| Output Load | 1 TTL Gate & C _L =100pF |

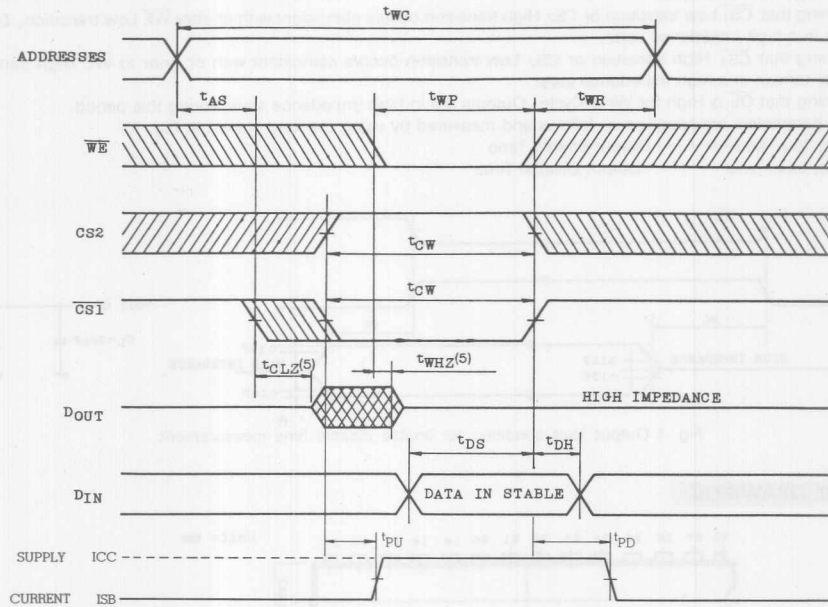
● READ CYCLE (1)



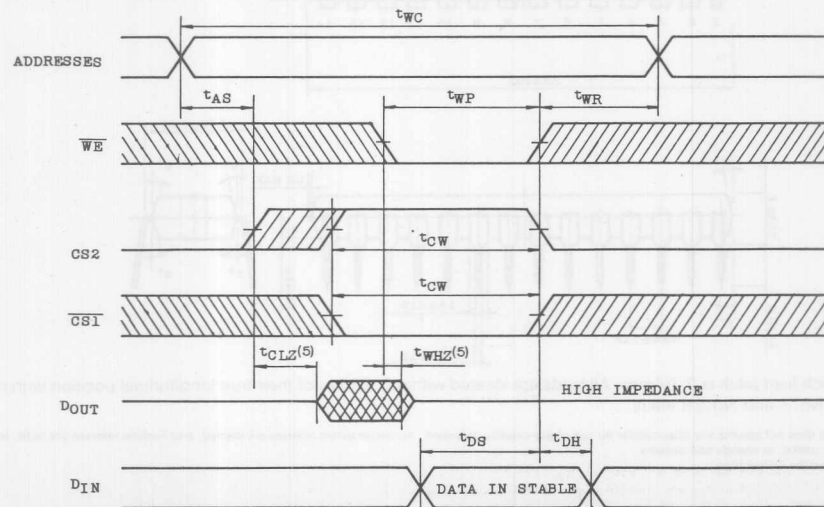
● WRITE CYCLE 1 (4) (\overline{WE} Controlled Write)



● WRITE CYCLE 2 (4) ($\overline{CS1}$ Controlled Write)



● WRITE CYCLE 3 (4) ($\overline{CS2}$ Controlled Write)



TMM2063P-10, TMM2063P-12 TMM2063P-15

Note :

1. \overline{WE} is High for Read Cycle.
2. Assuming that $\overline{CS_1}$ Low transition or $\overline{CS_2}$ High transition occurs coincident with or after \overline{WE} Low transition, Outputs remain in a high impedance state.
3. Assuming that $\overline{CS_1}$ High transition or $\overline{CS_2}$ Low transition occurs coincident with or prior to \overline{WE} High transition, Outputs remain in a high impedance state.
4. Assuming that \overline{OE} is High for Write Cycle, Outputs are in high impedance state during this period.
5. These parameters are specified as follows and measured by using the load shown in Fig. 1 .
(A) tCLZ, tOLZ, tWLZ.....Output Enable Time
(B) tCHZ, tOHZ, tWHZ.....Output Disable Time

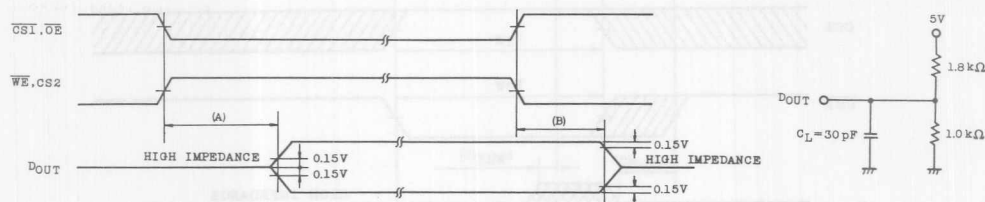
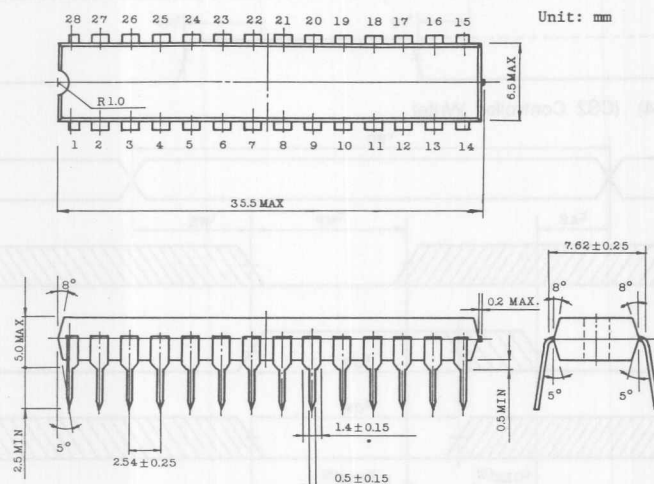


Fig. 1 Output load condition for enable disable time measurement.

OUTLINE DRAWINGS



NOTES : Each lead pitch is 2.54mm. All leads are located within 0.25mm of their true longitudinal position with respect to No. 1 and No. 28 leads.

Note : Toshiba does not assume any responsibility for use of any circuitry described ; no circuit patent licenses are implied, and Toshiba reserves the right, at any time without notice, to change said circuitry.

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TOSHIBA MOS MEMORY PRODUCTS

8,192 WORD \times 8 BIT STATIC RAM
N-CHANNEL SILICON GATE MOS

TMM2064P-10, TMM2064P-12
TMM2064P-15

DESCRIPTION

The TMM2064P is a 65,536 bits high speed and low power static random access memory organized as 8,192 words by 8 bits and operates from a single 5V supply. Toshiba's high performance device technology provides both high speed and low power features with a maximum access time of 100ns/120ns/150ns and maximum operating current of 80mA. When \overline{CS}_1 is a logical high or \overline{CS}_2 is a logical

low, the device is placed in a low power standby mode in which maximum standby current is 10mA. Thus the TMM2064P is most suitable for use in microcomputer peripheral memory where the low power applications are required. The TMM2064P is fabricated with ion implanted N channel silicon gate MOS technology for high performance and high reliability.

FEATURES

- Access Time and Current

| Part Number | Parameter | Access Time (Max.) | Operating Current (Max.) | Standby Current (Max.) |
|-------------|-----------|--------------------|--------------------------|------------------------|
| TMM2064P-10 | | 100ns | 80mA | 10mA |
| TMM2064P-12 | | 120ns | 80mA | 10mA |
| TMM2064P-15 | | 150ns | 80mA | 10mA |

- Single 5V Power Supply
- Fully Static Operation
- Power Down Feature : \overline{CS}_1 , \overline{CS}_2
- Output Buffer Control : \overline{OE}
- Three State Outputs
- All Inputs and Outputs : Directly TTL Compatible
- Inputs Protected : All inputs have protection against static charge.

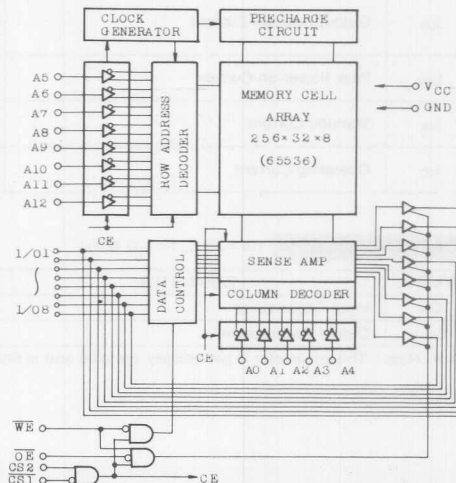
PIN CONNECTION

| | | | |
|------|----|----|-------------------|
| N.C. | 1 | 28 | V_{CC} |
| A12 | 2 | 27 | \overline{WE} |
| A7 | 3 | 26 | \overline{CS}_2 |
| A5 | 4 | 25 | A8 |
| A5 | 5 | 24 | A9 |
| A4 | 6 | 23 | A11 |
| A3 | 7 | 22 | \overline{OE} |
| A2 | 8 | 21 | A10 |
| A1 | 9 | 20 | \overline{CS}_1 |
| A0 | 10 | 19 | I/O8 |
| I/O1 | 11 | 18 | I/O7 |
| I/O2 | 12 | 17 | I/O6 |
| I/O3 | 13 | 16 | I/O5 |
| GND | 14 | 15 | I/O4 |

PIN NAMES

| SYMBOL | NAME |
|---------------------------------------|-----------------------|
| A0~A4 | Column Address Inputs |
| A5~A12 | Row Address Inputs |
| \overline{CS}_1 , \overline{CS}_2 | Chip Select Inputs |
| \overline{WE} | Write Enable Input |
| I/O1~I/O8 | Data Input/Output |
| \overline{OE} | Output Enable Input |
| V_{CC} | Power (5V) |
| GND | Ground |
| N.C. | No Connection |

BLOCK DIAGRAM



TMM2064P-10, TMM2064P-12 TMM2064P-15

MAXIMUM RATINGS

| SYMBOL | ITEM | RATING | UNIT |
|------------------------------------|------------------------------|-----------|--------|
| V _{CC} | Power Supply Voltage | -0.5~7.0 | V |
| V _{IN} , V _{OUT} | Input/Output Voltage | -0.5*~7.0 | V |
| T _{OPR} | Operating Temperature | 0~70 | °C |
| T _{STG} | Storage Temperature | -55~150 | °C |
| T _{SOLDER} | Soldering Temperature · Time | 260 · 10 | °C·sec |
| P _D | Power Dissipation (Ta=70°C) | 1.0 | W |

* -3.0V at Pulse width 50ns

D. C. RECOMMENDED OPERATING CONDITIONS (Ta=0~70°C)

| SYMBOL | PARAMETER | MIN. | TYP. | MAX. | UNIT |
|-----------------|--------------------|--------|------|----------------------|------|
| V _{IH} | Input High Voltage | 2.0 | — | V _{CC} +1.0 | V |
| V _{IL} | Input Low Voltage | -0.5** | — | 0.8 | V |
| V _{CC} | Supply Voltage | 4.5 | 5.0 | 5.5 | V |

** -3.0V at Pulse width 50ns

D. C. CHARACTERISTICS (Ta=0~70°C, V_{CC}=5.0V±10%)

| SYMBOL | PARAMETER | CONDITIONS | MIN. | TYP. | MAX. | UNIT |
|------------------|------------------------|--|------|------|------|------|
| I _{IL} | Input Leakage Current | V _{IN} =0V~5.5V | -10 | — | 10 | μA |
| V _{OH} | Output High Voltage | I _{OUT} =-1.0mA | 2.4 | — | — | V |
| V _{OL} | Output Low Voltage | I _{OUT} =2.1mA | — | — | 0.4 | V |
| I _{LO} | Output Leakage Current | CS ₁ =V _{IH} or CS ₂ =V _{IL} or WE=V _{IL} or OE=V _{IH} , V _{OUT} =0V~5.5V | -10 | — | 10 | μA |
| I _{SBP} | Peak Power-on Current | CS ₁ =V _{CC} , CS ₂ =0V I _{OUT} =0mA | — | — | 20 | mA |
| I _{SB} | Standby Current | CS ₁ =V _{IH} or CS ₂ =V _{IL} , I _{OUT} =0mA | — | — | 10 | mA |
| I _{CC} | Operating Current | CS ₁ =V _{IL} , CS ₂ =V _{IH} , I _{OUT} =0mA | — | — | 80 | mA |

CAPACITANCE *** (Ta=25°C, f=1.0 MHz)

| SYMBOL | PARAMETER | CONDITIONS | MAX. | UNIT |
|------------------|--------------------|---------------------|------|------|
| C _{IN} | Input Capacitance | V _{IN} =0V | 5 | pF |
| C _{OUT} | Output Capacitance | V _{IN} =0V | 10 | pF |

*** Note : This parameter is periodically sampled and is not 100% tested.

TMM2064P-10, TMM2064P-12 TMM2064P-15

A. C. CHARACTERISTICS

(Ta=0~70°C, Vcc=5V±10%)

Read Cycle

| SYMBOL | PARAMETER | TMM2064P-10 | | TMM2064P-12 | | TMM2064P-15 | | UNIT |
|------------------|--|-------------|------|-------------|------|-------------|------|------|
| | | MIN. | MAX. | MIN. | MAX. | MIN. | MAX. | |
| t _{RC} | Read Cycle Time | 100 | — | 120 | — | 150 | — | ns |
| t _{ACC} | Address Access Time | — | 100 | — | 120 | — | 150 | |
| t _{CO1} | CS ₁ Access Time | — | 100 | — | 120 | — | 150 | |
| t _{CO2} | CS ₂ Access Time | — | 100 | — | 120 | — | 150 | |
| t _{OE} | OE Access Time | — | 40 | — | 50 | — | 60 | |
| t _{OH} | Output Data Hold Time from Address Change | 10 | — | 10 | — | 10 | — | |
| t _{CLZ} | CS ₁ or CS ₂ to Output in Low-Z | 10 | — | 10 | — | 10 | — | |
| t _{CHZ} | CS ₁ or CS ₂ to Output in High-Z | — | 40 | — | 40 | — | 55 | |
| t _{OLZ} | OE to Output in Low-Z | 5 | — | 5 | — | 5 | — | |
| t _{OHZ} | OE to Output in High-Z | — | 35 | — | 35 | — | 50 | |
| t _{PU} | Chip Selection to Power Up Time | 0 | — | 0 | — | 0 | — | |
| t _{PD} | Chip Deselection to Power Down Time | — | 50 | — | 60 | — | 60 | |

Write Cycle

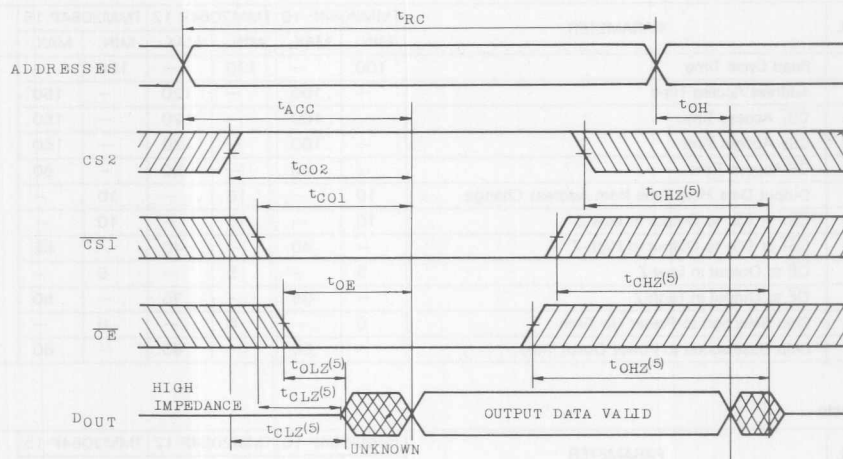
| SYMBOL | PARAMETER | TMM2064P-10 | | TMM2064P-12 | | TMM2064P-15 | | UNIT |
|------------------|--------------------------------|-------------|------|-------------|------|-------------|------|------|
| | | MIN. | MAX. | MIN. | MAX. | MIN. | MAX. | |
| t _{WC} | Write Cycle Time | 100 | — | 120 | — | 150 | — | ns |
| t _{CW} | Chip Selection to End of Write | 80 | — | 100 | — | 120 | — | |
| t _{AS} | Address Set Up Time | 10 | — | 10 | — | 10 | — | |
| t _{WP} | Write Pulse Width | 70 | — | 85 | — | 100 | — | |
| t _{WR} | Write Recovery Time | 0 | — | 0 | — | 0 | — | |
| t _{DS} | Data Set Up Time | 40 | — | 50 | — | 60 | — | |
| t _{DH} | Data Hold Time | 0 | — | 0 | — | 0 | — | |
| t _{WLZ} | WE to Output in Low-Z | 5 | — | 5 | — | 5 | — | |
| t _{WHZ} | WE to Output in High-Z | — | 30 | — | 35 | — | 40 | |

A. C. TEST CONDITIONS

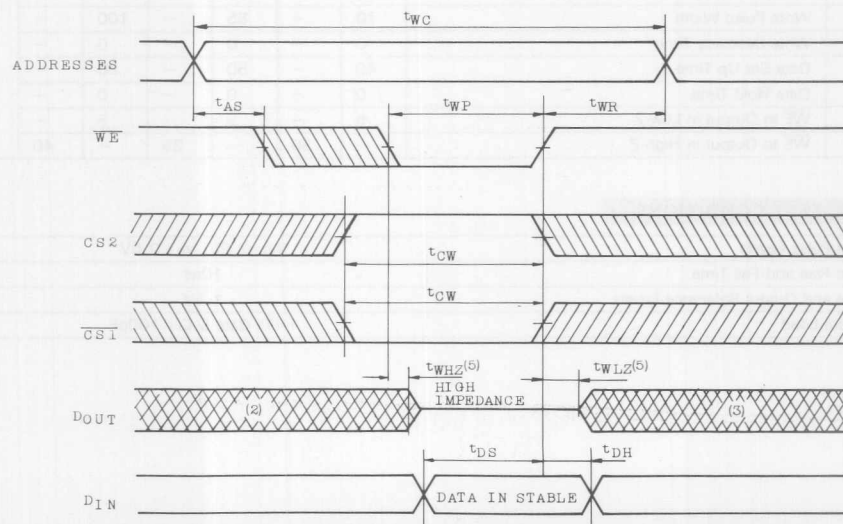
| | |
|-----------------------------------|--|
| Input Pulse Levels | V _{IH} =2.2V, V _{IL} =0.6V |
| Input Rise and Fall Time | 10ns |
| Input and Output Reference Levels | 1.5V |
| Output Load | 1 TTL Gate & C _L =100pF |

TIMING WAVEFORMS

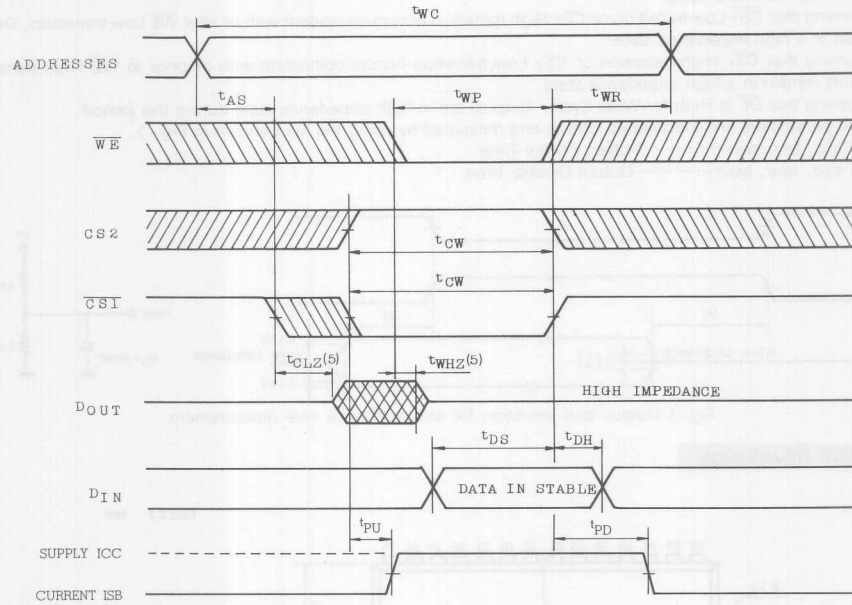
• READ CYCLE (1)



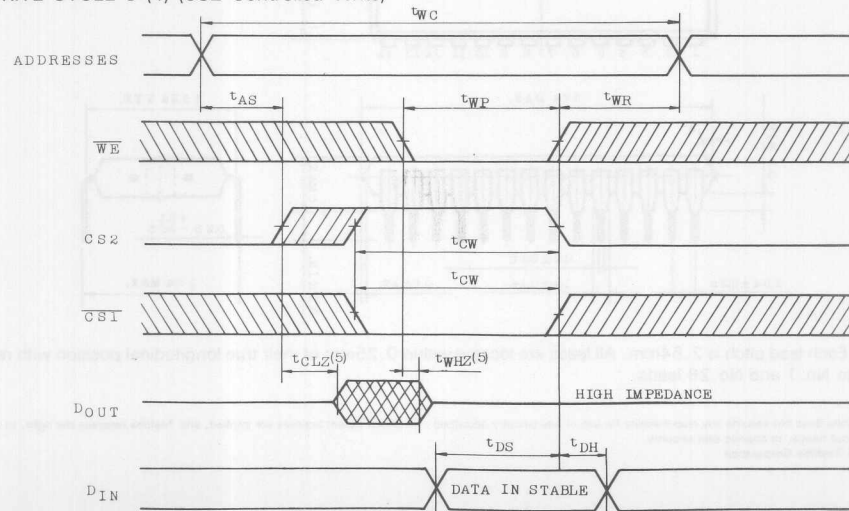
• WRITE CYCLE 1 (4) (\overline{WE} Controlled Write)



● WRITE CYCLE 2 (4) ($\overline{CS1}$ Controlled Write)



● WRITE CYCLE 3 (4) ($\overline{CS2}$ Controlled Write)



TMM2064P-10, TMM2064P-12 TMM2064P-15

Note :

1. \overline{WE} is High for Read Cycle.
2. Assuming that $\overline{CS1}$ Low transition or $\overline{CS2}$ High transition occurs coincident with or after \overline{WE} Low transition, Outputs remain in a high impedance state.
3. Assuming that $\overline{CS1}$ High transition or $\overline{CS2}$ Low transition occurs coincident with or prior to \overline{WE} High transition, Outputs remain in a high impedance state.
4. Assuming that \overline{OE} is High for Write Cycle, Outputs are in high impedance state during this period.
5. These parameters are specified as follows and measured by using the load shown in Fig. 1.
(A) t_{CLZ} , t_{OLZ} , t_{WLZ}Output Enable Time
(B) t_{CHZ} , t_{OHZ} , t_{WHZ}Output Disable Time

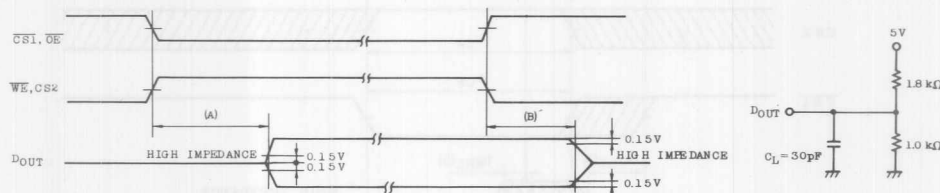
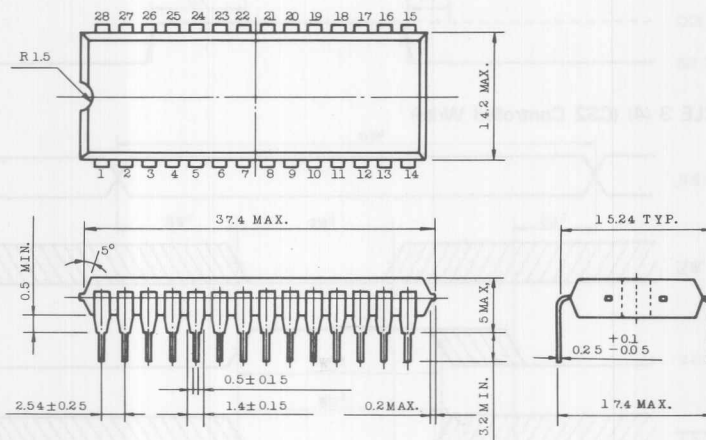


Fig. 1 Output load condition for enable disable time measurement.

OUTLINE DRAWINGS

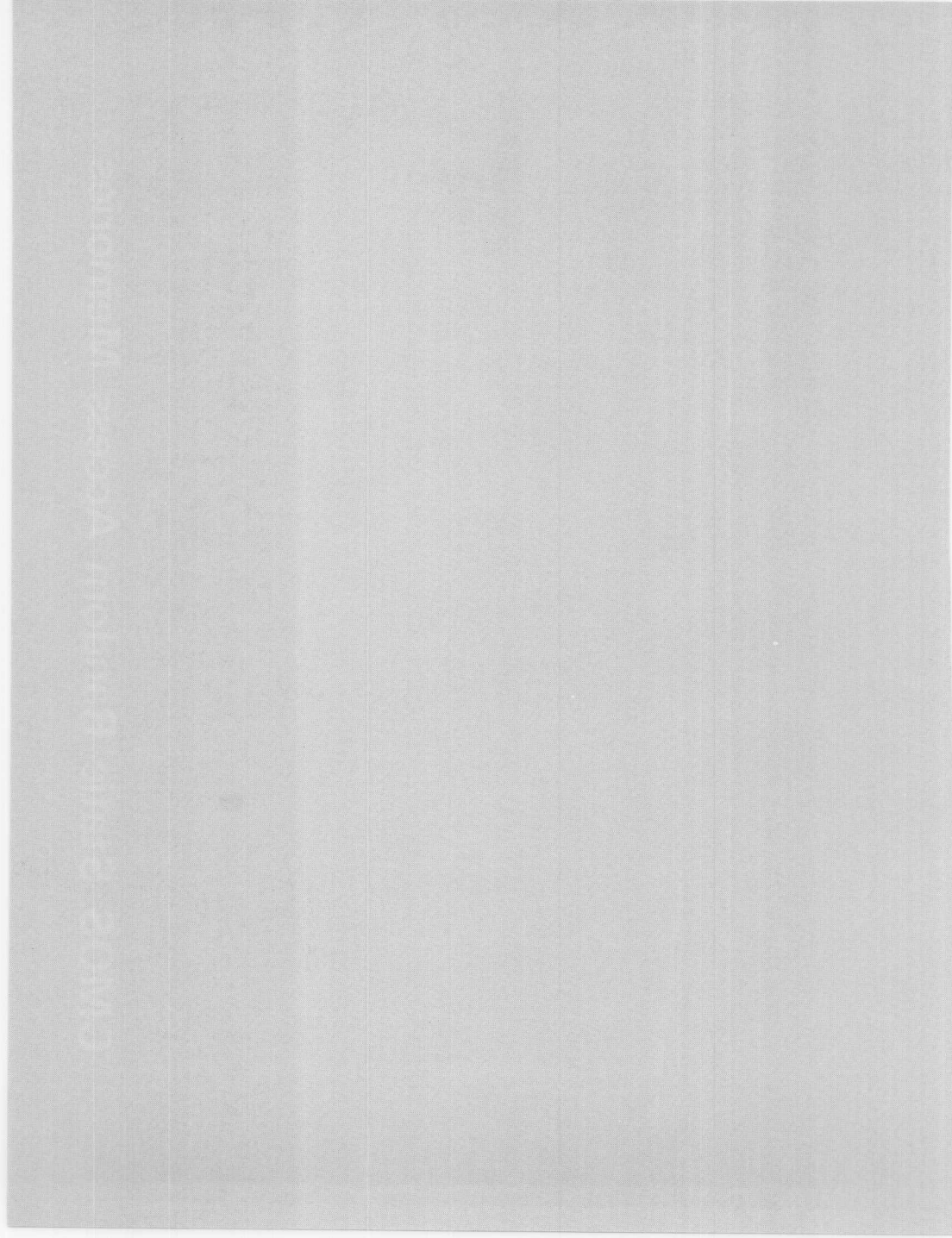
Unit: mm



NOTES : Each lead pitch is 2.54mm. All leads are located within 0.25mm of their true longitudinal position with respect to No.1 and No.28 leads.

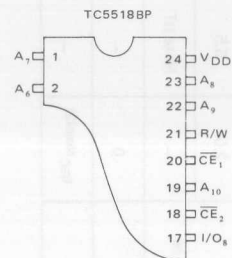
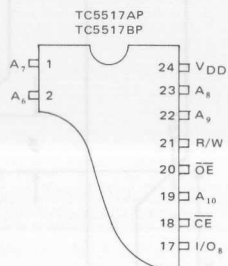
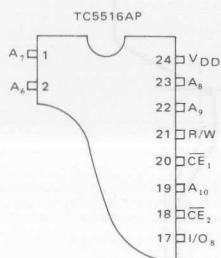
Note : Toshiba does not assume any responsibility for use of any circuitry described : no circuit patent licenses are implied, and Toshiba reserves the right, at any time without notice, to change said circuitry.

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16KBit CMOS STATIC RAM COMPARISON TABLE

PIN CONFIGURATION



OPERATION MODE

| Device Number | TC5516AP | | | | | | TC5517AP TC5517BP | | | | | | TC5518BP | | | | | |
|--------------------|-----------------|-----------------|-----|---------------------------------|---------------------------------|------------------|----------------------|----|-----|---------------------------------|---------------------------------|------------------|-----------------|-----------------|-----|---------------------------------|---------------------------------|------------------|
| Pin No. | 18 | 20 | 21 | 1~8, 22 23, 19 | 9~11 13~17 | Power | 18 | 20 | 21 | 1~8, 22 23, 19 | 9~11 13~17 | Power | 18 | 20 | 21 | 1~8, 22 23, 19 | 9~11 13~17 | Power |
| Mode Name | CE ₂ | CE ₁ | R/W | A ₀ ~A ₁₀ | I/O ₁ ~ ₈ | | CE | OE | R/W | A ₀ ~A ₁₀ | I/O ₁ ~ ₈ | | CE ₂ | CE ₁ | R/W | A ₀ ~A ₁₀ | I/O ₁ ~ ₈ | |
| WRITE | L | L | L | Valid | D _{IN} | I _{DDO} | L | * | L | Valid | D _{IN} | I _{DDO} | L | L | L | Valid | D _{IN} | I _{DDO} |
| READ | L | L | H | Valid | D _{OUT} | I _{DDO} | L | L | H | Valid | D _{OUT} | I _{DDO} | L | L | H | Valid | D _{OUT} | I _{DDO} |
| STANDBY 1 | L | H | * | * | High-Z | I _{DDO} | / | / | / | / | / | / | * | H | * | * | High-Z | I _{DDS} |
| STANDBY 2 | H | * | * | * | High-Z | I _{DDS} | H | * | * | * | High-Z | I _{DDS} | H | * | * | * | High-Z | I _{DDS} |
| OUTPUT DESELECT | / | / | / | / | / | / | L | H | * | * | High-Z | I _{DDO} | / | / | / | / | / | / |

* H or L

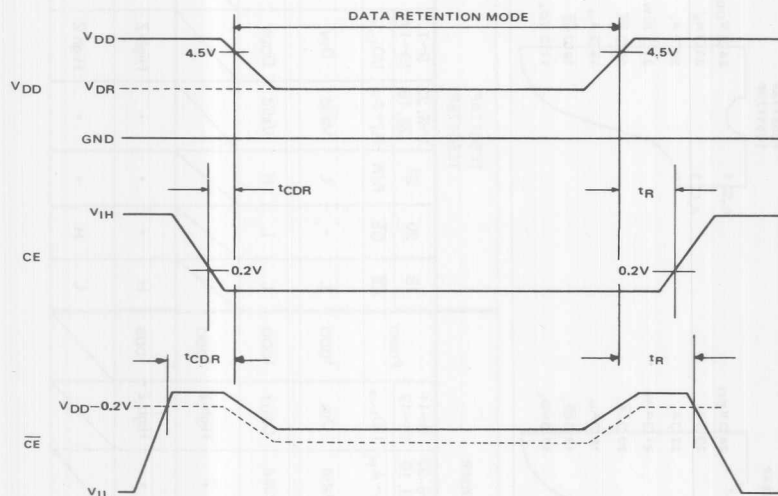
DATA RETENTION CHARACTERISTICS (Ta = -30 ~ 85°)

| SYMBOL | PARAMETER | CONDITIONS | Min. | Max. | UNIT |
|------------------|---|---|-------------------------|----------|------|
| V _{DR} | Data Retention Voltage | $0V \leq CE \leq 0.2V$ or $V_{DD}-0.2V \leq \overline{CE} \leq V_{DD}^{*(3)}$ | 2.0 | 5.5 | V |
| I _{DDS} | Data Retention Current | | — | Note (1) | μA |
| t _{CDR} | Chip Deselection to Data Retention Time | | 0 | — | μS |
| t _R | Recovery Time | | t _{RC} Note(2) | — | μS |

Note (1) : Refer to I_{DDS} specification in individual data sheet.

(2) : Read cycle time.

TIMING CHART



Note (3) : For 16K Bit CMOS RAM, $V_{DD}-0.5V \leq \overline{CE} \leq V_{DD}$
Details are specified in TC5516/17/18 data sheets.

TOSHIBA MOS MEMORY PRODUCTS

1,024 WORD \times 4 BIT CMOS STATIC RAM
SILICON GATE CMOS

TC5513AP-20
TC5513APL-20

DESCRIPTION

The TC5513AP is a 4,096-bit high speed static random access memory organized as 1,024 words by 4 bits and operates from a single 5-volt supply.

The TC5513AP is a fully CMOS RAM and is therefore suited for use in low power applications where battery operation and/or battery back up for

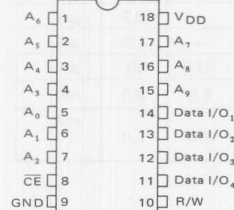
nonvolatility are required. The TC5513AP is guaranteed for data retention at power supply voltages as 2.0 volt. All inputs and outputs are TTL compatible.

The TC5513AP is packed in standard 18 pin dual-in-line plastic 0.3 inch width.

FEATURES

- Low Power Dissipation
27.5m W/MHz (MAX.): Operating
- Standby Current
 $0.2\mu\text{A}$ (MAX.) at $T_a = 25^\circ\text{C}$ } TC5513APL-20
 $1.0\mu\text{A}$ (MAX.) at $T_a = 60^\circ\text{C}$ }
 $20\mu\text{A}$ (MAX.) TC5513AP-20
- Fast Access Time
 $t_{\text{ACC}} : 200\text{ns}$ (MAX.)
- Single 5V Power Supply
- Data Retention Supply Voltage
2V to 5.5V
- Fully Static Operation
- On-chip Address Transition Detector
- Three State Outputs
- Inputs and outputs Directly TTL compatible
- Package
Plastic DIP: TC5513AP-20/APL-20

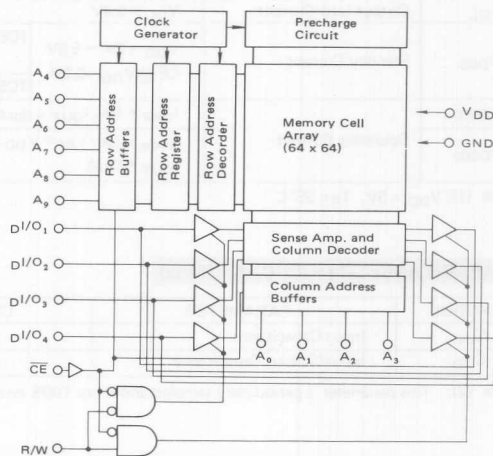
PIN CONNECTION (TOP VIEW)



PIN NAMES

| | |
|----------------------------|------------------------|
| $A_0 \sim A_9$ | Address Inputs |
| R/W | Read Write Input |
| $\overline{\text{CE}}$ | Chip Enable Input |
| Data I/O $_1 \sim 4$ | Data Input/Output |
| V_{DD}/GND | Power Supply Terminals |

BLOCK DIAGRAM



TC5513AP-20

TC5513APL-20

MAXIMUM RATINGS

| SYMBOL | ITEM | RATING | UNIT |
|---------------------|-------------------------------|------------------------------|----------|
| V _{DD} | Power Supply Voltage | -0.3 ~ 7.0 | V |
| V _{IN} | Input Voltage | -0.3 ~ 7.0 | V |
| V _{I/O} | I/O Voltage | -0.3 ~ V _{DD} + 0.5 | V |
| P _D | Power Dissipation (Ta = 85°C) | 550 | mW |
| T _{SOLDER} | Soldering Temperature • Time | 260 • 10 | °C • sec |
| T _{STG} | Storage Temperature | -55 ~ 150 | °C |
| T _{OPR} | Operating Temperature | -30 ~ 85 | °C |

D.C. RECOMMENDED OPERATING CONDITIONS

| SYMBOL | PARAMETER | MIN. | TYP. | MAX. | UNIT |
|-----------------|--------------------------|------|------|-----------------------|------|
| V _{DD} | Power Supply Voltage | 4.5 | 5.0 | 5.5 | V |
| V _{IH} | Input High Level Voltage | 2.2 | — | V _{DD} + 0.3 | V |
| V _{IL} | Input Low Level Voltage | -0.3 | — | 0.8 | V |
| V _{DH} | Data Retention Voltage | 2.0 | — | 5.5 | V |

D.C. CHARACTERISTICS (V_{DD} = 5V ± 10%, Ta = -30 ~ 85°C)

| SYMBOL | PARAMETER | CONDITIONS | | MIN. | TYP. ⁽¹⁾ | MAX. | UNIT | |
|-------------------|------------------------|---|--------------|---------|---------------------|------|------|----|
| I _{IL} | Input Leakage Current | 0V ≤ V _{IN} ≤ V _{DD} | | — | — | ±1.0 | μA | |
| I _{LO} | Output Leakage Current | CE = V _{IH} , 0V ≤ V _{I/O} ≤ V _{DD} | | — | — | ±1.0 | μA | |
| I _{OH} | Output High Current | V _{OH} = 2.4V | | -1.0 | — | — | mA | |
| I _{OL} | Output Low Current | V _{OL} = 0.4V | | 2.0 | — | — | mA | |
| I _{DDS} | Standby Current | V _{DD} = 2V ~ 5.5V CE ≥ V _{DD} - 0.2V | TC5513APL-20 | Ta=25°C | — | — | 0.2 | μA |
| | | | | Ta=60°C | — | — | 1.0 | μA |
| | | | TC5513AP-20 | | — | 0.05 | 20 | μA |
| I _{DD01} | Operating Current | t _{cycle} = 1μs, I _{OUT} = 0mA | | — | 5.0 | 9.0 | mA | |
| I _{DD02} | | t _{cycle} = 1μs, V _{IH} = V _{DD} , V _{IL} = 0V, I _{OUT} = 0mA | | — | 3.0 | 5.0 | mA | |

Note (1): V_{DD} = 5V, Ta = 25°C

CAPACITANCE (Ta = 25°C, f = 1MHz)

| SYMBOL | PARAMETER | CONDITIONS | MIN. | TYP. | MAX. | UNIT |
|------------------|--------------------------|-----------------------|------|------|------|------|
| C _{IN} | Input Capacitance | V _{IN} = 0V | — | 4 | 8 | pF |
| C _{I/O} | Input/Output Capacitance | V _{I/O} = 0V | — | 5 | 10 | pF |

Note (2): This parameter is periodically sampled and is not 100% tested.

A.C. CHARACTERISTICS ($V_{DD} = 5V \pm 10\%$, $T_a = -30 \sim 85^\circ C$)

• READ CYCLE

| SYMBOL | PARAMETER | TC5513AP-20/APL-20 | | UNIT |
|-----------|-----------------------|--------------------|------|------|
| | | MIN. | MAX. | |
| t_{RC} | Read Cycle Time | 200 | — | ns |
| t_{ACC} | Access Time | — | 200 | ns |
| t_{CO} | CE Access Time | — | 200 | ns |
| t_{OH} | Output Data Hold Time | 15 | — | ns |
| t_{DIS} | Output Disable Time | — | 60 | ns |
| t_{COE} | Output Enable Time | 5 | — | ns |

• WRITE CYCLE

| SYMBOL | PARAMETER | TC5513AP-20/APL-20 | | UNIT |
|----------|---------------------|--------------------|------|------|
| | | MIN. | MAX. | |
| t_{WC} | Write Cycle Time | 200 | — | ns |
| t_{AW} | Address Setup Time | 0 | — | ns |
| t_{WP} | Write Pulse Width | 120 | — | ns |
| t_{DS} | Data Setup Time | 120 | — | ns |
| t_{DH} | Data Hold Time | 0 | — | ns |
| t_{WR} | Write Recovery Time | 0 | — | ns |

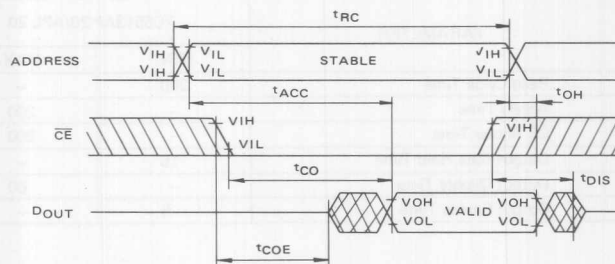
A.C. TEST CONDITIONS

- Output Load : 100pF + 1 TTL Gate
- Input Pulse Levels : 0.6V, 2.4V
- Timing Measurement Reference Levels
 - Input : 0.8V, 2.2V
 - Output : 0.8V, 2.2V
- Input Pulse Rise and Fall Times : 10ns

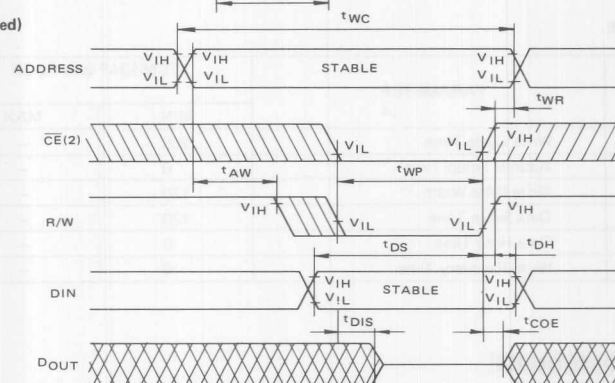
TC5513AP-20 TC5513APL-20

TIMING WAVEFORMS

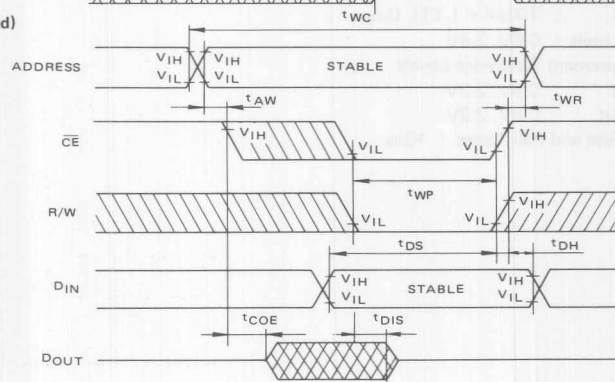
• Read Cycle (1)



• Write Cycle 1 (R/W Controlled)



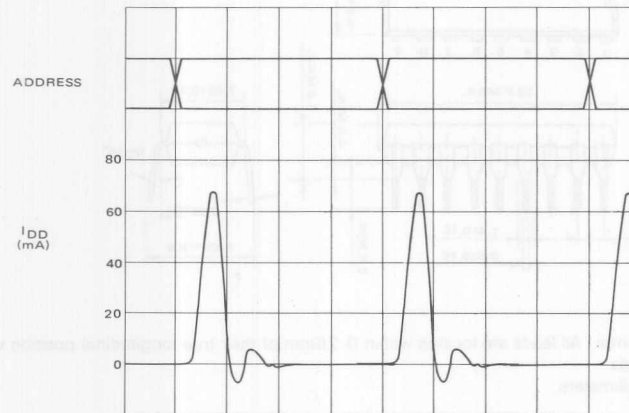
• Write Cycle 2 (CE Controlled)



Notes: (1) R/W is high for a Read Cycle.

(2) If the CE low transition occurs simultaneously with the R/W low transition, the output buffers remain in high impedance state.

TYPICAL CURRENT WAVEFORM

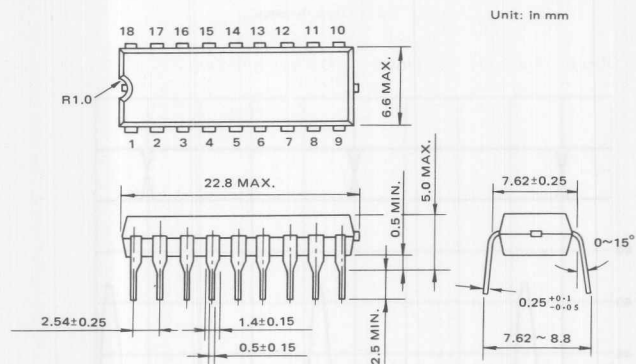


50ns/DIVISION
 $V_{DD} = 5.5V$

TC5513AP-20 TC5513APL-20

OUTLINE DRAWINGS

● PLASTIC PACKAGE



Note : Each lead pitch is 2.54mm. All leads are located within 0.25mm of their true longitudinal position with respect to No. 1 and No. 18 leads.
 All dimensions are in millimeters.

Note: Toshiba does not assume any responsibility for use of any circuitry described; no circuit patent licenses are implied, and Toshiba reserves the right, at any time without notice, to change said circuitry.

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1,024 WORD × 4 BIT CMOS STATIC RAM
SILICON GATE CMOS

TC5514AP-2/-3

TC5514APL-2/-3

DESCRIPTION

The TC5514AP is a 4,096 bit high speed and low power random access memory organized as 1,024 words by 4 bits using CMOS technology, and operates from a single 5-volt supply.

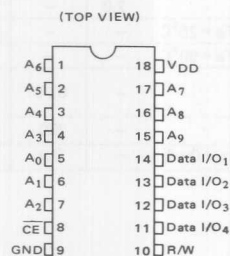
The 5514AP is compatible with the industry produced NMOS 2114 type 4KRAM, yet offers a more than 90% reduction in power of their NMOS equivalents.

The TC5514AP is a fully CMOS RAM, therefore it is suited for use in low power applications where

FEATURES

- Standby Current
0.2μA (Max.) at Ta=25°C
1.0μA (Max.) at Ta=60°C } : TC5514APL
20μA (Max.) : TC5514AP
- Low Power Dissipation : 15mW (Typ.) operating
- Single 5-volt Supply : 5V ± 10%
- Data Retention Supply Voltage : 2 ~ 5.5V
- Three State Outputs
- All Inputs and Outputs : Directly TTL Compatible

PIN CONNECTION



PIN NAMES

| | |
|---------------------------------|--------------------------|
| A ₀ ~ A ₉ | Address Inputs |
| R/W | Read Write Control Input |
| CE | Chip Enable Input |
| Data I/O ₁ ~ 4 | Data Input/Output |
| V _{DD} /GND | Power Supply Terminals |

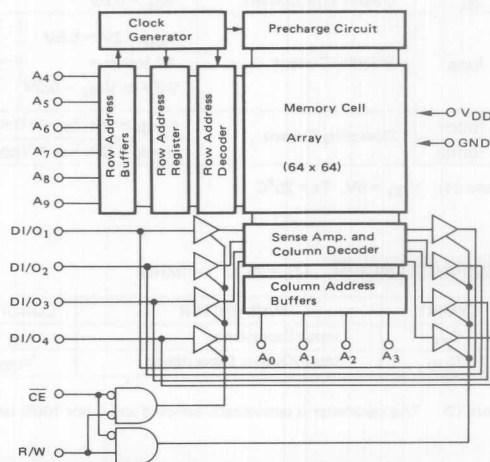
battery operation and battery back up for nonvolatility are required. Furthermore the TC5514APL guaranteed a standby current equal to or less than 1μA at 60°C ambient temperature is available.

The TC5514AP is guaranteed for data retention at a power supply as low as 2 volts. The TC5514AP is directly TTL compatible in all inputs and outputs.

The TC5514AP is offered in standard 18 pin plastic, 0.3inch in width.

- Access Time
200ns (Max.) : TC5514 AP/APL-2
300ns (Max.) : TC5514 AP/APL-3
- Fully Static Operation
- On-chip Address Transition Detector
- Fully Compatible with TMM2114AP Family (Nch 2114 type 4KRAM)
- Package
Plastic DIP : TC5514AP/APL

BLOCK DIAGRAM



TC5514AP-2/-3

TC5514APL-2/-3

MAXIMUM RATINGS

| SYMBOL | ITEM | RATING | UNIT |
|--------------|--|--------------|-----------------------------------|
| V_{DD} | Power Supply Voltage | -0.3 ~ 7.0 | V |
| V_{IN} | Input Voltage | -0.3 ~ 7.0 | V |
| $V_{I/O}$ | I/O Voltage | 0 ~ V_{DD} | V |
| P_D | Power Dissipation ($T_a = 85^\circ\text{C}$) | 550 | mW |
| T_{SOLDER} | Soldering Temperature - Time | 260 · 10 | $^\circ\text{C} \cdot \text{sec}$ |
| T_{STG} | Storage Temperature | -55 ~ 150 | $^\circ\text{C}$ |
| T_{OPR} | Operating Temperature | -30 ~ 85 | $^\circ\text{C}$ |

D.C. RECOMMENDED OPERATING CONDITIONS

| SYMBOL | PARAMETER | MIN. | TYP. | MAX. | UNIT |
|----------|--------------------------|------|------|----------------|------|
| V_{DD} | Power Supply Voltage | 4.5 | 5.0 | 5.5 | V |
| V_{IH} | Input High Level Voltage | 2.2 | — | $V_{DD} + 0.3$ | V |
| V_{IL} | Input Low Level Voltage | -0.3 | — | 0.8 | V |
| V_{DH} | Data Retention Voltage | 2.0 | — | 5.5 | V |

D.C. CHARACTERISTICS ($V_{DD} = 5V \pm 10\%$, $T_a = -30 \sim 85^\circ\text{C}$ unless otherwise noted.)

| SYMBOL | PARAMETER | CONDITIONS | | | MIN. | TYP. (1) | MAX. | UNIT |
|-------------------|------------------------|--|-----------|-----------------------|------|----------|-------|------|
| I _{IL} | Input Leakage Current | 0V ≤ V _{IN} ≤ V _{DD} | | | — | — | ± 1.0 | μA |
| I _{LO} | Output Leakage Current | CE = V _{IH} , 0V ≤ V _{I/O} ≤ V _{DD} | | | — | — | ± 1.0 | μA |
| I _{OH} | Output High Current | V _{OH} = 2.4V | | | −1.0 | — | — | mA |
| I _{OL} | Output Low Current | V _{OL} = 0.4V | | | 2.0 | — | — | mA |
| I _{DDS} | Standby Current | V _{DD} = 2V ~ 5.5V All Inputs = 0.2V or V _{DD} − 0.2V | TC5514APL | T _a = 25°C | — | — | 0.2 | μA |
| | | | | T _a = 60°C | — | — | 1.0 | μA |
| | | TC5514AP | — | 0.05 | 20 | μA | | |
| | | | — | — | — | — | — | |
| I _{DDO1} | Operating Current | t _{cycle} = 1μs, I _{OUT} = 0mA | | | — | 5.0 | 9.0 | mA |
| I _{DDO2} | | t _{cycle} = 1μs, V _{IH} = V _{DD} , V _{IL} = 0V, I _{OUT} = 0mA | | | — | 3.0 | 5.0 | |

Note (1): $V_{DD} = 5V$, $T_a = 25^\circ\text{C}$

CAPACITANCE(2) ($T_a = 25^\circ\text{C}$, $f = 1\text{MHz}$)

| SYMBOL | PARAMETER | CONDITIONS | MIN. | TYP. | MAX. | UNIT |
|-----------|--------------------------|----------------|------|------|------|------|
| C_{IN} | Input Capacitance | $V_{IN} = 0V$ | — | 4 | 8 | pF |
| $C_{I/O}$ | Input/Output Capacitance | $V_{I/O} = 0V$ | — | 5 | 10 | pF |

Note (2): This parameter is periodically sampled and is not 100% tested.

TC5514AP-2/-3

TC5514APL-2/-3

A.C. CHARACTERISTICS (V_{DD} = 5V ± 10%, T_a = -30 ~ 85°C)

• READ CYCLE

| SYMBOL | PARAMETER | TC5514AP-2/APL-2 | | TC5514AP-3/APL-3 | | UNIT |
|------------------|-----------------------|------------------|------|------------------|------|------|
| | | MIN. | MAX. | MIN. | MAX. | |
| t _{RC} | Read Cycle Time | 200 | — | 300 | — | ns |
| t _{ACC} | Access Time | — | 200 | — | 300 | ns |
| t _{CO} | CE Access Time | — | 70 | — | 100 | ns |
| t _{OH} | Output Data Hold Time | 15 | — | 20 | — | ns |
| t _{DIS} | Output Disable Time | — | 60 | — | 80 | ns |
| t _{COE} | Output Enable Time | 5 | — | 5 | — | ns |

• WRITE CYCLE

| SYMBOL | PARAMETER | TC5514AP-2/APL-2 | | TC5514AP-3/APL-3 | | UNIT |
|-----------------|---------------------|------------------|------|------------------|------|------|
| | | MIN. | MAX. | MIN. | MAX. | |
| t _{WC} | Write Cycle Time | 200 | — | 300 | — | ns |
| t _{AW} | Address Setup Time | 0 | — | 0 | — | ns |
| t _{WP} | Write Pulse Width | 120 | — | 150 | — | ns |
| t _{DS} | Data Setup Time | 120 | — | 150 | — | ns |
| t _{DH} | Data Hold Time | 0 | — | 0 | — | ns |
| t _{WR} | Write Recovery Time | 0 | — | 0 | — | ns |

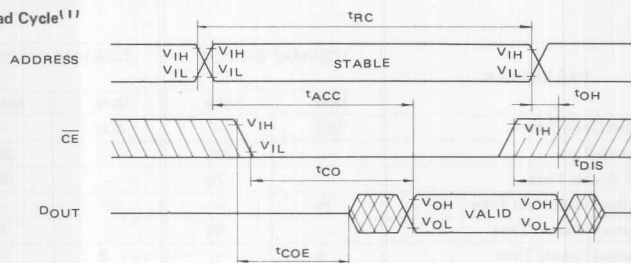
A.C. TEST CONDITIONS

- Output Load : 100 pF + 1 TTL Gate
- Input Pulse Levels : 0.6V, 2.4V
- Timing Measurement Reference Levels
 - Input : 0.8V, 2.2V
 - Output : 0.8V, 2.2V
- Input Pulse Rise and Fall Times : 10 ns

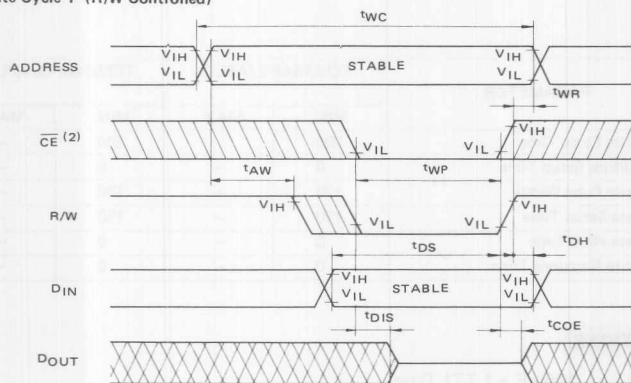
TC5514AP-2/-3 TC5514APL-2/-3

TIMING WAVEFORMS

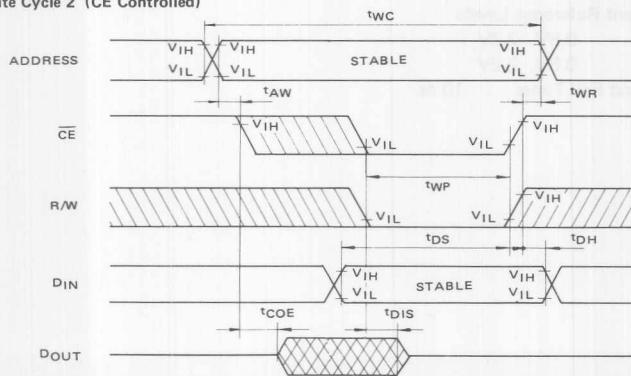
• Read Cycle⁽¹⁾



• Write Cycle 1 (R/W Controlled)



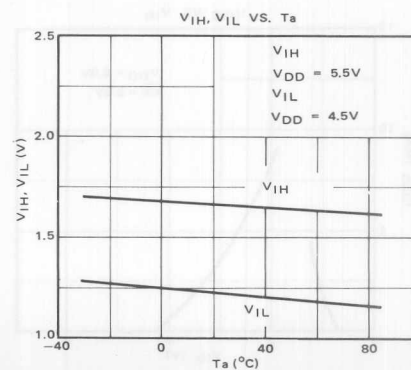
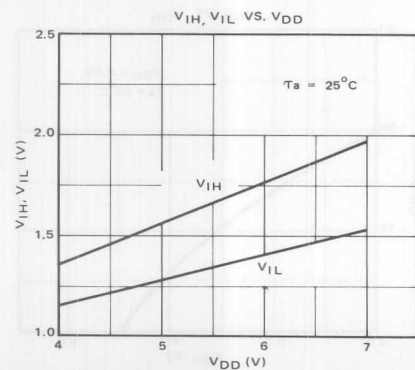
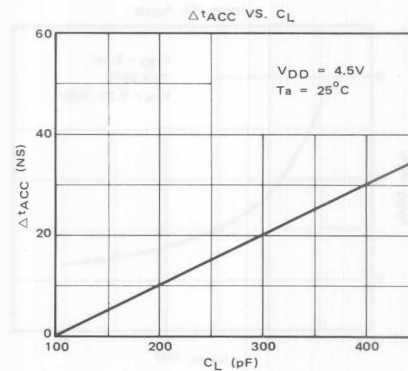
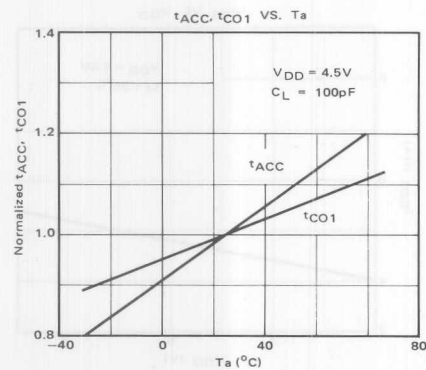
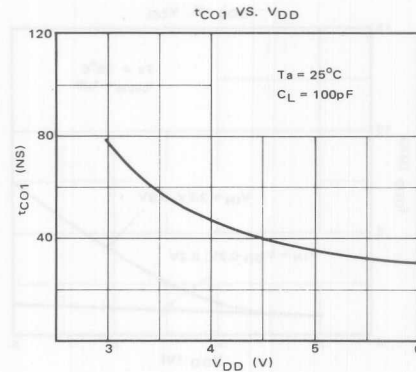
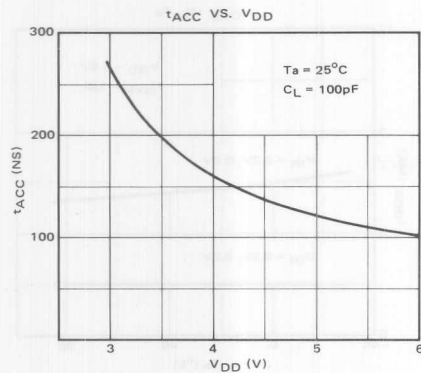
• Write Cycle 2 (CE Controlled)



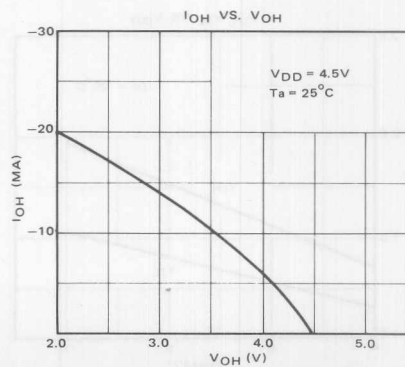
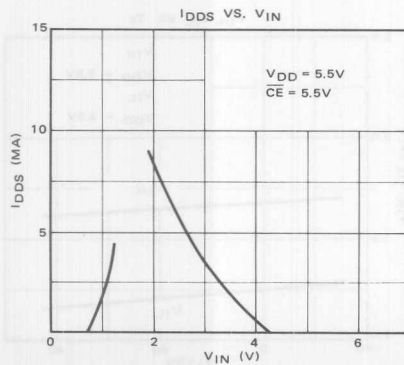
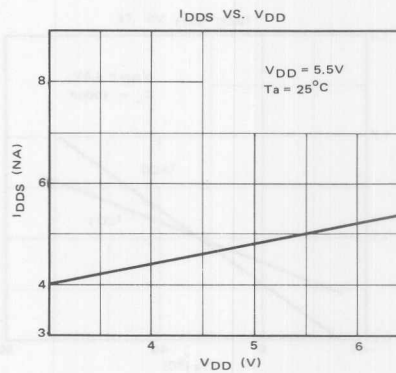
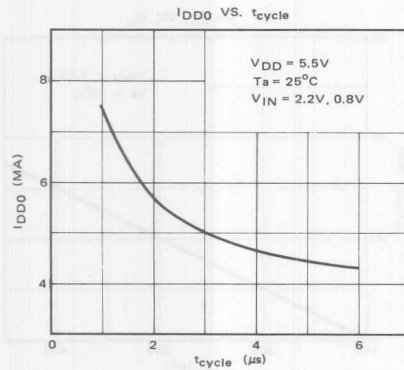
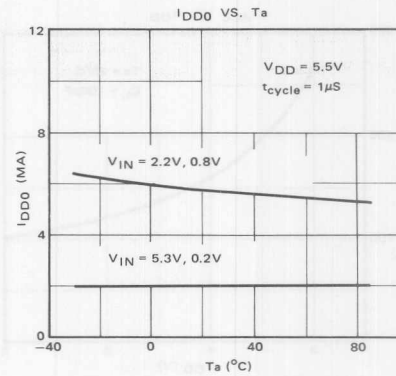
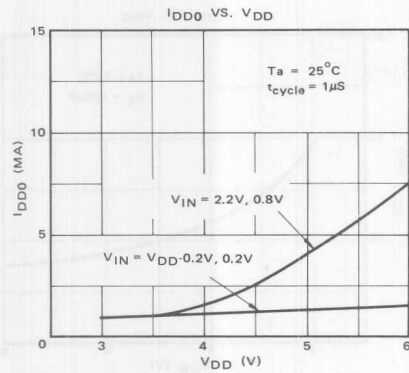
- Notes: (1) R/W is high for a Read Cycle.
(2) If the CE low transition occurs simultaneously with the R/W low transition, the output buffers remain in a high impedance state.

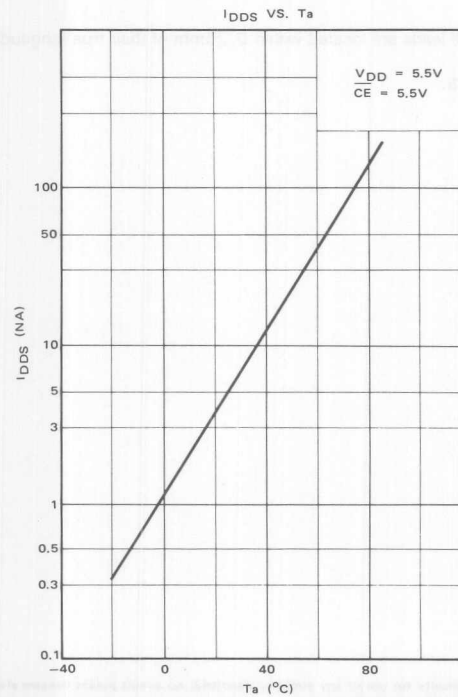
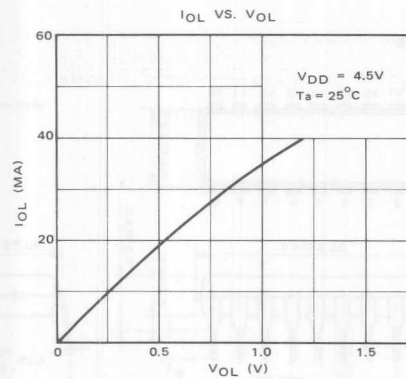
TC5514AP-2/-3

TC5514APL-2/-3



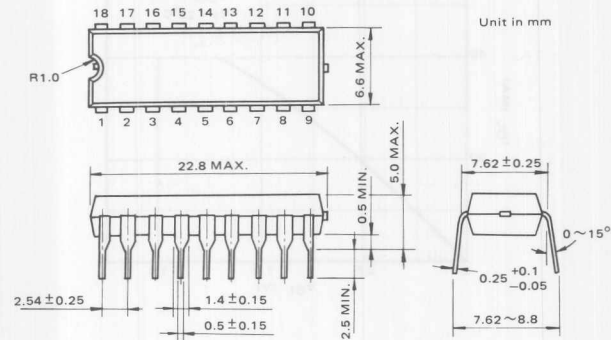
TC5514AP-2/-3 TC5514APL-2/-3





TC5514AP-2/-3 TC5514APL-2/-3

● PLASTIC PACKAGE



Note : Each lead pitch is 2.54mm. All leads are located within 0.25mm of their true longitudinal position with respect to No. 1 and No. 18 leads.
All dimensions are in millimeters.

Notes: Toshiba does not assume any responsibility for use of any circuitry described; no circuit patent licenses are implied, and Toshiba reserves the right, at any time without notice, to change said circuitry.
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TOSHIBA MOS MEMORY PRODUCTS

2,048 WORD \times 8 BIT CMOS STATIC RAM
SILICON GATE CMOS

TC5516AP/-2, TC5516APL/-2
TC5516AF/-2, TC5516AFL/-2

DESCRIPTION

The TC5516AP/AF is a 16384-bit static random access memory organized as 2048 words by 8 bit using CMOS technology, and operates from a single 5 volt supply.

The TC5516AP/AF is featured by two chip enable inputs, that is, \overline{CE}_1 for fast memory access and \overline{CE}_2 for a minimum standby current mode, and is suited for low power application where battery operation or battery back up for nonvolatility are required. Furthermore the TC5516APL/AFL guaranteed a

standby current equal to or less than $1\mu A$ at $60^\circ C$ ambient temperature is available.

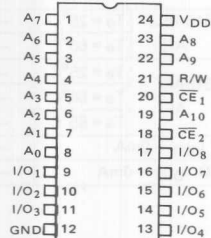
The TC5516AP is also featured by pin compatibility with 2716 type EPROM. This means that the TC5516AP and EPROM can be interchanged in the same socket, and the flexibility in the definition of the quantity of RAM versus EPROM obtained as a result allows the wide application in microcomputer system.

FEATURES

- Standby Current
 - $0.2\mu A$ (Max.) at $T_a = 25^\circ C$
 - $1.0\mu A$ (Max.) at $T_a = 60^\circ C$
 - $1.0\mu A$ (Max.) at $T_a = 25^\circ C$
 - $5.0\mu A$ (Max.) at $T_a = 60^\circ C$
- Low Power Dissipation : 200mW (Typ.)
- Single 5V Power Supply : $5V \pm 10\%$
- Data Retention Supply Voltage: 2.0 ~ 5.5V
- Fully Static Operation

- Access Time
 - 250ns (Max.): TC5516AP/APL/AF/AFL
 - 200ns (Max.): TC5516AP-2/APL-2/AF-2/AFL-2
- Two Chip Enable (\overline{CE}_1 , \overline{CE}_2) for Simple Memory Expansion and Battery Back Up.
- All Inputs and Outputs Directly TTL Compatible
- Three State Outputs
- Package
 - Plastic DIP : TC5516AP/APL
 - Plastic FP : TC5516AF/AFL

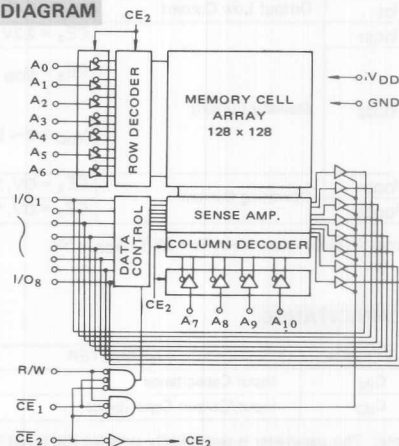
PIN CONNECTION (TOP VIEW)



PIN NAMES

| | |
|------------------------------------|--------------------------|
| $A_0 \sim A_{10}$ | Address Inputs |
| R/W | Read/Write Control Input |
| $\overline{CE}_1, \overline{CE}_2$ | Chip Enable Inputs |
| $I/O_1 \sim I/O_8$ | Data Input/Output |
| V_{DD} | Power (+5V) |
| GND | Ground |

BLOCK DIAGRAM



TC5516AP/-2, TC5516APL/-2 TC5516AF/-2, TC5516AFL/-2

ABSOLUTE MAXIMUM RATINGS

| SYMBOL | ITEM | RATING |
|--------------|--|------------------------------------|
| V_{DD} | Power Supply Voltage | $-0.3V \sim 7.0V$ |
| V_{IN} | Input Voltage | $-0.3V \sim V_{DD} + 0.3$ |
| $V_{I/O}$ | Input/Output Voltage | $-0.3V \sim V_{DD} + 0.3$ |
| P_D | Power Dissipation ($T_a = 85^\circ C$) | 0.8W (0.45W)* |
| T_{STG} | Storage Temperature | $-55^\circ C \sim 150^\circ C$ |
| T_{OPR} | Operating Temperature | $-30^\circ C \sim 85^\circ C$ |
| T_{SOLDER} | Soldering Temperature · Time | $260^\circ C \cdot 10 \text{ sec}$ |

*Plastic FP

RECOMMENDED D.C. OPERATING CONDITIONS ($T_a = -30 \sim 85^\circ C$)

| SYMBOL | PARAMETER | MIN. | TYP. | MAX. | UNIT |
|----------|------------------------|------|------|----------------|------|
| V_{DD} | Power Supply Voltage | 4.5 | 5.0 | 5.5 | V |
| V_{IH} | Input High Voltage | 2.2 | — | $V_{DD} + 0.3$ | V |
| V_{IL} | Input Low Voltage | -0.3 | — | 0.8 | V |
| V_{DH} | Data Retention Voltage | 2.0 | — | 5.5 | V |

D.C. CHARACTERISTICS ($T_a = -30 \sim 85^\circ C$, $V_{DD} = 5V \pm 10\%$)

| SYMBOL | PARAMETER | CONDITIONS | | | | MIN. | TYP. | MAX. | UNIT |
|-------------------|-----------------------|---|------------------|-----------|---|-------|------|------|------|
| I _{IL} | Input Leakage Current | 0 ≤ V _{IN} ≤ V _{DD} | | | | — | — | ±1.0 | μA |
| I _{LO} | I/O Leakage Current | CE ₂ = V _{IH} , 0V ≤ V _{I/O} ≤ V _{DD} | | | | — | — | ±5.0 | μA |
| I _{OH} | Output High Current | V _{OH} = 2.4V | | | | −1.0 | −2.0 | — | mA |
| I _{OL} | Output Low Current | V _{OL} = 0.4V | | | | 2.0 | 3.0 | — | mA |
| I _{DDS1} | Standby Current | CE ₂ = 2.2V | | | | — | 1.0 | 3.0 | mA |
| I _{DDS2} | | CE ₂ = V _{DD} − 0.5V | TC5516AP/ AFL | Ta = 25°C | — | 0.005 | 0.2 | μA | |
| | | | | Ta = 60°C | — | — | 1.0 | | |
| | | V _{DD} = 2 ~ 5.5V | TC5516AP/ AF | Ta = 25°C | — | 0.05 | 1.0 | | |
| | | | | Ta = 60°C | — | — | 5.0 | | |
| I _{DDO1} | Operating Current | | | | | — | — | 30 | |
| I _{DDO2} | | CE ₂ = 0V, V _{IN} = V _{IH} /V _{IL} , I _{OUT} = 0mA | | | | — | 40 | 70 | mA |
| | | CE ₂ = 0V, V _{IN} = V _{DD} /GND, I _{OUT} = 0mA | | | | — | 30 | 55 | |

Note: Typical values are at $T_a = 25^\circ C$, $V_{DD} = 5V$.

CAPACITANCE

| SYMBOL | PARAMETER | MIN. | TYP. | MAX. | UNIT |
|-----------|--------------------------|------|------|------|------|
| C_{IN} | Input Capacitance | — | 5 | 10 | pF |
| $C_{I/O}$ | Input/Output Capacitance | — | 5 | 10 | pF |

Note: This parameter is periodically sampled and is not 100% tested.

TC5516AP/-2, TC5516APL/-2 TC5516AF/-2, TC5516AFL/-2

A.C. CHARACTERISTICS ($T_a = -30 \sim 85^\circ\text{C}$, $V_{DD} = 5V \pm 10\%$)

• Read Cycle

| SYMBOL | PARAMETER | TC5516AP-2/APL-2 TC5516AF-2/AFL-2 | | TC5516AP/APL TC5516AF/AFL | | UNIT |
|-----------|---|--------------------------------------|------|------------------------------|------|------|
| | | MIN. | MAX. | MIN. | MAX. | |
| t_{RC} | Read Cycle Time | 200 | — | 250 | — | ns |
| t_{ACC} | Access Time | — | 200 | — | 250 | ns |
| t_{CO1} | \overline{CE}_1 to Output Valid | — | 100 | — | 100 | ns |
| t_{CO2} | \overline{CE}_2 to Output Valid | — | 200 | — | 250 | ns |
| t_{COE} | \overline{CE}_1 or \overline{CE}_2 to Output Active | 10 | — | 10 | — | ns |
| t_{OD} | Output High-Z from Deselection | — | 80 | — | 80 | ns |
| t_{OH} | Output Hold from Address Change | 10 | — | 10 | — | ns |

• Write Cycle

| SYMBOL | PARAMETER | TC5516AP-2/APL-2 TC5516AF-2/AFL-2 | | TC5516AP/APL TC5516AF/AFL | | UNIT |
|-----------|------------------------|--------------------------------------|------|------------------------------|------|------|
| | | MIN. | MAX. | MIN. | MAX. | |
| t_{WC} | Write Cycle Time | 200 | — | 250 | — | ns |
| t_{WP} | Write Pulse Width | 160 | — | 200 | — | ns |
| t_{AW} | Address Setup Time | 0 | — | 0 | — | ns |
| t_{WR} | Write Recovery Time | 10 | — | 10 | — | ns |
| t_{ODW} | Output High-Z from R/W | — | 80 | — | 80 | ns |
| t_{OEW} | Output Active from R/W | 10 | — | 10 | — | ns |
| t_{DS} | Data Set Up Time | 80 | — | 120 | — | ns |
| t_{DH} | Data Hold Time | 0 | — | 0 | — | ns |

A.C. TEST CONDITIONS

Output Load : 100 pF + ITTL Gate

Input Pulse Levels : 0.6V, 2.4V

Timing Measurement Reference Levels

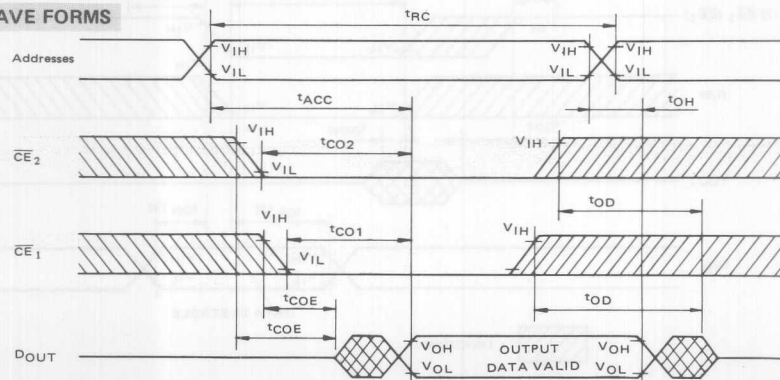
Input : 0.8V and 2.2V

Output : 0.8V and 2.2V

Input Pulse Rise and Fall Times : 10ns

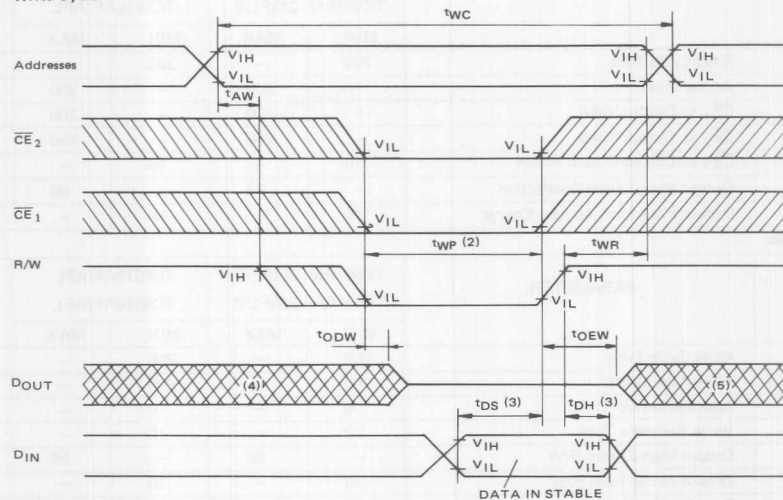
TIMING WAVE FORMS

• Read Cycle

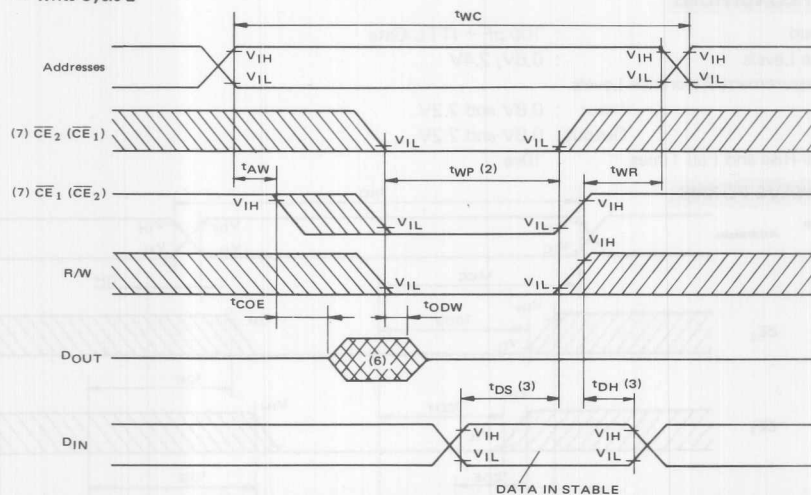



TC5516AP/-2, TC5516APL/-2 TC5516AF/-2, TC5516AFL/-2

• Write Cycle 1



• Write Cycle 2



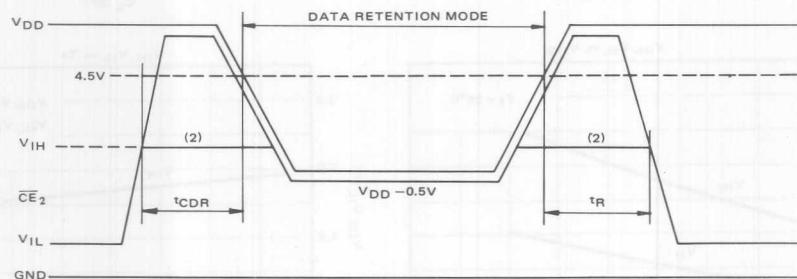
 : UNKNOWN

- NOTE: (1) R/W is high for a Read Cycle.
- (2) t_{WP} is specified as the logical "AND" of \overline{CE}_1 , \overline{CE}_2 and R/W.
 t_{WP} is measured from the latter of \overline{CE}_1 , \overline{CE}_2 or R/W going low to the earlier of \overline{CE}_1 , \overline{CE}_2 or R/W going high.
- (3) t_{DH} , t_{DS} are measured from the earlier of \overline{CE}_1 , \overline{CE}_2 or R/W going high.
- (4) If the \overline{CE}_1 , or \overline{CE}_2 low transition occurs simultaneously with or latter from the R/W low transition in a Write Cycle 1, the output buffers remain in a high impedance state in this period.
- (5) If the \overline{CE}_1 or \overline{CE}_2 high transition occurs prior to or simultaneously with the R/W high transition in a Write Cycle 1, the output buffers remain in a high impedance state in this period.
- (6) If the R/W is low or the R/W low transition occurs prior to or simultaneously with the \overline{CE}_1 or \overline{CE}_2 low transition, the output buffers remain in a high impedance state in this period.
- (7) A write occurs during the overlap of a low \overline{CE}_1 , low \overline{CE}_2 and low R/W. In write cycle 2, write is controlled by either \overline{CE}_1 or \overline{CE}_2 .

DATA RETENTION CHARACTERISTICS ($T_a = -30 \sim 85^\circ\text{C}$)

| SYMBOL | PARAMETER | | | | MIN. | TYP. | MAX. | UNIT |
|-------------------|--|-------------------|-----------------------|---|---------------------|------|------|------|
| V _{DH} | Data Retention Power Supply Voltage | | | | 2.0 | — | 5.5 | V |
| I _{DSS2} | Standby Current | TC5516APL/ AFL | T _a = 25°C | — | 0.005 | 0.2 | μA | |
| | | | T _a = 60°C | — | — | 1.0 | | |
| | | TC5516AP/ AF | T _a = 25°C | — | 0.05 | 1.0 | | |
| | | | T _a = 60°C | — | — | 5.0 | | |
| | | | T _a = 85°C | — | — | 30 | | |
| t _{CDR} | From Chip Deselection to Data Retention Mode | | | | 0 | — | — | μs |
| t _R | Recover Time | | | | t _{RC} (1) | — | — | μs |

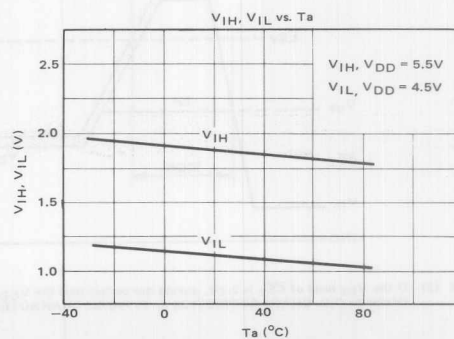
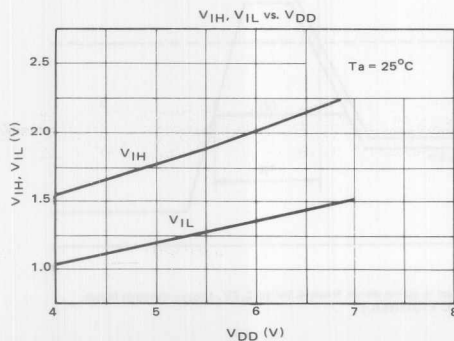
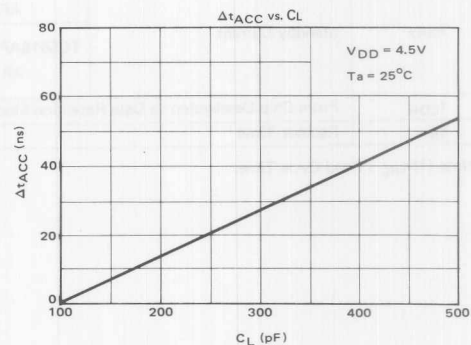
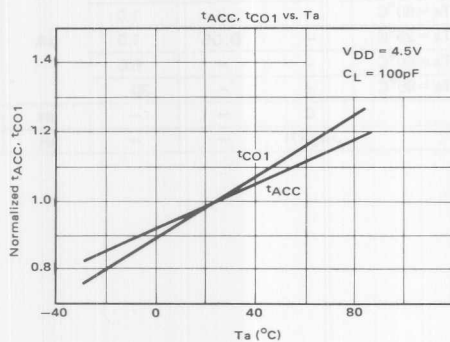
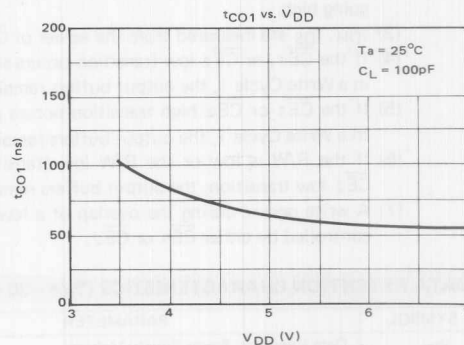
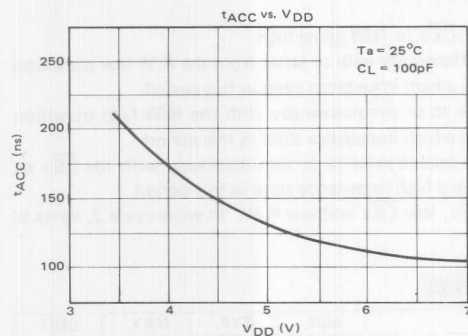
Note (1) t_{RC} : Read Cycle Time.



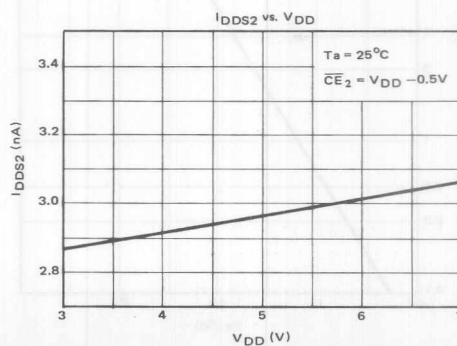
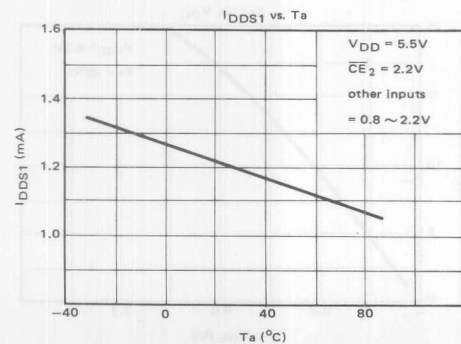
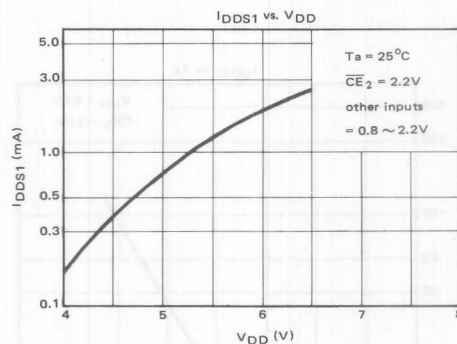
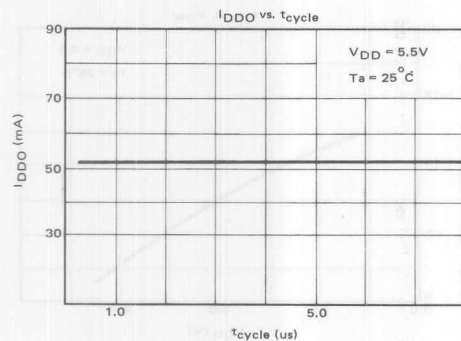
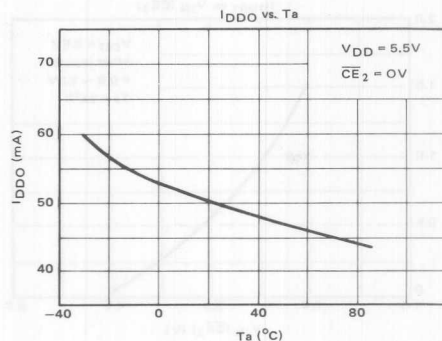
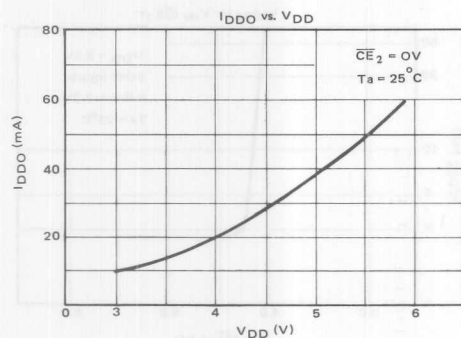
Note: (2) If the V_{IH} level of \overline{CE}_2 is 2.2V, during the period that the V_{DD} voltage is going down from 4.5V to 2.7V, I_{SSD1} current flows. (Refer to D.C. CHARACTERISTICS or TYPICAL CHARACTERISTIC FIGURES.)

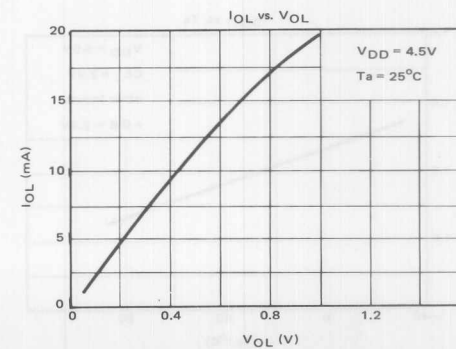
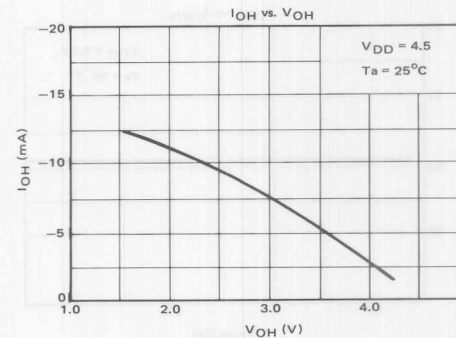
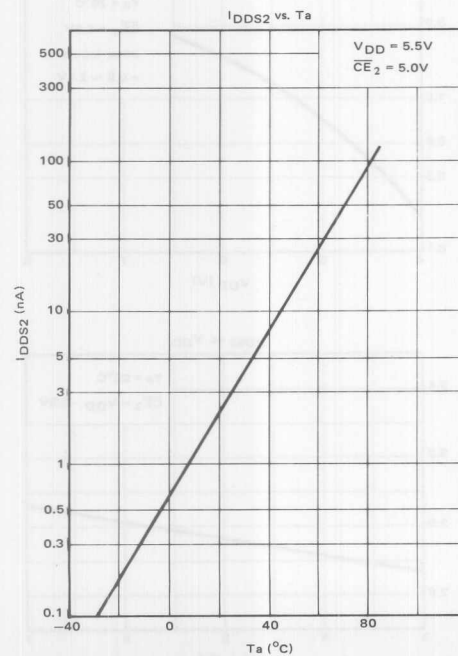
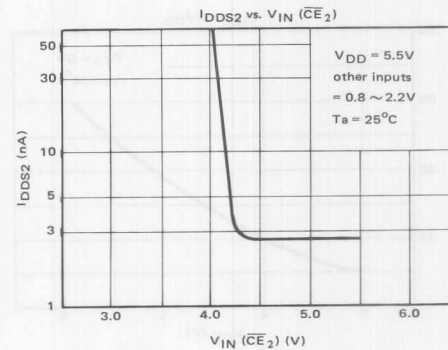
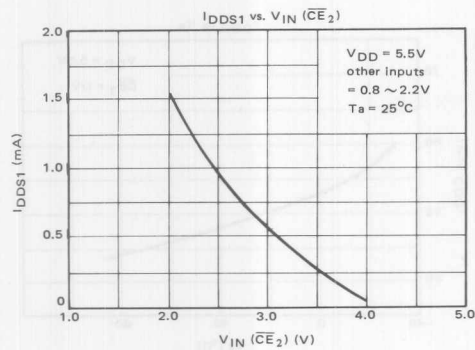
TC5516AP/-2, TC5516APL/-2 TC5516AF/-2, TC5516AFL/-2

TYPICAL CHARACTERISTICS



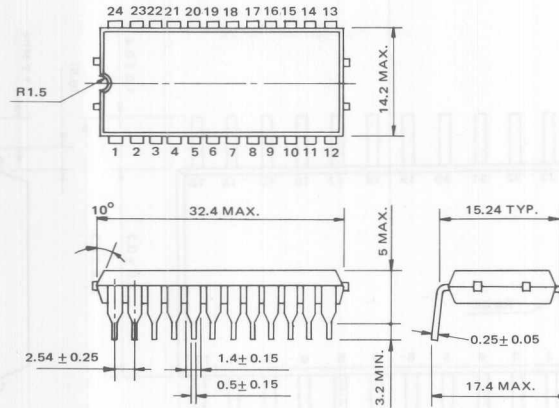
TC5516AP/-2, TC5516APL/-2
TC5516AF/-2, TC5516AFL/-2





OUTLINE DRAWINGS

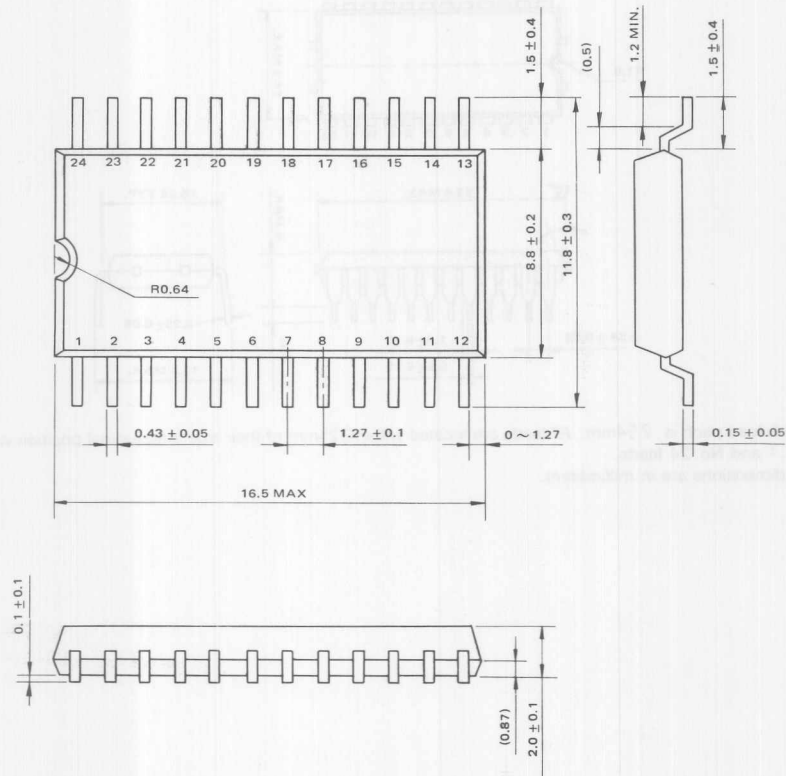
• Plastic DIP



Note : Each lead pitch is 2.54 mm . All leads are located within 0.25 mm of their true longitudinal position with respect to No. 1 and No. 24 leads.
All dimensions are in millimeters.

TC5516AP/-2, TC5516APL/-2
TC5516AF/-2, TC5516AFL/-2

● Plastic FP



Note : Each lead pitch is 1.27mm. All leads are located within 0.1mm of their true longitudinal position with respect to No.1 and No.24 leads.

PACKAGE INFORMATION FOR FLAT PACKAGE

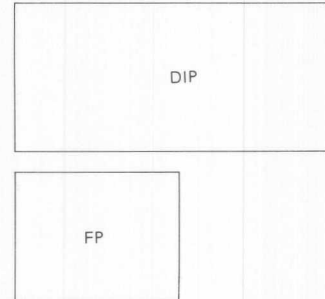
This new flat package is a very small and thin compared with conventional standard dual-in-line package. Differences are as follows.

1. Difference in dimension between flat and standard package.

Unit : mm

| | Flat package | Standard package |
|------------|--------------|------------------|
| Length | 16.5 | 32.4 |
| Width | 9.0 | 14.2 |
| Lead Pitch | 1.27 | 2.54 |
| Thickness | 2.1 | 5 |

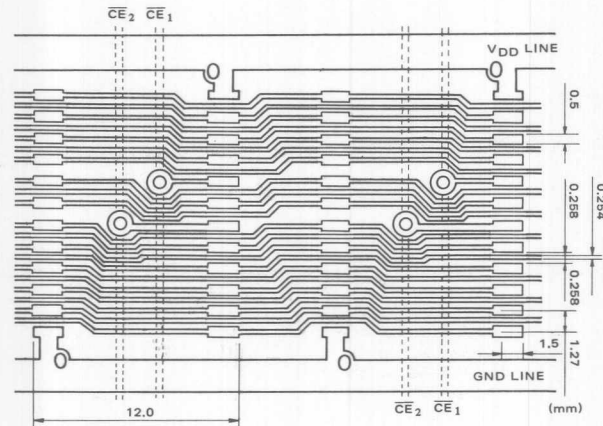
2. Comparison in occupied space.



3. Advantage of this package

- Small dimensions
- Capability of High Density Assembly
- Capability of thin Assembly — Capability of Assembly on both side of PC board.

4. PC pattern layout example



TC5516AP/-2, TC5516APL/-2 TC5516AF/-2, TC5516AFL/-2

FEATURES AND ADVANTAGES FOR FLATPACK CASE

The new flat package is very small and this package with conventional standard leads is the package. Dimensions are as follows.

1. Comparison in overall size



2. Difference in dimension between flat and standard package

| Unit: mm | | |
|------------|------------------|--------------|
| | Standard package | Flat package |
| Length | 12.5 | 12.5 |
| Width | 9.5 | 9.5 |
| Lead pitch | 1.27 | 1.27 |
| Thickness | 2.7 | 2 |

3. Advantage of the package

- Small dimension
- Capability of High Density Assembly
- Capability of the Assembly --- Capability of Assembly on both side of PC board

4. PC pattern layout example



Note: Toshiba does not assume any responsibility for use of any circuitry described; no circuit patent licenses are implied, and Toshiba reserves the right, at any time without notice, to change said circuitry.
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TOSHIBA MOS MEMORY PRODUCTS

2,048 WORD × 8 BIT CMOS STATIC RAM
SILICON GATE CMOS

TC5517AP/-2, TC5517APL/-2
TC5517AF/-2, TC5517AFL/-2

DESCRIPTION

The TC5517AP/AF in a 16384-bit static random access memory organized as 2048 words by 8 bits using CMOS technology, and operates from a single 5 volt supply.

The TC5517AP/AF is featured by output enable and chip enable inputs, that is, \overline{OE} for fast memory access and \overline{CE} for a minimum standby current mode, and is suited for low power application where battery operation or battery back up for nonvolatility are required. Furthermore the TC5517APL guaranteed

standby current equal to or less than $1\mu A$ at 60°C ambient temperature is available.

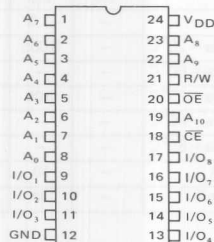
The TC5517AP is also featured by pin compatibility with 2716 type EPROM. This means that the TC5517AP and EPROM can be interchanged in the same socket, and the flexibility in the definition of the quantity of RAM versus EPROM obtained as a result allows the wide application in microcomputer system.

FEATURES

- Standby Current
 - $0.2\mu A$ (Max.) at $T_a = 25^\circ C$ } TC5517APL/AFL
 - $1.0\mu A$ (Max.) at $T_a = 60^\circ C$ }
 - $1.0\mu A$ (Max.) at $T_a = 25^\circ C$ } TC5517AP/AF
 - $5.0\mu A$ (Max.) at $T_a = 60^\circ C$ }
- Low Power Dissipation : 200mW (Typ.)
operating
- Single 5V Power Supply : $5V \pm 10\%$
- Data Retention Supply Voltage: 2.0 ~ 5.5V
- Fully Static Operation

- Access Time
 - 250ns (Max.) : TC5517AP/APL/AF/AFL
 - 200ns (Max.) : TC5517AP-2/APL-2/AF-2/AFL-2
- Two Control Input (\overline{CE} , \overline{OE})
- Pin Compatible with Nch Static RAM TMM2016P
- All Inputs and Outputs Directly TTL Compatible
- Three State Outputs
- Package
 - Plastic DIP : TC5517AP/APL
 - Plastic FP : TC5517AF/AFL

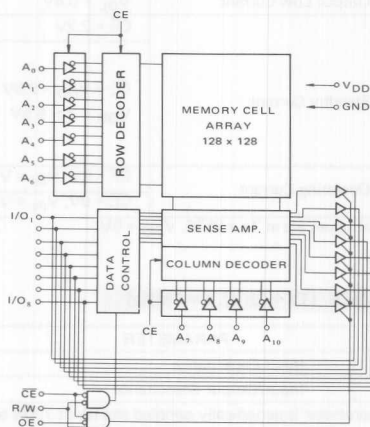
PIN CONNECTION (TOP VIEW)



PIN NAMES

| | |
|--------------------|--------------------------|
| $A_0 \sim A_{10}$ | Address Inputs |
| R/W | Read/Write Control Input |
| \overline{OE} | Output Enable Input |
| \overline{CE} | Chip Enable Input |
| $I/O_1 \sim I/O_8$ | Data Input/Output |
| V_{DD} | Power (+5V) |
| GND | Ground |

BLOCK DIAGRAM



TC5517AP/-2, TC5517APL/-2 TC5517AF/-2, TC5517AFL/-2

ABSOLUTE MAXIMUM RATINGS

| SYMBOL | ITEM | RATING |
|--------------|--|-----------------------|
| V_{DD} | Power Supply Voltage | -0.3V ~ 7.0V |
| V_{IN} | Input Voltage | -0.3V ~ $V_{DD}+0.3V$ |
| $V_{I/O}$ | Input/Output Voltage | -0.3V ~ $V_{DD}+0.3V$ |
| P_D | Power Dissipation ($T_a = 85^\circ\text{C}$) | 0.8W (0.45W)* |
| T_{STG} | Storage Temperature | -55°C ~ 150°C |
| T_{OPR} | Operating Temperature | -30°C ~ 85°C |
| T_{SOLDER} | Soldering Temperature • Time | 260°C • 10 sec. |

*Plastic FP

RECOMMENDED D.C. OPERATING CONDITIONS ($T_a = -30 \sim 85^\circ\text{C}$)

| SYMBOL | PARAMETER | MIN. | TYP. | MAX. | UNIT |
|----------|------------------------|------|------|--------------|------|
| V_{DD} | Power Supply Voltage | 4.5 | 5.0 | 5.5 | V |
| V_{IH} | Input High Voltage | 2.2 | — | $V_{DD}+0.3$ | V |
| V_{IL} | Input Low Voltage | -0.3 | — | 0.8 | V |
| V_{DH} | Data Retention Voltage | 2.0 | — | 5.5 | V |

D.C. CHARACTERISTICS ($T_a = -30 \sim 85^\circ\text{C}$, $V_{DD} = 5V \pm 10\%$)

| SYMBOL | PARAMETER | CONDITIONS | | | MIN. | TYP. | MAX. | UNIT |
|-------------------|-----------------------|--|-------------------|-----------|------|-------|------|------|
| I _{IL} | Input Leakage Current | 0 ≤ V _{IN} ≤ V _{DD} | | | — | — | ±1.0 | μA |
| I _{LO} | I/O Leakage Current | CE = V _{IH} , 0V ≤ V _{I/O} ≤ V _{DD} | | | — | — | ±5.0 | μA |
| I _{OH} | Output High Current | V _{OH} = 2.4V | | | -1.0 | -2.0 | — | mA |
| I _{OL} | Output Low Current | V _{OL} = 0.4V | | | 2.0 | 3.0 | — | mA |
| I _{DDS1} | Standby Current | CE = 2.2V | | | — | 1.0 | 3.0 | mA |
| I _{DDS2} | | CE = V _{DD} - 0.5V V _{DD} = 2 ~ 5.5V | TC5517APL/ AFL | Ta = 25°C | — | 0.005 | 0.2 | μA |
| | | | | Ta = 60°C | — | — | 1.0 | |
| | | | TC5517AP/ AF | Ta = 25°C | — | 0.05 | 1.0 | |
| | | | | Ta = 60°C | — | — | 5.0 | |
| | | | Ta = 85°C | — | — | 30 | | |
| I _{DDO1} | Operating Current | CE = 0V, V _{IN} = V _{IH} /V _{IL} , I _{OUT} = 0mA | | | — | 40 | 70 | mA |
| I _{DDO2} | | CE = 0V, V _{IN} = V _{DD} /GND, I _{OUT} = 0mA | | | — | 30 | 55 | |

Note : Typical values are at $T_a = 25^\circ\text{C}$, $V_{DD} = 5V$.

CAPACITANCE ($T_a = 25^\circ\text{C}$, $f = 1\text{MHz}$)

| SYMBOL | PARAMETER | MIN. | TYP. | MAX. | UNIT |
|-----------|--------------------------|------|------|------|------|
| C_{IN} | Input Capacitance | — | 5 | 10 | pF |
| $C_{I/O}$ | Input/Output Capacitance | — | 5 | 10 | pF |

Note : This parameter is periodically sampled and is not 100% tested.

TC5517AP/-2, TC5517APL/-2 TC5517AF/-2, TC5517AFL/-2

A.C. CHARACTERISTICS (Ta = -30 ~ 85°C, VDD = 5V ± 10%)

• Read Cycle

| SYMBOL | PARAMETER | TC5517AP-2/APL-2 TC5517AF-2/AFL-2 | | TC5517AP/APL TC5517AF/AFL | | UNIT |
|------------------|---------------------------------|--------------------------------------|------|------------------------------|------|------|
| | | MIN. | MAX. | MIN. | MAX. | |
| t _{RC} | Read Cycle Time | 200 | — | 250 | — | ns |
| t _{ACC} | Access Time | — | 200 | — | 250 | ns |
| t _{OE} | OE to Output Valid | — | 100 | — | 100 | ns |
| t _{CO} | CE to Output Valid | — | 200 | — | 250 | ns |
| t _{COE} | OE or CE to Output Active | 10 | — | 10 | — | ns |
| t _{OD} | Output High-Z from Deselection | — | 80 | — | 80 | ns |
| t _{OH} | Output Hold from Address Change | 10 | — | 10 | — | ns |

• Write Cycle

| SYMBOL | PARAMETER | TC5517AP-2/APL-2 TC5517AF-2/AFL-2 | | TC5517AP/APL TC5517AF/AFL | | UNIT |
|------------------|------------------------|--------------------------------------|------|------------------------------|------|------|
| | | MIN. | MAX. | MIN. | MAX. | |
| t _{WC} | Write Cycle Time | 200 | — | 250 | — | ns |
| t _{WP} | Write Pulse Width | 160 | — | 200 | — | ns |
| t _{AW} | Address Set Up Time | 0 | — | 0 | — | ns |
| t _{WR} | Write Recovery Time | 10 | — | 10 | — | ns |
| t _{ODW} | Output High-Z from R/W | — | 80 | — | 80 | ns |
| t _{OEW} | Output Active from R/W | 10 | — | 10 | — | ns |
| t _{DS} | Data Set Up Time | 80 | — | 120 | — | ns |
| t _{DH} | Data Hold Time | 0 | — | 0 | — | ns |

A.C. TEST CONDITIONS

Output Load : 100pF + 1TTL Gate

Input Pulse Levels : 0.6V, 2.4V

Timing Measurement Reference Levels

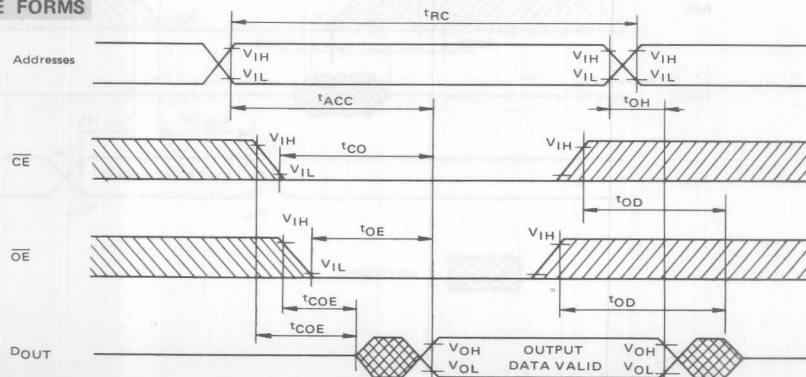
Input : 0.8V and 2.2V

Output : 0.8V and 2.2V

Input Pulse Rise and Fall Times : 10ns

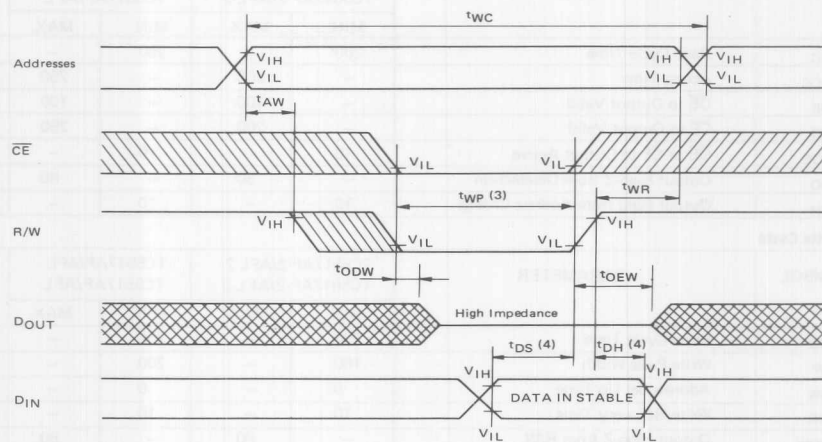
TIMING WAVE FORMS

• Read Cycle (1)

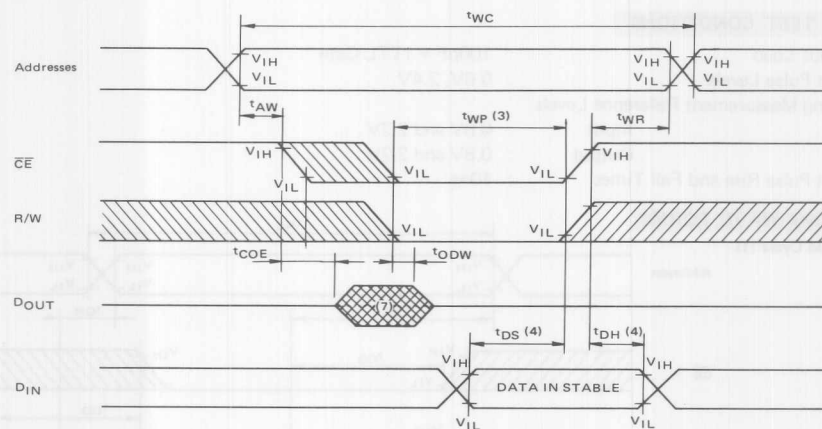


TC5517AP/-2, TC5517APL/-2 TC5517AF/-2, TC5517AFL/-2

• Write Cycle 1 (1)



• Write Cycle 2 (2)



 : UNKNOWN

NOTE: (1) R/W is high for a Read Cycle.

(2) $\overline{OE} = V_{IH}$ or V_{IL} . If $\overline{OE} = V_{IH}$ during write cycle, the output buffers remain in a high impedance state.

(3) t_{WP} is specified as the logical "AND" of \overline{CE} and R/W.

t_{WP} is measured from the latter of \overline{CE} of R/W going low to the earlier of \overline{CE} or R/W going high.

(4) t_{DH} , t_{DS} are measured from the earlier of \overline{CE} of R/W going high.

(5) If the \overline{CE} low transition occurs simultaneously with or latter from the R/W low transition in a Write Cycle 1, the output buffers remain in a high impedance state in this period.

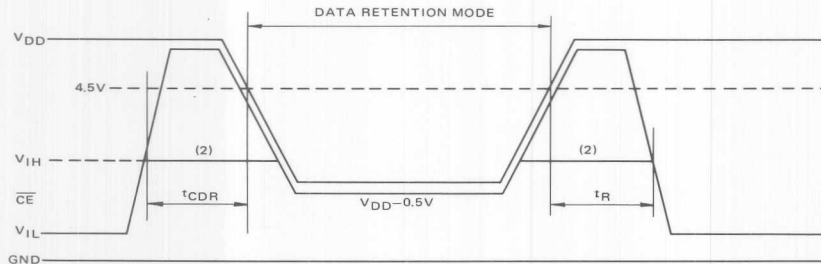
(6) If the \overline{CE} high transition occurs prior to or simultaneously with the R/W high transition in a Write Cycle 1, the output buffers remain in a high impedance state in this period.

(7) If the R/W is low or the R/W low transition occurs prior to or simultaneously with the \overline{CE} low transition, the output buffers remain in high impedance state in this period.

DATA RETENTION CHARACTERISTICS ($T_a = -30 \sim 85^\circ\text{C}$)

| SYMBOL | PARAMETER | | MIN. | TYP. | MAX. | UNIT |
|------------|--|-------------------|--------------------------|------|-------|---------------|
| V_{DH} | Data Retention Power Supply Voltage | | 2.0 | — | 5.5 | V |
| I_{DDS2} | Standby Current | TC5517APL/ AFL | $T_a = 25^\circ\text{C}$ | — | 0.005 | 0.2 |
| | | | $T_a = 60^\circ\text{C}$ | — | — | 1.0 |
| | | TC5517AP/ AF | $T_a = 25^\circ\text{C}$ | — | 0.05 | 1.0 |
| | | | $T_a = 60^\circ\text{C}$ | — | — | 5.0 |
| | | | $T_a = 85^\circ\text{C}$ | — | — | 30 |
| t_{CDR} | From Chip Deselection to Data Retention Mode | | 0 | — | — | μs |
| t_R | Recovery Time | | $t_{RC}(1)$ | — | — | μs |

Note (1) t_{RC} : Read Cycle Time

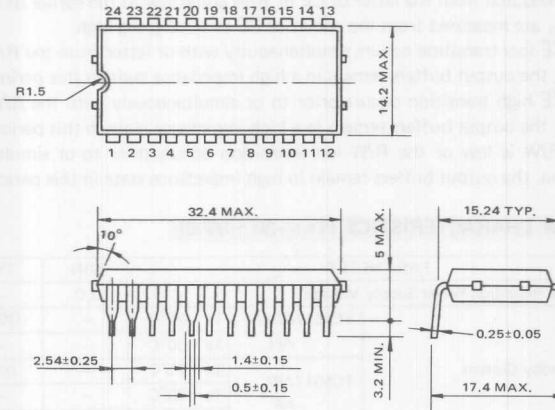


Note (2) If the V_{IH} level of \overline{CE} is 2.2V, during the period that the V_{DD} voltage is going down from 4.5V to 2.7V, I_{DDs1} current flows.

TC5517AP/-2, TC5517APL/-2 TC5517AF/-2, TC5517AFL/-2

OUTLINE DRAWINGS

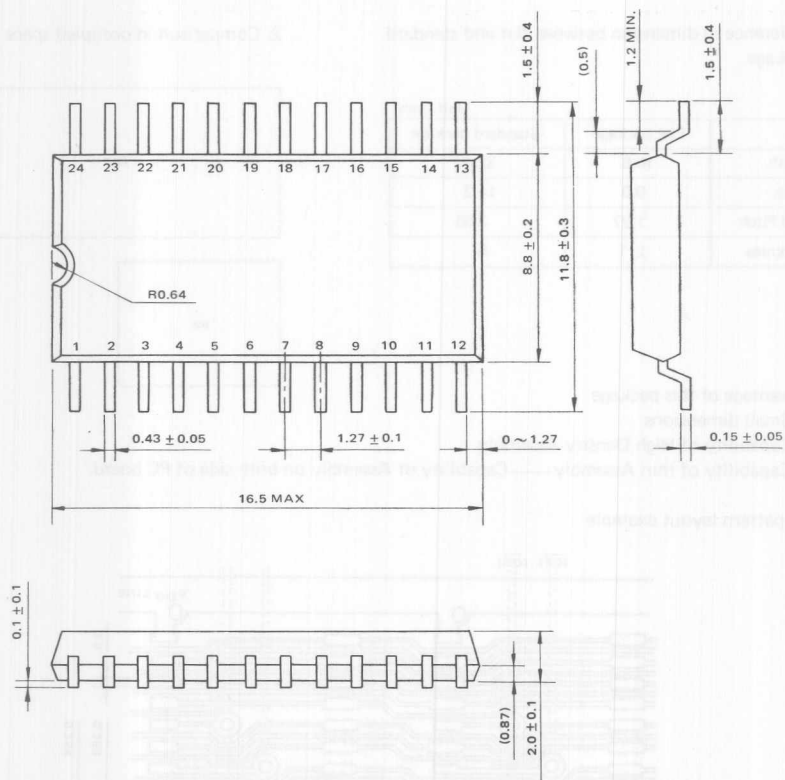
- Plastic DIP



Note : Each lead pitch is 2.54mm. All leads are located within 0.25mm of their true longitudinal position with respect to No. 1 and No. 24 leads.
All dimensions are in millimeters.

TC5517AP/-2, TC5517APL/-2 TC5517AF/-2, TC5517AFL/-2

● Plastic FP



Note : Each lead pitch is 1.27mm. All leads are located within 0.1mm of their true longitudinal position with respect to No.1 and No.24 leads.

TC5517AP/-2, TC5517APL/-2 TC5517AF/-2, TC5517AFL/-2

PACKAGE INFORMATION FOR FLAT PACKAGE

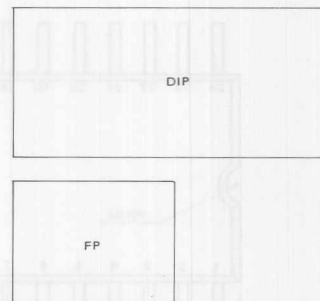
This new flat package is a very small and thin compared with conventional standard dual-in-line package. Differences are as follows.

1. Difference in dimension between flat and standard package.

Unit: mm

| | Flat package | Standard package |
|------------|--------------|------------------|
| Length | 16.5 | 32.4 |
| Width | 9.0 | 14.2 |
| Lead Pitch | 1.27 | 2.54 |
| Thickness | 2.1 | 5 |

2. Comparison in occupied space



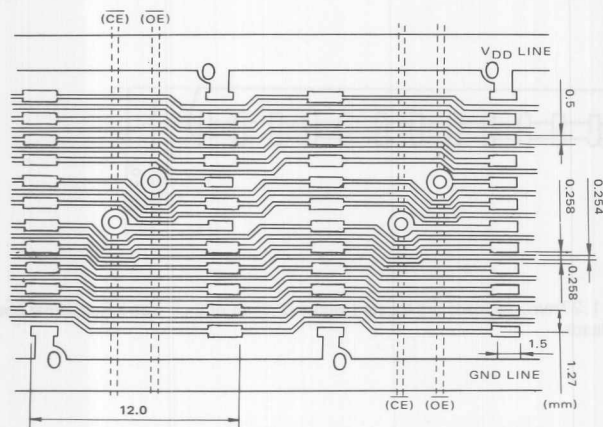
3. Advantage of this package

Small dimensions

Capability of High Density Assembly

Capability of thin Assembly — Capability of Assembly on both side of PC board.

4. PC pattern layout example



Note: Toshiba does not assume any responsibility for use of any circuitry described; no circuit patent licenses are implied, and Toshiba reserves the right, at any time without notice, to change said circuitry.

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TOSHIBA MOS MEMORY PRODUCTS

2,048 WORD \times 8 BIT CMOS STATIC RAM
SILICON GATE CMOS

TC5517BP-20/BPL-20/BP-25/BPL-25
TC5517BF-20/BFL-20/BF-25/BFL-25

DESCRIPTION

The TC5517BP/BF is a 16384-bit high speed and low power fully static random access memory organized as 2048 words by 8 bits using CMOS technology, and operates from a single 5 volt supply.

The TC5517BP/BF has a output enable input (\overline{OE}) for fast memory access and output control and chip enable input (\overline{CE}) which is used for device selection and can be used in order to achieve the minimum standby current mode easily for battery back up.

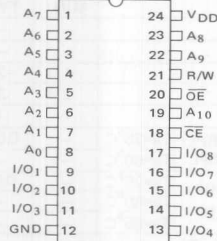
Also the high speed and low power characteristics which maximum access time is 200ns and maximum operating current is 5mA/MHz are achieved.

FEATURES

- Low Power Dissipation
27.5mW/MHz (Max.) Operating
- Standby Current
0.2 μ A (Max.) at $T_a=25^\circ\text{C}$ } TC5517BPL-20/BPL-25/
1.0 μ A (Max.) at $T_a=60^\circ\text{C}$ } BFL-20/BFL-25
1.0 μ A (Max.) at $T_a=25^\circ\text{C}$ } TC5517BP-20/BP-25
5.0 μ A (Max.) at $T_a=60^\circ\text{C}$ } BF-20/BF-25
- Single 5V Power Supply : $5V \pm 10\%$
- Data Retention Supply Voltage 2.0 ~ 5.5V
- Fully Static Operation

PIN CONNECTION

(TOP VIEW)



PIN NAMES

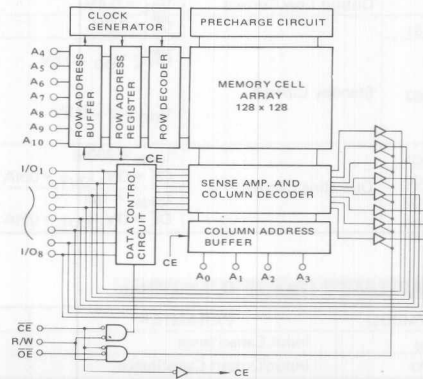
| | |
|--------------------|--------------------------|
| $A_0 \sim A_{10}$ | Address Inputs |
| R/W | Read/Write Control Input |
| \overline{OE} | Output Enable Input |
| \overline{CE} | Chip Enable Input |
| $I/O_1 \sim I/O_8$ | Data Input/Output |
| V_{DD} | Power (+5V) |
| GND | Ground |

Thus the TC5517BP/BF is most suitable for use in low power applications where battery operations or battery back up for nonvolatility are required. Furthermore the TC5517BPL/BFL guaranteed a standby current equal to or less than 1 μ A at 60 $^\circ\text{C}$ ambient temperature available.

And the TC5517BP is pin compatible with 2716 type EPROM. This means that the TC5517BP and EPROM can be interchanged in the same socket, and the flexibility in the definition of the quantity of RAM versus EPROM allows the wide application in microcomputer system.

- Fast Access Time
 $t_{acc}=200\text{ns}(\text{Max.})$: TC5517BP-20/BPL-20/BF-20/
/BFL-20
 $t_{acc}=250\text{ns}(\text{Max.})$: TC5517BP-25/BPL-25/BF-25/
/BFL-25
- Output Buffer Control : \overline{OE}
- On-chip Address Transition Detector
- All inputs and outputs Directly TTL Compatible
- Three State Outputs
- Package
Plastic DIP : TC5517BP-20/BPL-20/BP-25/
BPL-25
Plastic FP : TC5517BF-20/BFL-20/BF-25/
BFL-25

BLOCK DIAGRAM



TC5517BP-20/BPL-20/BP-25/BPL-25 TC5517BF-20/BFL-20/BF-25/BFL-25

OPERATION MODE

| MODE | CE | OE | R/W | A ₀ ~ A ₁₀ | I/O ₁ ~ s | POWER |
|-----------------|----|----|-----|----------------------------------|----------------------|------------------|
| Read | L | L | H | Stable | Data Out | I _{DDO} |
| Write | L | * | L | Stable | Data In | I _{DDO} |
| Output Deselect | L | H | H | * | High Impedance | I _{DDO} |
| **Standby | H | * | * | * | High Impedance | I _{DDS} |

Note: *: H or L **: Data Retention Mode

ABSOLUTE MAXIMUM RATINGS

| SYMBOL | ITEM | RATING |
|---------------------|-------------------------------|--------------------------------|
| V _{DD} | Power Supply Voltage | -0.3V ~ 7.0V |
| V _{IN} | Input Voltage | -0.3V ~ V _{DD} + 0.3V |
| V _{I/O} | Input/Output Voltage | -0.3V ~ V _{DD} + 0.3V |
| P _D | Power Dissipation (Ta = 85°C) | 0.8W (0.45W) * |
| T _{STG} | Storage Temperature | -55°C ~ 150°C |
| T _{OPR} | Operating Temperature | -30°C ~ 85°C |
| T _{SOLDER} | Soldering Temperature · Time | 260 °C · 10 sec. |

* Plastic FP = 0.45W

RECOMMENDED D.C. OPERATING CONDITIONS (Ta = -30 ~ 85°C)

| SYMBOL | PARAMETER | MIN. | TYP. | MAX. | UNIT |
|-----------------|------------------------|------|------|-----------------------|------|
| V _{DD} | Power Supply Voltage | 4.5 | 5.0 | 5.5 | V |
| V _{IH} | Input High Voltage | 2.2 | — | V _{DD} + 0.3 | V |
| V _{IL} | Input Low Voltage | -0.3 | — | 0.8 | V |
| V _{DH} | Data Retention Voltage | 2.0 | — | 5.5 | V |

D.C. CHARACTERISTICS (Ta = -30 ~ 85°C, V_{DD} = 5V ± 10%)

| SYMBOL | PARAMETER | CONDITIONS | | MIN. | TYP. | MAX. | UNIT |
|-------------------|-----------------------|--|--|---------|------|-------|------|
| I _{IL} | Input Leakage Current | 0 ≤ V _{IN} ≤ V _{DD} | | — | — | ±1.0 | μA |
| I _{LO} | I/O Leakage Current | CE = V _{IH} , 0V ≤ V _{I/O} ≤ V _{DD} | | — | — | ±5.0 | μA |
| I _{OH} | Output High Current | V _{OH} = 2.4V | | −1.0 | −2.0 | — | mA |
| I _{OL} | Output Low Current | V _{OL} = 0.4V | | 2.0 | 3.0 | — | mA |
| I _{DDS1} | Standby Current | CE = 2.2V | | — | 1.0 | 3.0 | mA |
| I _{DDS2} | | CE ≥ V _{DD} − 0.5V | TC5517BPL/ BFL | Ta=25°C | — | 0.005 | 0.2 |
| | | | | Ta=60°C | — | — | 1.0 |
| | | V _{DD} = 2 ~ 5.5V | TC5517BP/ BF | Ta=25°C | — | 0.05 | 1.0 |
| | | | | Ta=60°C | — | — | 5.0 |
| I _{DDO1} | Operating Current | t _{cycle} = 1μs | V _{IN} = V _{DD} /GND | Ta=85°C | — | — | 30 |
| | | | | — | — | — | 30 |
| | | | | — | — | — | 25 |
| | | | | — | — | — | 10 |
| I _{DDO2} | Operating Current | CE = 0V, I _{OUT} = 0mA | V _{IN} = V _{DD} /GND | — | — | 5 | mA |
| I _{DDO3} | | | | — | — | — | |
| I _{DDO4} | | | | — | — | — | |

Note: Typical Values are at Ta = 25°C, V_{DD} = 5V.

CAPACITANCE (Ta = 25°C, f = 1MHz)

| SYMBOL | PARAMETER | MIN. | TYP. | MAX. | UNIT |
|------------------|--------------------------|------|------|------|------|
| C _{IN} | Input Capacitance | — | 5 | 10 | pF |
| C _{I/O} | Input/Output Capacitance | — | 5 | 10 | pF |

Note: This paramter is periodically sampled and is not 100% tested.

TC5517BP-20/BPL-20/BP-25/BPL-25 TC5517BF-20/BFL-20/BF-25/BFL-25

A.C. CHARACTERISTICS ($T_a = -30 \sim 85^\circ\text{C}$, $V_{DD} = 5V \pm 10\%$)

• Read Cycle

| SYMBOL | PARAMETER | TC5517BP-20/BPL-20 TC5517BF-20/BFL-20 | | TC5517BP-25/BPL-25 TC5517BF-25/BFL-25 | | UNIT |
|-----------|---|--|------|--|------|------|
| | | MIN. | MAX. | MIN. | MAX. | |
| t_{RC} | Read Cycle Time | 200 | — | 250 | — | ns |
| t_{ACC} | Access Time | — | 200 | — | 250 | |
| t_{OE} | \overline{OE} to Output valid | — | 100 | — | 120 | |
| t_{CO} | \overline{CE} to Output Valid | — | 200 | — | 250 | |
| t_{COE} | \overline{OE} or \overline{CE} to Output Active | 10 | — | 10 | — | |
| t_{OD} | Output High-Z from Deselection | — | 60 | — | 70 | |
| t_{OH} | Output Hold from Address Change | 20 | — | 20 | — | |

• Write Cycle

| SYMBOL | PARAMETER | TC5517BP-20/BPL-20 TC5517BF-20/BFL-20 | | TC5517BP-25/BPL-25 TC5517BF-25/BFL-25 | | UNIT |
|-----------|------------------------|--|------|--|------|------|
| | | MIN. | MAX. | MIN. | MAX. | |
| t_{WC} | Write Cycle Time | 200 | — | 250 | — | ns |
| t_{WP} | Write Pulse Width | 150 | — | 170 | — | |
| t_{AW} | Address set up Time | 0 | — | 0 | — | |
| t_{WR} | Write Recovery Time | 0 | — | 0 | — | |
| t_{ODW} | Output High-Z from R/W | — | 60 | — | 70 | |
| t_{OEw} | Output Active from R/W | 10 | — | 10 | — | |
| t_{DS} | Data set up Time | 90 | — | 100 | — | |
| t_{DH} | Data Hold Time | 0 | — | 0 | — | |

A.C. TEST CONDITIONS

Output Load : 100pF + 1TTL Gate

Input Pulse Levels : 0.6V, 2.4V

Timing Measurement Reference Levels

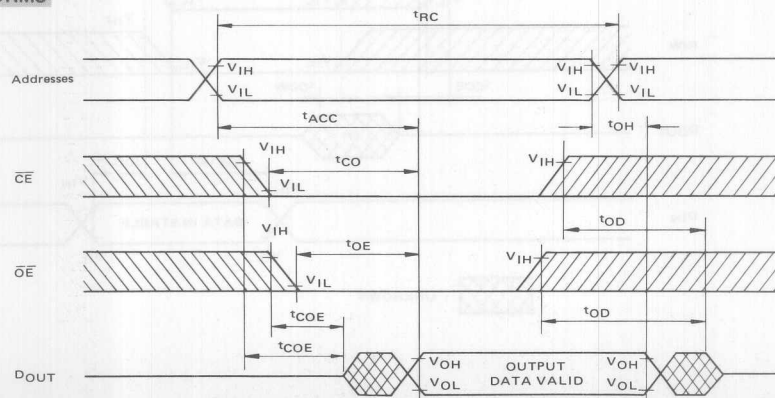
Input : 0.8V and 2.2V

Output : 0.8V and 2.2V

Input Pulse Rise and Fall Times : 10ns

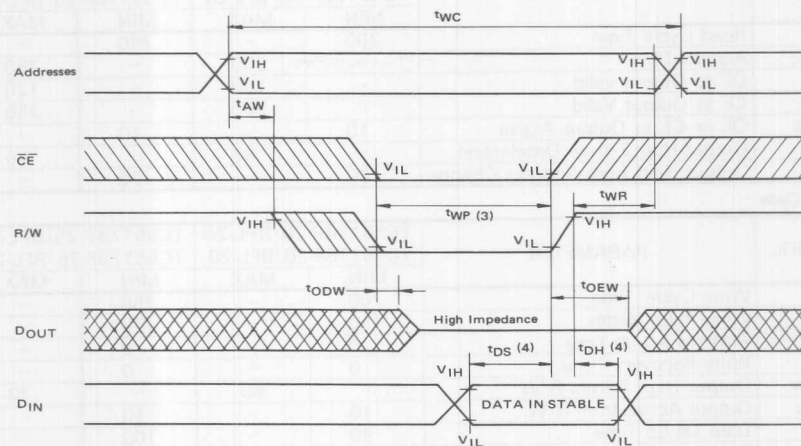
TIMING WAVEFORMS

• Read Cycle (1)

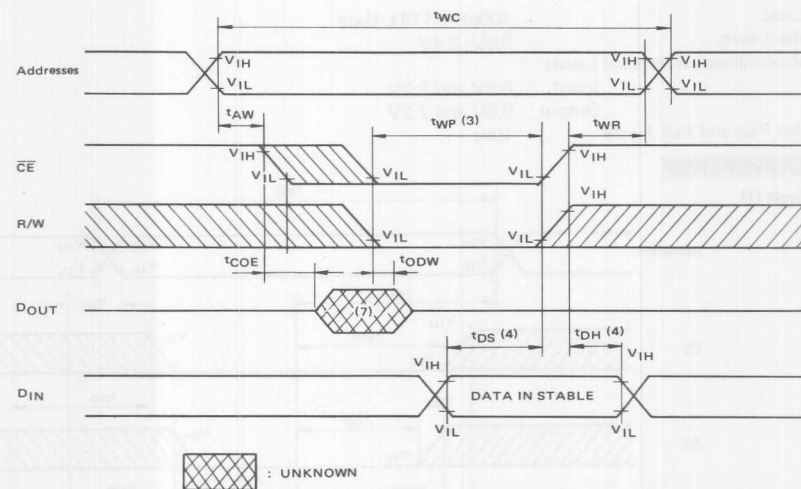


TC5517BP-20/BPL-20/BP-25/BPL-25 TC5517BF-20/BFL-20/BF-25/BFL-25

• Write Cycle 1 (2)



• Write Cycle 2 (2)



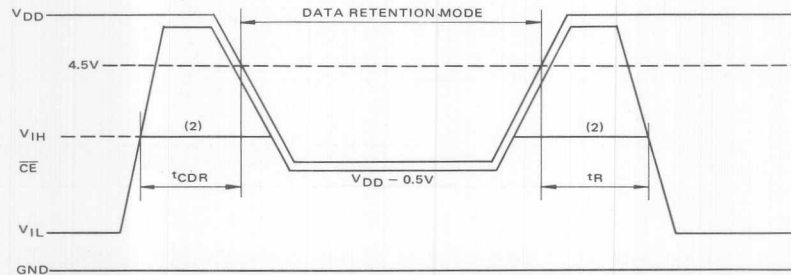
TC5517BP-20/BPL-20/BP-25/BPL-25 TC5517BF-20/BFL-20/BF-25/BFL-25

- Note: (1) R/W is high for a Read Cycle.
 (2) $\overline{OE} = V_{IH}$ or V_{IL} . If, $\overline{OE} = V_{IH}$ during write cycle, the output buffers remain in a high impedance state.
 (3) t_{WP} is specified as the logical "AND" of \overline{CE} and R/W.
 t_{WP} is measured from the latter of \overline{CE} or R/W going low to the earlier of \overline{CE} or R/W going high.
 (4) t_{DH} , t_{DS} are measured from the earlier of \overline{CE} or R/W going high.
 (5) If the \overline{CE} low transition occurs simultaneously with or latter from the R/W low transition in a Write Cycle 1, the output buffers remain in a high impedance state in this period.
 (6) If the \overline{CE} high transition occurs prior to or simultaneously with the R/W high transition in a Write Cycle 1, the output buffers remain in a high impedance state in this period.
 (7) If the R/W is low or the R/W low transition occurs prior to or simultaneously with the \overline{CE} low transition, the output buffers remain in high impedance state in this period.

DATA RETENTION CHARACTERISTICS (Ta = -30 ~ 85°C)

| SYMBOL | PARAMETER | | | | MIN. | TYP. | MAX. | UNIT |
|-------------------|--|-------------------|---------|---|---------------------|------|------|------|
| V _{DH} | Data Retention Power Supply Voltage | | | | 2.0 | — | 5.5 | V |
| I _{DDS2} | Standby Current | TC5517BPL/ BFL | Ta=25°C | — | 0.005 | 0.2 | μA | |
| | | | Ta=60°C | — | — | 1.0 | | |
| | | TC5517BP/ BF | Ta=25°C | — | 0.05 | 1.0 | | |
| | | | Ta=60°C | — | — | 5.0 | | |
| | | | Ta=85°C | — | — | 30 | | |
| t _{CDR} | From Chip Deselection to Data Retention Mode | | | | 0 | — | — | μs |
| t _R | Recovery Time | | | | t _{RC} (1) | — | — | μs |

Note (1) t_{RC} : Read Cycle Time

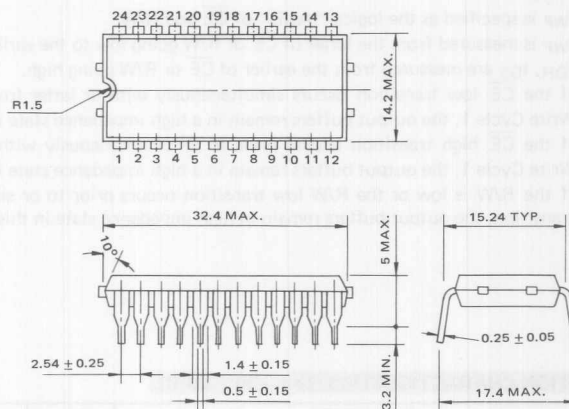


Note (2) If the V_{IH} level of \overline{CE} is 2.2V, during the period that the V_{DD} voltage is going down from 4.5V to 2.7V, I_{DDS1} current flows.

TC5517BP-20/BPL-20/BP-25/BPL-25 TC5517BF-20/BFL-20/BF-25/BFL-25

OUTLINE DRAWINGS

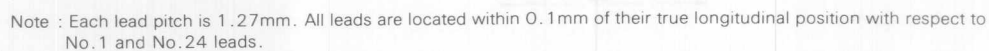
- Plastic DIP



Note : Each lead pitch is 2.54mm. All leads are located within 0.25mm of their true longitudinal position with respect to No.1 and No.24 leads.

All dimensions are in millimeters.

- Plastic FP



TC5517BP-20/BPL-20/BP-25/BPL-25 TC5517BF-20/BFL-20/BF-25/BFL-25

PACKAGE INFORMATION FOR FLAT PACKAGE

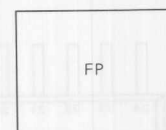
This new flat package is a very small and thin compared with conventional standard dual-in-line package. Differences are as follows.

1. Difference in dimension between flat and standard package.

Unit :mm

| | Flat package | Standard package |
|------------|--------------|------------------|
| Length | 16.5 | 32.4 |
| Width | 9.0 | 14.2 |
| Lead Pitch | 1.27 | 2.54 |
| Thickness | 2.1 | 5 |

2. Comparison in occupied space



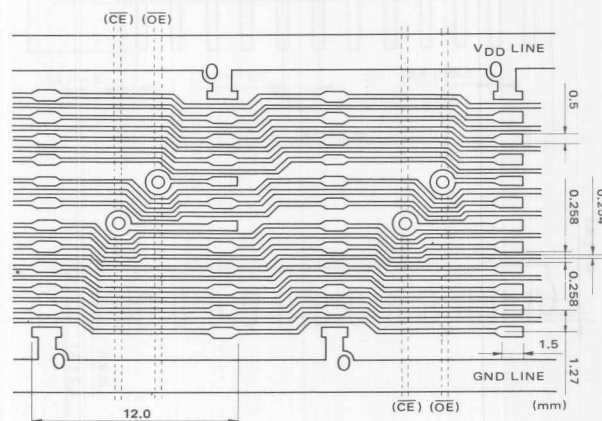
3. Advantage of this package

Small dimensions

Capability of High Density Assembly

Capability of thin Assembly — Capability of Assembly on both side of PC board.

4. PC pattern layout example



Note: Toshiba does not assume any responsibility for use of any circuitry described; no circuit patent licenses are implied, and Toshiba reserves the right, at any time without notice, to change said circuitry.

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TOSHIBA MOS MEMORY PRODUCTS

2,048 WORD \times 8 BIT CMOS STATIC RAM
SILICON GATE CMOS

TC5518BP-20/BPL-20/BP-25/BPL-25
TC5518BF-20/BFL-20/BF-25/BFL-25

DESCRIPTION

The TC5518BP/BF is a 16384-bit high speed and low power fully static random access memory organized as 2048 words by 8 bits using CMOS technology, and operates from a single 5 volt supply.

The TC5518BP/BF has two chip enable inputs, \overline{CE}_1 and \overline{CE}_2 , which are used for device selection and can be used in order to achieve the minimum standby current mode easily for battery back up. Also the high speed and low power characteristics which maximum access time is 200ns and maximum operating current is 5mA/MHz are achieved.

Thus the TC5518BP/BF is most suitable for use in

low power applications where battery operation or battery back up for nonvolatility are required. Furthermore the TC5518BPL/BFL guaranteed a standby current equal to or less than $1\mu A$ at $60^\circ C$ ambient temperature available.

And the TC5518BP is pin compatible with 2716 type EPROM. This means that the TC5518BP and EPROM can be interchanged in the same socket, and the flexibility in the definition of the quantity of RAM versus EPROM allows the wide application in microcomputer system.

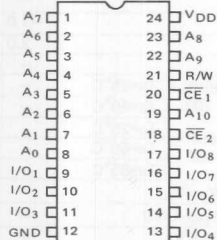
FEATURES

- Low Power Dissipation
27.5mW/MHz (Max.) Operating
- Standby Current
 $0.2\mu A$ (Max.) at $T_a = 25^\circ C$ TC5518BPL/
 $1.0\mu A$ (Max.) at $T_a = 60^\circ C$ BFL-20
 $1.0\mu A$ (Max.) at $T_a = 25^\circ C$ TC5518BP/
 $5.0\mu A$ (Max.) at $T_a = 60^\circ C$ BF-20
- Single 5V Power Supply: $5V \pm 10\%$
- Data Retention Supply Voltage
2.0 ~ 5.5V
- Fully Static Operation

- Fast Access Time
 $t_{acc} = 200ns$ (Max.): TC5518BP-20/BPL-20/BF-20/
BFL-20
 $t_{acc} = 250ns$ (Max.): TC5518BP-25/BPL-25/BF-25/
BFL-25
- Two Chip Enables (\overline{CE}_1 , \overline{CE}_2) for Simple
Memory Expansion and Battery Back Up
- On-chip Address Transition Detector
- All Inputs and Outputs Directly TTL Compatible
- Three State Outputs
- Package
Plastic DIP: TC5518BP-20/BPL-20/BP-25/
BPL-25
Plastic FP: TC5518BF-20/BFL-20/BF-25/
BFL-25

PIN CONNECTION

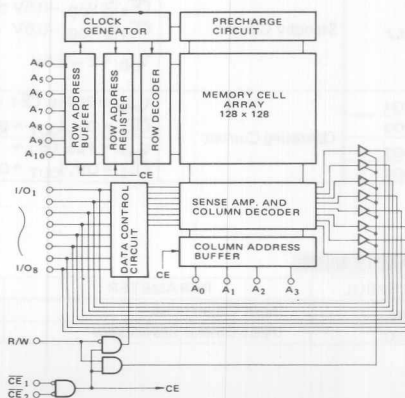
(Top VIEW)



PIN NAMES

| | |
|------------------------------------|--------------------------|
| $A_0 \sim A_{10}$ | Address Inputs |
| R/W | Read/Write Control Input |
| $\overline{CE}_1, \overline{CE}_2$ | Chip Enable Inputs |
| $I/O_1 \sim I/O_8$ | Data Input/Output |
| V_{DD} | Power (+5V) |
| GND | Ground |

BLOCK DIAGRAM



TC5518BP-20/BPL-20/BP-25/BPL-25 TC5518BF-20/BFL-20/BF-25/BFL-25

OPERATION MODE

| MODE | \overline{CE}_2 | \overline{CE}_1 | R/W | $A_0 \sim A_{10}$ | $I/O_1 \sim 8$ | POWER |
|--------------|-------------------|-------------------|-----|-------------------|----------------|-----------|
| Read | L | L | H | Stable | Data Out | I_{DDO} |
| Write | L | L | L | Stable | Data In | I_{DDO} |
| ** Standby 1 | * | H | * | * | High Impedance | I_{DDS} |
| ** Standby 2 | H | * | * | * | High Impedance | I_{DDS} |

Note; *: H or L **: Data Retention Mode

ABSOLUTE MAXIMUM RATINGS

| SYMBOL | ITEM | RATING |
|--------------|--|-----------------------|
| V_{DD} | Power Supply Voltage | -0.3V ~ 7.0V |
| V_{IN} | Input Voltage | -0.3V ~ $V_{DD}+0.3V$ |
| $V_{I/O}$ | Input/Output Voltage | -0.3V ~ $V_{DD}+0.3V$ |
| P_D | Power Dissipation ($T_a = 85^\circ\text{C}$) | 0.8W (0.45W)* |
| T_{STG} | Storage Temperature | -55°C ~ 150°C |
| T_{OPR} | Operating Temperature | -30°C ~ 85°C |
| T_{SOLDER} | Soldering Temperature · Time | 260°C · 10 sec |

*: Plastic FP = 0.45W

RECOMMENDED D.C. OPERATING CONDITIONS ($T_a = -30 \sim 85^\circ\text{C}$)

| SYMBOL | PARAMETER | MIN. | TYP. | MAX. | UNIT |
|----------|------------------------|------|------|--------------|------|
| V_{DD} | Power Supply Voltage | 4.5 | 5.0 | 5.5 | V |
| V_{IH} | Input High Voltage | 2.2 | — | $V_{DD}+0.3$ | V |
| V_{IL} | Input Low Voltage | -0.3 | — | 0.8 | V |
| V_{DH} | Data Retention Voltage | 2.0 | — | 5.5 | V |

D.C. CHARACTERISTICS ($T_a = -30 \sim 85^\circ\text{C}$, $V_{DD} = 5V \pm 10\%$)

| SYMBOL | PARAMETER | CONDITIONS | | MIN. | TYP. | MAX. | UNIT |
|-------------------|-----------------------|---|--|------|-------|------|------|
| I _{IL} | Input Leakage Current | 0 ≤ V _{IN} ≤ V _{DD} | | — | — | ±1.0 | μA |
| I _{LO} | I/O Leakage Current | CE ₂ = V _{IH} , 0V ≤ V _{I/O} ≤ V _{DD} | | — | — | ±5.0 | μA |
| I _{OH} | Output High Current | V _{OH} = 2.4V | | −1.0 | −2.0 | — | mA |
| I _{OL} | Output Low Current | V _{OL} = 0.4V | | 2.0 | 3.0 | — | mA |
| I _{DDS1} | Standby Current | CE ₂ = 2.2V or CE ₁ = 2.2V | | — | 1.0 | 3.0 | mA |
| I _{DDS2} | | TC5518BPL/ BFL | Ta=25°C | — | 0.005 | 0.2 | μA |
| | | | Ta=60°C | — | — | 1.0 | |
| | | TC5518BP/ BF | Ta=25°C | — | 0.05 | 1.0 | |
| | | | Ta=60°C | — | — | 5.0 | |
| I _{DDO1} | Operating Current | t _{cycle} = 200ns, CE ₁ = CE ₂ = 0V, I _{OUT} = 0mA | V _{IN} = V _{IH} /V _{IL} | — | — | 30 | mA |
| I _{DDO2} | | | V _{IN} = V _{DD} /GND | — | — | 25 | |
| I _{DDO3} | | | V _{IN} = V _{IH} /V _{IL} | — | — | 10 | |
| I _{DDO4} | | | V _{IN} = V _{DD} /GND | — | — | 5 | |

Note: Typical Values are at $T_a = 25^\circ\text{C}$, $V_{DD} = 5V$

CAPACITANCE

| SYMBOL | PARAMETER | MIN. | TYP. | MAX. | UNIT |
|-----------|--------------------------|------|------|------|------|
| C_{IN} | Input Capacitance | — | 5 | 10 | pF |
| $C_{I/O}$ | Input/Output Capacitance | — | 5 | 10 | pF |

Note: This parameter is periodically sampled and is not 100% tested.

TC5518BP-20/BPL-20/BP-25/BPL-25 TC5518BF-20/BFL-20/BF-25/BFL-25

A.C. CHARACTERISTICS ($T_a = -30 \sim 85^\circ\text{C}$, $V_{DD} = 5V \pm 10\%$)

Read Cycle

| SYMBOL | PARAMETER | TC5518BP-20/BPL-20 TC5518BF-20/BFL-20 | | TC5518BP-25/BPL-25 TC5518BF-25/BFL-25 | | UNIT |
|-----------|---|--|------|--|------|------|
| | | MIN. | MAX. | MIN. | MAX. | |
| t_{RC} | Read Cycle Time | 200 | — | 250 | — | ns |
| t_{ACC} | Access Time | — | 200 | — | 250 | |
| t_{CO1} | $\overline{CE1}$ to Output Valid | — | 200 | — | 250 | |
| t_{CO2} | $\overline{CE2}$ to Output Valid | — | 200 | — | 250 | |
| t_{COE} | $\overline{CE1}$ or $\overline{CE2}$ to Output Active | 10 | — | 10 | — | |
| t_{OD} | Output High-Z Deselection | — | 60 | — | 70 | |
| t_{OH} | Output Hold from Address Change | 20 | — | 20 | — | |

Write Cycle

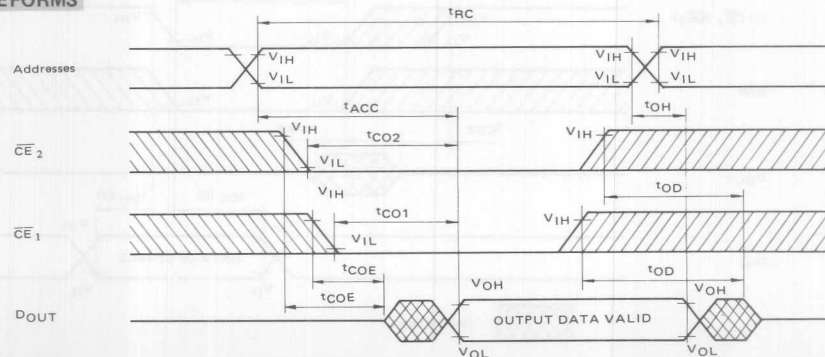
| SYMBOL | PARAMETER | TC5518BP-20/BPL-20 TC5518BF-20/BFL-20 | | TC5518BP-25/BPL-25 TC5518BF-25/BFL-25 | | UNIT |
|-----------|------------------------|--|------|--|------|------|
| | | MIN. | MAX. | MIN. | MAX. | |
| t_{WC} | Write Cycle Time | 200 | — | 250 | — | ns |
| t_{WP} | Write Pulse Width | 150 | — | 170 | — | |
| t_{AW} | Address set up Time | 0 | — | 0 | — | |
| t_{WR} | Write Recovery Time | 0 | — | 0 | — | |
| t_{ODW} | Output High-Z from R/W | — | 60 | — | 70 | |
| t_{OEW} | Output Active from R/W | 10 | — | 10 | — | |
| t_{DS} | Data set up Time | 90 | — | 100 | — | |
| t_{DH} | Data Hold Time | 0 | — | 0 | — | |

A.C. TEST CONDITIONS

Output Load : 100pF + 1TTL Gate
Input Pulse Levels : 0.6V, 2.4V
Timing Measurement Reference Levels
Input : 0.8V and 2.2V
Output : 0.8V and 2.2V
Input Pulse Rise and Fall Times : 10 ns

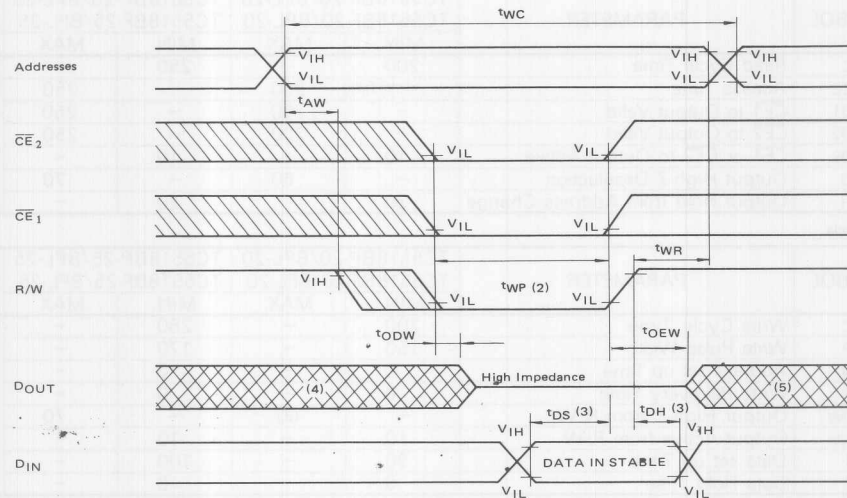
TIMING WAVEFORMS

Read Cycle (1)

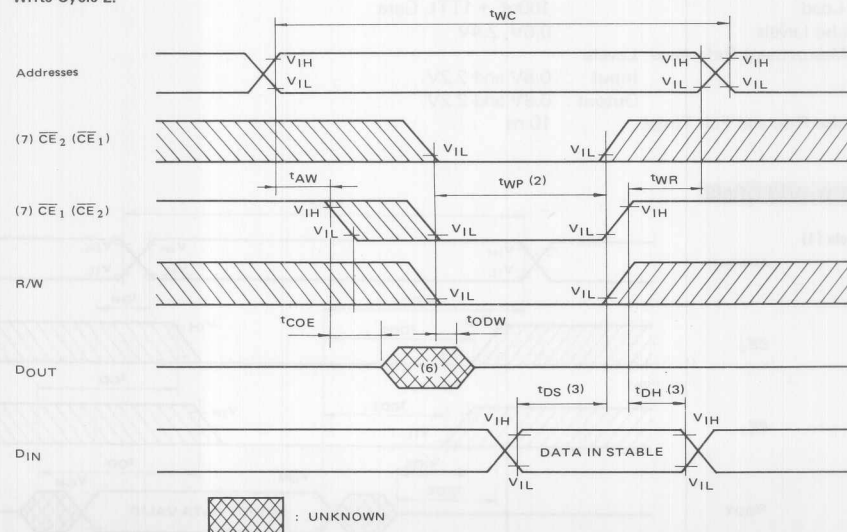


TC5518BP-20/BPL-20/BP-25/BPL-25
TC5518BF-20/BFL-20/BF-25/BFL-25

Write Cycle 1.



Write Cycle 2.



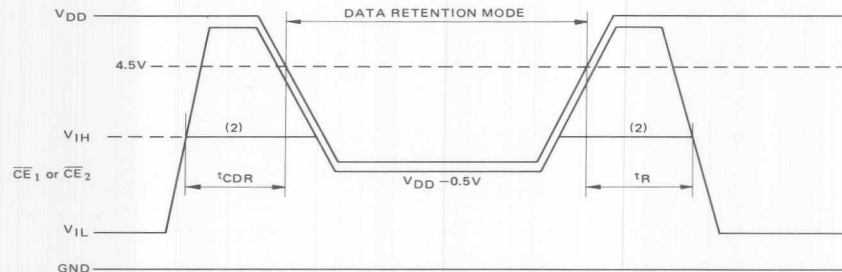
TC5518BP-20/BPL-20/BP-25/BPL-25 TC5518BF-20/BFL-20/BF-25/BFL-25

- Note: (1) R/W is high for a Read Cycle.
 (2) t_{WP} is specified as the logical "AND" of $\overline{CE}1$, $\overline{CE}2$ and R/W.
 t_{WP} is measured from the latter of $\overline{CE}1$, $\overline{CE}2$ or R/W going low to the earlier of $\overline{CE}1$, $\overline{CE}2$ or R/W going high.
 (3) t_{PH} , t_{PS} are measured from the earlier of $\overline{CE}1$, $\overline{CE}2$ or R/W going high.
 (4) If the $\overline{CE}1$, or $\overline{CE}2$ low transition occurs simultaneously with or latter from the R/W low transition in a Write Cycle 1, the output buffers remain in a high impedance state in this period.
 (5) If the $\overline{CE}1$ or $\overline{CE}2$ high transition occurs prior to or simultaneously with the R/W high transition in a Write Cycle 1, the output buffers remain in a high impedance state in this period.
 (6) If the R/W is low or the R/W low transition occurs prior to or simultaneously with the $\overline{CE}1$ or $\overline{CE}2$ low transition, the output buffers remain in a high impedance state in this period.
 (7) A write occurs during the overlap of a low $\overline{CE}1$, low $\overline{CE}2$ and low R/W.
 In write cycle 2, write is controlled by either $\overline{CE}1$ or $\overline{CE}2$.

DATA RETENTION CHARACTERISTICS ($T_a = -30 \sim 85^\circ\text{C}$)

| SYMBOL | PARAMETER | MIN. | TYP. | MAX. | UNIT |
|------------|--|-------------------|------|--------------------------|---------------|
| V_{DH} | Data Retention Power Supply Voltage | 2.0 | — | 5.5 | V |
| I_{DDS2} | Standby Current | TC5518BPL/ BFL | | $T_a = 25^\circ\text{C}$ | 0.2 |
| | | | | $T_a = 60^\circ\text{C}$ | 1.0 |
| | | TC5518BP/ BF | | $T_a = 25^\circ\text{C}$ | 1.0 |
| | | | | $T_a = 60^\circ\text{C}$ | 5.0 |
| | | | | $T_a = 85^\circ\text{C}$ | 30 |
| t_{CDR} | From Chip Deselection to Data Retention Mode | 0 | — | — | μs |
| t_R | Recover Time | $t_{RC}(1)$ | — | — | μs |

Note (1) t_{RC} : Read Cycle Time

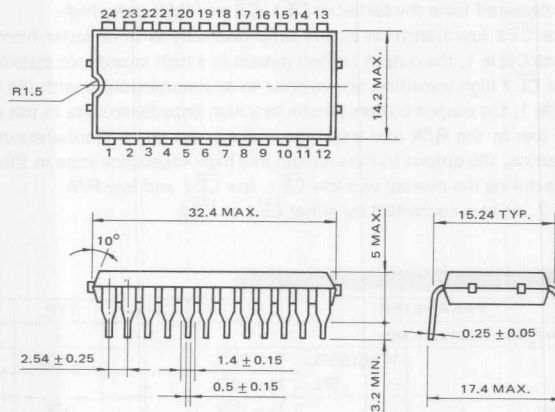


Note (2) if the V_{IH} level of $\overline{CE}2$ ($\overline{CE}1$) is 2.2V, during the period that the V_{DD} voltage is going down from 4.5V to 2.7V, I_{DDS1} current flows.

TC5518BP-20/BPL-20/BP-25/BPL-25
TC5518BF-20/BFL-20/BF-25/BFL-25

OUTLINE DRAWINGS

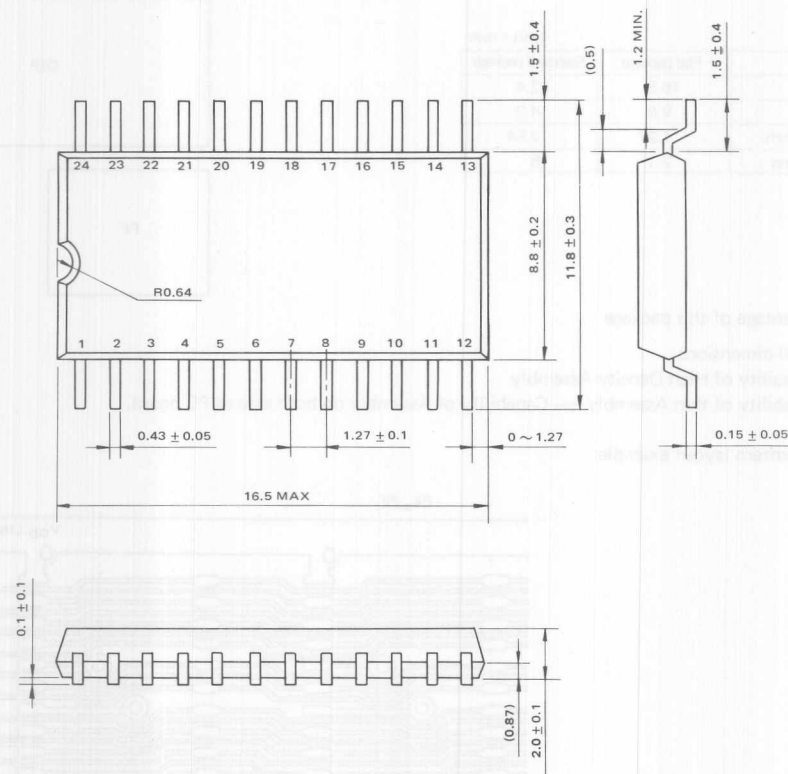
● Plastic DIP



Note : Each lead pitch is 2.54mm. All leads are located within 0.25mm of their true longitudinal position with respect to No.1 and No.24 leads.
All dimensions are in millimeters.

TC5518BP-20/BPL-20/BP-25/BPL-25
TC5518BF-20/BFL-20/BF-25/BFL-25

● Plastic FP



Note : Each lead pitch is 1.27mm. All leads are located within 0.1mm of their true longitudinal position with respect to No.1 and No.24 leads.

TC5518BP-20/BPL-20/BP-25/BPL-25 TC5518BF-20/BFL-20/BF-25/BFL-25

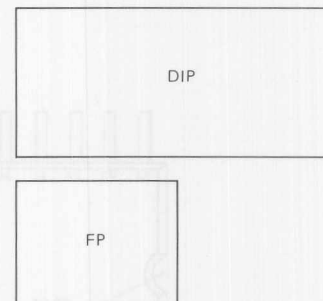
PACKAGE INFORMATION FOR FLAT PACKAGE

This new flat package is a very small and thin compared with conventional standard dual-in-line package. Differences are as follows.

1. Difference in dimension between flat and standard package.
2. Comparison in occupied space

Unit : mm

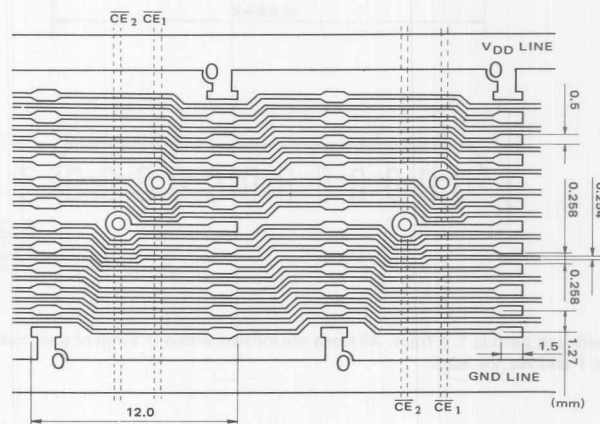
| | Flat package | Standard package |
|------------|--------------|------------------|
| Length | 16.5 | 32.4 |
| Width | 9.0 | 14.2 |
| Lead Pitch | 1.27 | 2.54 |
| Thickness | 2.1 | 5 |



3. Advantage of this package

Small dimensions
Capability of High Density Assembly
Capability of thin Assembly — Capability of Assembly on both side of PC board.

4. PC pattern layout example



Note: Toshiba does not assume any responsibility for use of any circuitry described; no circuit patent licenses are implied, and Toshiba reserves the right, at any time without notice, to change said circuitry.

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TOSHIBA MOS MEMORY PRODUCTS

2,048 WORD \times 8 BIT CMOS STATIC RAM

TC5517CP-15/CPL-15/CP-20/CPL-20
TC5517CF-15/CFL-15/CF-20/CFL-20

DESCRIPTION

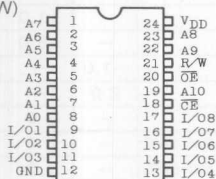
The TC5517CP/CF is a 16384-bit high speed and low power fully static random access memory organized as 2048 words by 8 bits using CMOS technology, and operates from a single 5 volt supply. The TC5517CP/CF has a output enable input (\overline{OE}) for fast memory access and output control and chip enable input (\overline{CE}) which is used for device selection and can be used in order to achieve the minimum standby current mode easily for battery back up. Also the high speed and low power characteristics which maximum access time is 150ns, 200ns and maximum operating current is 5mA/MHz are achieved.

FEATURES

- Low Power Dissipation
27.5mW/MHz(Max.) Operating
- Standby Current
0.2 μ A(Max.) at Ta=25°C, TC5517CPL-15/CPL-20
1.0 μ A(Max.) at Ta=60°C, CFL-15/CFL-20
1.0 μ A(Max.) at Ta=25°C, TC5517CP-15/CP-20
5.0 μ A(Max.) at Ta=60°C, CF-15/CF-20
- Single 5V Power Supply: 5V \pm 10%
- Data Retention Supply Voltage
2.0~5.5V
- Fully Static Operation
- Fast Access Time
t_{acc}=150ns(Max.) : TC5517CP-15/CPL-15
CF-15/CFL-15

PIN CONNECTION

(TOP VIEW)



PIN NAMES

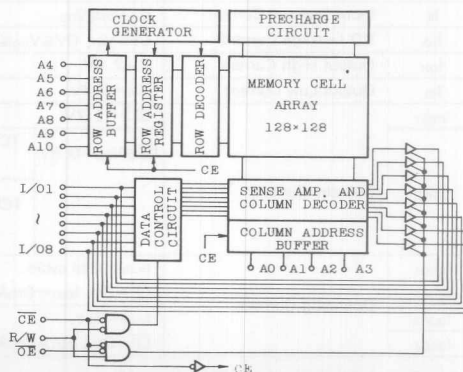
| | |
|------------------------------------|--------------------------|
| A ₀ ~A ₁₀ | Address Inputs |
| R/W | Read/Write Control Input |
| \overline{OE} | Output Enable Input |
| \overline{CE} | Chip Enable Input |
| I/O ₁ ~I/O ₈ | Data Input/Output |
| V _{DD} | Power (+5V) |
| GND | Ground |

Thus the TC5517CP/CF is most suitable for use in low power applications where battery operation or battery back up for nonvolatility are required. Furthermore the TC5517CPL/CFL guaranteed a standby current equal to or less than 1 μ A at 60°C ambient temperature available. And the TC5517CP is pin compatible with 2716 type EPROM. This means that the TC5517CP and EPROM can be interchanged in the same socket and the flexibility in the definition of the quantity of RAM versus EPROM allows the wide application in microcomputer system.

t_{acc}=200ns(Max.) : TC5517CP-20/CPL-20
CF-20/CFL-20

- Output Buffer Control : \overline{OE}
- On-Chip Address Transition Detector
- All Inputs and Outputs Directly TTL Compatible
- Three State Outputs
- Package;
Plastic DIP: TC5517CP-15/CPL-15
(600 mil) CP-20/CPL-20
Plastic FP : TC5517CF-15/CFL-15
CF-20/CFL-20

BLOCK DIAGRAM



TC5517CP-15/CPL-15/CP-20/CPL-20 TC5517CF-15/CFL-15/CF-20/CFL-20

OPERATION MODE

| MODE | \overline{CE} | \overline{OE} | R/W | $A_9 \sim A_{10}$ | I/O ₁ ~I/O ₈ | POWER |
|-----------------|-----------------|-----------------|-----|-------------------|------------------------------------|------------------|
| Read | L | L | H | Stable | Data Out | I _{DDO} |
| Write | L | * | L | Stable | Data In | I _{DDO} |
| Output Deselect | L | H | H | * | High Impedance | I _{DDO} |
| ** Standby | H | * | * | * | High Impedance | I _{DDs} |

ABSOLUTE MAXIMUM RATINGS

| SYMBOL | ITEM | RATING |
|---------------------|----------------------------|-----------------------------|
| V _{DD} | Power Supply Voltage | -0.3~7.0V |
| V _{IN} | Input Voltage | -0.3V~V _{DD} +0.3V |
| V _{I/O} | Input/Output Voltage | -0.3V~V _{DD} +0.3V |
| P _D | Power Dissipation(Ta=85°C) | 0.8W(0.45W)* |
| T _{STG} | Storage Temperature | -55°C~150°C |
| T _{OPR} | Operating Temperature | -30°C~85°C |
| T _{SOLDER} | Soldering Temperature-Time | 260°C-10sec. |

*Plastic FP=0.45W

RECOMMENDED D. C. OPERATING CONDITIONS (Ta = -30~85°C)

| SYMBOL | PARAMETER | MIN. | TYP. | MAX. | UNIT |
|-----------------|------------------------|------|------|----------------------|------|
| V _{DD} | Power Supply Voltage | 4.5 | 5.0 | 5.5 | V |
| V _{IH} | Input High Voltage | 2.2 | — | V _{DD} +0.3 | V |
| V _{IL} | Input Low Voltage | -0.3 | — | 0.8 | V |
| V _{DH} | Data Retention Voltage | 2.0 | — | 5.5 | V |

D. C. CHARACTERISTICS

(Ta=30~85°C, V_{DD}=5V±10%)

| SYMBOL | PARAMETER | CONDITIONS | | TC5517CP-15/CF-15 | | TC5517CP-20/CF-20 | | UNIT | | |
|-------------------|-----------------------|--|----------------|--|------|-------------------|------|------|----|----|
| | | | | MIN. | MAX. | MIN. | MAX. | | | |
| I _{IL} | Input Leakage Current | 0 ≤ V _{IN} ≤ V _{DD} | | — | ±1.0 | — | ±1.0 | μA | | |
| I _{LO} | I/O Leakage Current | CE = V _{IH} , 0V ≤ V _{I/O} ≤ V _{DD} | | — | ±5.0 | — | ±5.0 | μA | | |
| I _{OH} | Output High Current | V _{OH} 2.4V | | −1.0 | — | −1.0 | — | mA | | |
| I _{OL} | Output Low Current | V _{OL} 0.4V | | 2.0 | — | 2.0 | — | mA | | |
| I _{DDs1} | Standby Current | CE2 = 2.2V | | — | 3.0 | — | 3.0 | mA | | |
| I _{DDs2} | | CE ≤ V _{DD} − 0.5V | TC5517CPL/ CFL | Ta = 25°C | — | 0.2 | — | 0.2 | μA | |
| | | | | Ta = 60°C | — | 1.0 | — | 1.0 | | |
| | | TC5517CP/ CF | Ta = 25°C | — | 1.0 | — | 1.0 | | | |
| | | | Ta = 60°C | — | 5.0 | — | 5.0 | | | |
| | | | Ta = 85°C | — | 30 | — | 30 | | | |
| I _{DDO1} | Operating Current | t _{cycle} = Mini cycle, CE = 0V, I _{OUT} = 0mA | | V _{IN} = V _{IH} /V _{IL} | | — | 45 | 30 | mA | |
| I _{DDO2} | | | | V _{IN} = V _{DD} /GND | | — | 40 | 25 | | |
| I _{DDO3} | | t _{cycle} = 1 μs, CE = 0V, I _{OUT} = 0mA | | V _{IN} = V _{IH} /V _{IL} | | — | 10 | — | | 10 |
| I _{DDO4} | | | | V _{IN} = V _{DD} /GND | | — | 5 | — | | 5 |

Note : Typical values are at Ta=25°C, V_{DD}=5V.

TC5517CP-15/CPL-15/CP-20/CPL-20 TC5517CF-15/CFL-15/CF-20/CFL-20

CAPACITANCE

| SYMBOL | PARAMETER | MIN. | TYP. | MAX. | UNIT |
|------------------|--------------------------|------|------|------|------|
| C _{IN} | Input Capacitance | — | 5 | 10 | pF |
| C _{I/O} | Input/Output Capacitance | — | 5 | 10 | pF |

Note : This parameter is periodically sampled and is not 100% tested.

A. C. CHARACTERISTICS

(Ta = -30 ~ 85°C, V_{DD} = 5V ± 10%)

Read Cycle

| SYMBOL | PARAMETER | TC5517CP-15/CPL-15 TC5517CF-15/CFL-15 | | TC5517CP-20/CPL-20 TC5517CF-20/CFL-20 | | UNITS |
|------------------|---------------------------------|--|------|--|------|-------|
| | | MIN. | MAX. | MIN. | MAX. | |
| t _{RC} | Read Cycle Time | 150 | — | 200 | — | ns |
| t _{ACC} | Address Time | — | 150 | — | 200 | |
| t _{OE} | CE to Output Valid | — | 70 | — | 100 | |
| t _{CO} | CE to Output Valid | — | 150 | — | 200 | |
| t _{COE} | CE or OE to Output Active | 10 | — | 10 | — | |
| t _{OD} | Output High-Z from Deselection | — | 50 | — | 60 | |
| t _{OH} | Output Hold from Address Change | 15 | — | 20 | — | |

Write Cycle

| SYMBOL | PARAMETER | TC5517CP-15/CPL-15 TC5517CF-15/CFL-15 | | TC5517CP-20/CPL-20 TC5517CF-20/CFL-20 | | UNITS |
|------------------|------------------------|--|------|--|------|-------|
| | | MIN. | MAX. | MIN. | MAX. | |
| t _{WC} | Write Cycle Time | 100 | — | 200 | — | ns |
| t _{WP} | Write Pulse Width | 120 | — | 150 | — | |
| t _{AW} | Address Set up Time | 0 | — | 0 | — | |
| t _{WR} | Write Recovery Time | 0 | — | 0 | — | |
| t _{ODW} | Output High-Z from R/W | — | 50 | — | 60 | |
| t _{OE} | Output Active from R/W | 10 | — | 10 | — | |
| t _{DS} | Data Set up Time | 60 | — | 80 | — | |
| t _{DH} | Data Hold Time | 0 | — | 0 | — | |

A. C. TEST CONDITIONS

Output Load : 100pF + 1TTL Gate

Timing Measurement Reference Levels

Input Pulse Levels: 0.6V, 2.4V

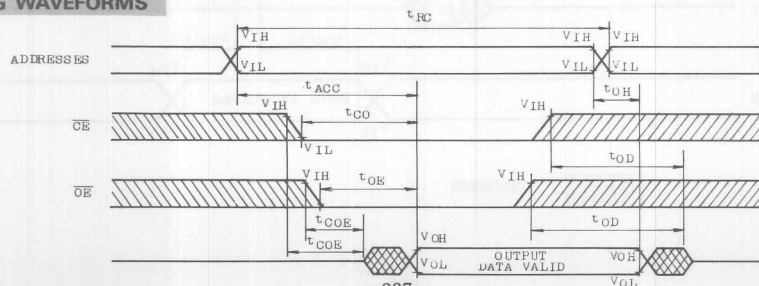
Input : 0.8V and 2.2V

Output : 0.8V and 2.2V

Input Pulse Rise and Fall Times

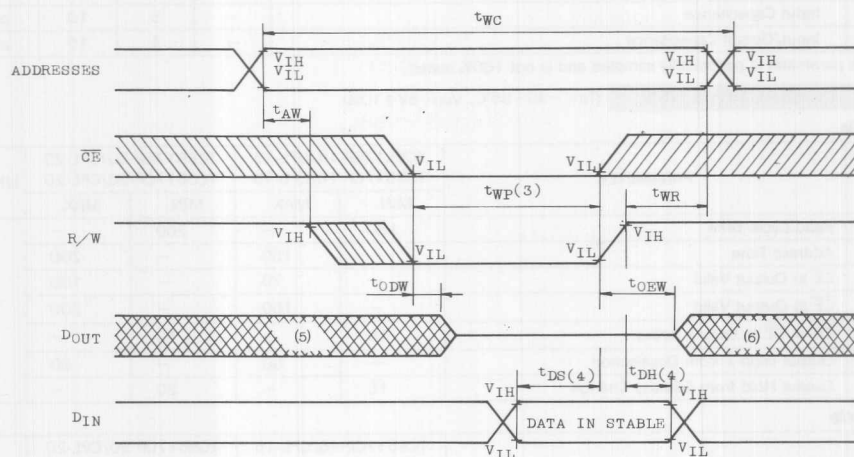
: 10ns

TIMING WAVEFORMS

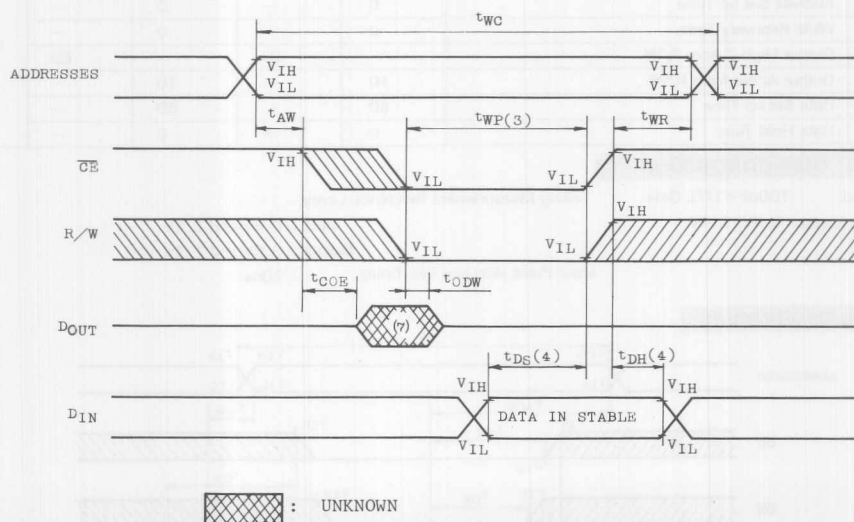


TC5517CP-15/CPL-15/CP-20/CPL-20
TC5517CF-15/CFL-15/CF-20/CFL-20

● Write Cycle 1 (2)



● Write Cycle 2 (2)



Note:

1. R/W is high for a Read Cycle.
2. $\overline{OE} = V_{IH}$ or V_{IL} . If, $\overline{OE} = V_{IH}$ during write cycle, the output buffers remain in a high impedance state.
3. t_{WP} is specified as the logical "AND" of \overline{CE} and R/W.
 t_{WP} is measured from the latter of \overline{CE} or R/W going low to the earlier of \overline{CE} or R/W going high.
4. t_{DH} , t_{DS} are measured from the earlier of \overline{CE} or R/W going high.
5. If the \overline{CE} low transition occurs simultaneously with or latter from the R/W low transition in a Write Cycle 1, the output buffers remain in a high impedance state in this period.
6. If the \overline{CE} high transition occurs prior to or simultaneously with the R/W high transition in a Write Cycle 1, the output buffers remain in a high impedance state in this period.
7. If the R/W is low or the R/W low transition occurs prior to or simultaneously with the \overline{CE} low transition, the output buffers remain in high impedance state in this period.

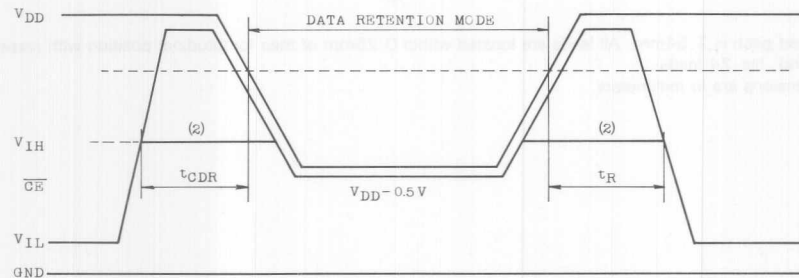
DATA RETENTION CHARACTERISTICS

($T_a = -30 \sim 85^\circ\text{C}$)

| SYMBOL | PARAMETER | | | MIN. | TYP. | MAX. | UNIT |
|------------------|--|---------------|-----------|---------------------|-------|------|------|
| V _{DH} | Data Retention Power Supply Voltage | | | 2.0 | — | 5.5 | V |
| I _{DD2} | Standby Current | TC5517CPL/CFL | Ta = 25°C | — | 0.005 | 0.2 | μA |
| | | | Ta = 60°C | — | — | 1.0 | |
| | | TC5517CP/CF | Ta = 25°C | — | 0.05 | 1.0 | |
| | | | Ta = 60°C | — | — | 5.0 | |
| | | | Ta = 85°C | — | — | 30 | |
| t _{CDR} | From Chip Deselection to Data Retention Mode | | | 0 | — | — | μs |
| t _R | Recovery Time | | | t _{rc} (1) | — | — | |

Note :

1. t_{RC} : Read Cycle Time

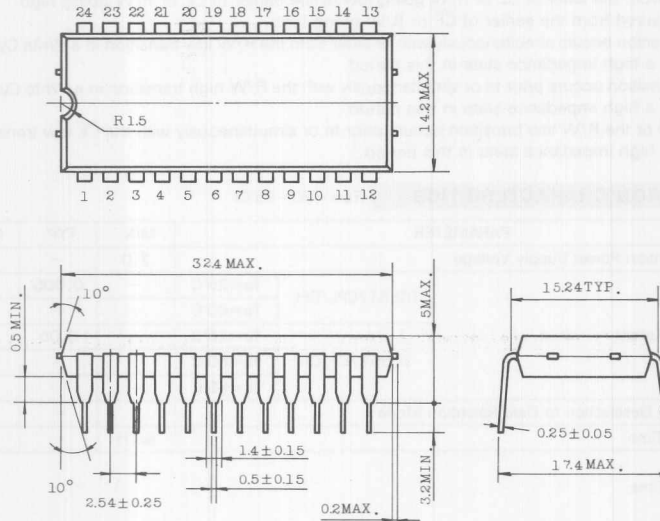


Note :

2. If the V_{IH} level of \overline{CE} is 2.2V, during the period that the V_{DD} voltage is going down from 4.5V to 2.7V I_{DDS1} current flows.

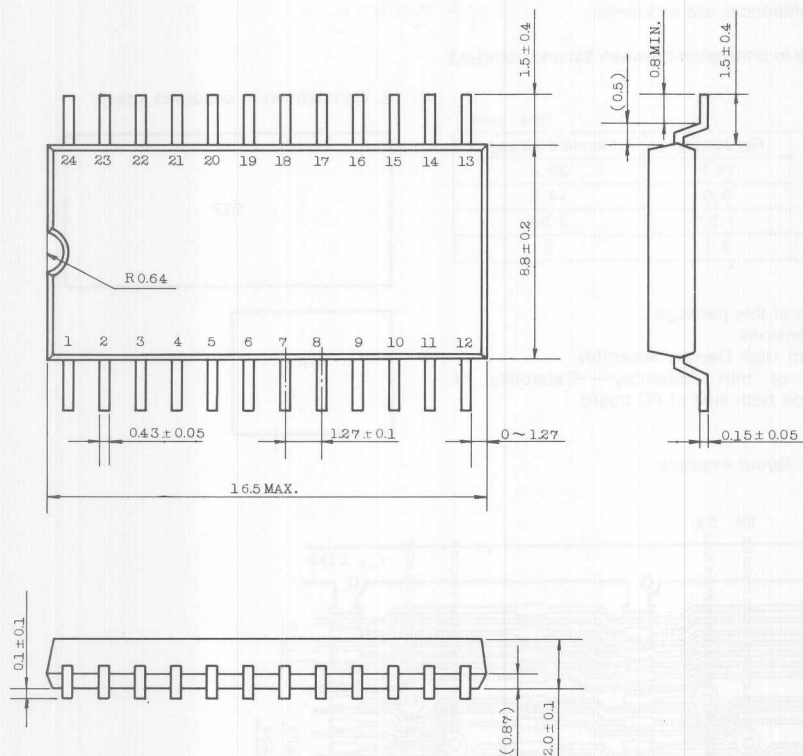
OUTLINE DRAWINGS

- Plastic DIP



Note : Each lead pitch is 2.54mm. All leads are located within 0.25mm of their longitudinal position with respect to No.1 and No.24 leads.
All dimensions are in millimeters.

● Plastic FP



Note : Each lead pitch is 1.27mm.
All leads are located within 0.1mm of their true longitudinal position with respect to No.1 and No.24 leads.

TC5517CP-15/CPL-15/CP-20/CPL-20 TC5517CF-15/CFL-15/CF-20/CFL-20

PACKAGE INFORMATION FOR FLAT PACKAGE

This new flat package is a very small and thin compared with conventional standard dual-in-line package. Differences are as follows.

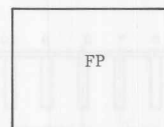
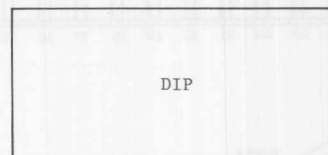
1. Difference in dimension between flat and standard package.

Unit : mm

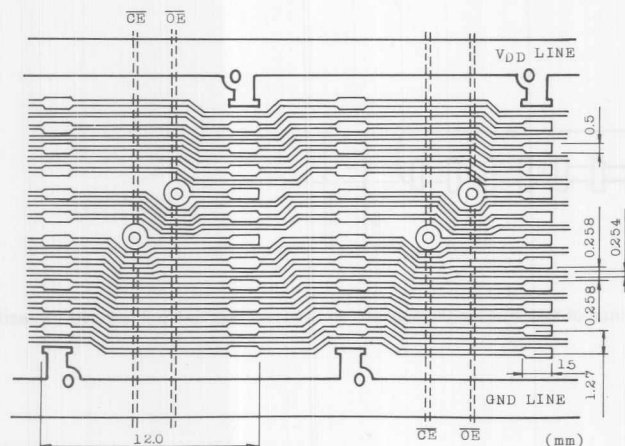
| | Flat package | Standard package |
|------------|--------------|------------------|
| Length | 16.5 | 32.4 |
| Width | 9.0 | 14.2 |
| Lead Pitch | 1.27 | 2.54 |
| Thickness | 2.1 | 5 |

3. Advantage of this package
Small dimensions
Capability of High Density Assembly
Capability of thin Assembly—Capability of Assembly on both side of PC board.

2. Comparison in occupied space.



4. PC pattern layout example.



Note : Toshiba does not assume any responsibility for use of any circuitry described ; no circuit patent licenses are implied, and Toshiba reserves the right, at any time without notice, to change said circuitry.
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TOSHIBA MOS MEMORY PRODUCTS

2,048 WORD × 8 BIT CMOS STATIC RAM

TC5518CP-15/CPL-15/CP-20/CPL-20
TC5518CF-15/CFL-15/CF-20/CFL-20

DESCRIPTION

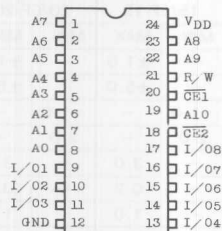
The TC5518CP/CF is a 16384-bit high speed and low power fully static random access memory organized as 2048 words by a 8 bits using CMOS technology, and operates from a single 5 volt supply. The TC5518CP/CF has two chip enable inputs, \overline{CE}_1 and \overline{CE}_2 , which are used for device selection and can be used in order to achieve minimum standby current mode easily for battery back up. Also the high speed and low power characteristics which maximum access time is 150ns, 200ns and maximum operating current is 5mA/MHz are achieved. Thus

the TC5518CP/CF is most suitable for use in low power applications where battery operation or battery back up for nonvolatility are required. Furthermore the TC5518CPL/CFL guaranteed a standby current equal to or less than $1\mu A$ at $60^\circ C$ ambient temperature available. And the TC5518CP is pin compatible with 2716 type EPROM. This means that the TC5518CP and EPROM can be interchanged in the same socket and the flexibility in the definition of the quantity of RAM versus EPROM allows the wide application in microcomputer system.

FEATURES

- Low Power Dissipation
27.5mW/MHz(Max.) Operating
- Standby Current
 - 0.2 μA (Max.) at $T_a=25^\circ C$ TC5518CPL-15/CPL-20
 - 1.0 μA (Max.) at $T_a=60^\circ C$ CFL-15/CFL-20
 - 1.0 μA (Max.) at $T_a=25^\circ C$ TC5518CP-15/CP-20
 - 5.0 μA (Max.) at $T_a=60^\circ C$ CF-15/CF-20
- Single 5V Power Supply : $5V \pm 10\%$
- Data Retention Supply Voltage : 2.0~5.5V
- Fully Static Operation
- Fast Access Time
 $t_{acc}=150ns$ (Max.) : TC5518CP-15/CPL-15
CF-15/CFL-15
- $t_{acc}=200ns$ (Max.) : TC5518CP-20/CPL-20
CF-20/CFL-20
- Two Chip Enables ($\overline{CE}_1, \overline{CE}_2$) for Simple Memory Expansion and Battery Back Up
- On-Chip Address Transition Detector
- All Inputs and Outputs Directly TTL Compatible
- Three State Outputs
- Package ; Plastic DIP : TC5518CP-15/CPL-15 (600 mil) CP-20/CPL-20
Plastic FP : TC5518CF-15/CFL-15 CF-20/CFL-20

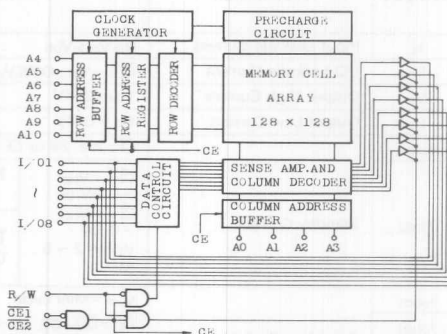
PIN CONNECTION (TOP VIEW)



PIN NAMES

| | |
|------------------------------------|--------------------------|
| $A_0 \sim A_{10}$ | Address Inputs |
| R/W | Read/Write Control Input |
| $\overline{CE}_1, \overline{CE}_2$ | Chip Enable Inputs |
| I/O ₁ I/O ₈ | Data Input/Output |
| V _{DD} | Power (+5V) |
| GND | Ground |

BLOCK DIAGRAM



TC5518CP-15/CPL-15/CP-20/CPL-20

TC5518CF-15/CFL-15/CF-20/CFL-20

OPERATION MODE

| MODE | \overline{CE}_2 | \overline{CE}_1 | R/W | $A_0 \sim A_{10}$ | I/O ₁ ~I/O ₈ | POWER |
|--------------|-------------------|-------------------|-----|-------------------|------------------------------------|------------------|
| Read | L | L | H | Stable | Data Out | I _{DD0} |
| Write | L | L | L | Stable | Data In | I _{DD0} |
| ** Standby 1 | * | H | * | * | High Impedance | I _{DD5} |
| ** Standby 2 | H | * | * | * | High Impedance | I _{DD5} |

Note : * : H or L ** : Data Retention Mode

ABSOLUTE MAXIMUM RATINGS

| SYMBOL | ITEM | RATING |
|---------------------|----------------------------|-----------------------------|
| V _{DD} | Power Supply Voltage | -0.3~7.0V |
| V _{IN} | Input Voltage | -0.3V~V _{DD} +0.3V |
| V _{I/O} | Input/Output Voltage | -0.3V~V _{DD} +0.3V |
| P _D | Power Dissipation(Ta=85°C) | 0.8W(0.45W)* |
| T _{STG} | Storage Temperature | -55°C~150°C |
| T _{OPR} | Operating Temperature | -30°C~85°C |
| T _{SOLDER} | Soldering Temperature·Time | 260°C·10sec. |

*Plastic FP=0.45W

RECOMMENDED D. C. OPERATING CONDITIONS (Ta=-30~85°C)

| SYMBOL | PARAMETER | MIN. | TYP. | MAX. | UNIT |
|-----------------|------------------------|------|------|----------------------|------|
| V _{DD} | Power Supply Voltage | 4.5 | 5.0 | 5.5 | V |
| V _{IH} | Input High Voltage | 2.2 | — | V _{DD} +0.3 | V |
| V _{IL} | Input Low Voltage | -0.3 | — | 0.8 | V |
| V _{DH} | Data Retention Voltage | 2.0 | — | 5.5 | V |

D. C. CHARACTERISTICS

(Ta=30~85°C, V_{DD}=5V±10%)

| SYMBOL | PARAMETER | CONDITIONS | | | TC5518CP-15/CF-15 | | TC5518CP-20/CF-20 | | UNIT |
|-------------------|-----------------------|--|-------------------|--|-------------------|------|-------------------|------|------|
| | | | | | MIN. | MAX. | MIN. | MAX. | |
| I _{IL} | Input Leakage Current | 0 ≤ V _{IN} ≤ V _{DD} | | | — | ±1.0 | — | ±1.0 | μA |
| I _{LO} | I/O Leakage Current | $\overline{CE}_2 = V_{IH}$, 0V ≤ V _{I/O} ≤ V _{DD} | | | — | ±5.0 | — | ±5.0 | μA |
| I _{OH} | Output High Current | V _{OH} = 2.4V | | | -1.0 | — | -1.0 | — | mA |
| I _{OL} | Output Low Current | V _{OL} = 0.4V | | | 2.0 | — | 2.0 | — | mA |
| I _{DD51} | Standby Current | $\overline{CE}_2 = 2.2V$ or $\overline{CE}_1 = 2.2V$ | | | — | 3.0 | — | 3.0 | mA |
| I _{DD52} | | $\overline{CE}_2 = V_{DD} - 0.5V$ or $\overline{CE}_1 = V_{DD} - 0.5V$ | TC5518CPL/ CFL | Ta = 25°C | — | 0.2 | — | 0.2 | μA |
| | | | | Ta = 60°C | — | 1.0 | — | 1.0 | |
| | | TC5518CP/ CF | Ta = 25°C | — | 1.0 | — | 1.0 | | |
| | | | Ta = 60°C | — | 5.0 | — | 5.0 | | |
| | | | Ta = 85°C | — | 30 | — | 30 | | |
| I _{DD01} | Operating Current | t _{cycle} = Mini cycle, | | V _{IN} = V _{IH} /V _{IL} | | — | | 30 | mA |
| I _{DD02} | | $\overline{CE}_1 = \overline{CE}_2 = 0V$, I _{OUT} = 0mA | | V _{IN} = V _{DD} /GND | | — | | 25 | |
| I _{DD03} | | t _{cycle} = 1μs, $\overline{CE}_1 =$ | | V _{IN} = V _{IH} /V _{IL} | | — | | 10 | |
| I _{DD04} | | $\overline{CE}_2 = 0V$, I _{OUT} = 0mA | | V _{IN} = V _{DD} /GND | | — | | 5 | |

Note : Typical values are at Ta=25°C, V_{DD}=5V.

TC5518CP-15/CPL-15/CP-20/CPL-20 TC5518CF-15/CFL-15/CF-20/CFL-20

CAPACITANCE

| SYMBOL | PARAMETER | MIN. | TYP. | MAX. | UNIT |
|------------------|--------------------------|------|------|------|------|
| C _{IN} | Input Capacitance | — | 5 | 10 | pF |
| C _{OUT} | Input/Output Capacitance | — | 5 | 10 | pF |

Note : This parameter is periodically sampled and is not 100% tested.

A. C. CHARACTERISTICS

(Ta = -30~85°C, V_{DD}5V±10%)

Read Cycle

| SYMBOL | PARAMETER | TC5518CP-15/CPL-15 TC5518CF-15/CFL-15 | | TC5518CP-20/CPL-20 TC5518CF-20/CFL-20 | | UNIT |
|------------------|---|--|------|--|------|------|
| | | MIN. | MAX. | MIN. | MAX. | |
| t _{RC} | Read Cycle Time | 150 | — | 200 | — | ns |
| t _{ACC} | Address Time | — | 150 | — | 200 | |
| t _{CO1} | CE ₁ to Output Valid | — | 150 | — | 200 | |
| t _{CO2} | CE ₂ to Output Valid | — | 150 | — | 200 | |
| t _{COE} | CE ₁ or CE ₂ to Output Active | 10 | — | 10 | — | |
| t _{OD} | Output High-Z Deselection | — | 50 | — | 60 | |
| t _{OH} | Output Hold from Address Change | 15 | — | 20 | — | |

| SYMBOL | PARAMETER | TC5518CP-15/CPL-15 TC5518CF-15/CFL-15 | | TC5518CP-20/CPL-20 TC5518CF-20/CFL-20 | | UNIT |
|------------------|------------------------|--|------|--|------|------|
| | | MIN. | MAX. | MIN. | MAX. | |
| t _{WC} | Write Cycle Time | 150 | — | 200 | — | ns |
| t _{WP} | Write Pulse Width | 120 | — | 150 | — | |
| t _{AW} | Address Set up Time | 0 | — | 0 | — | |
| t _{WR} | Write Recovery Time | 0 | — | 0 | — | |
| t _{ODW} | Output High-Z from R/W | — | 50 | — | 60 | |
| t _{OEW} | Output Active from R/W | 10 | — | 10 | — | |
| t _{DS} | Data Set up Time | 60 | — | 80 | — | |
| t _{DH} | Data Hold Time | 0 | — | 0 | — | |

A. C. TEST CONDITIONS

Output Load : 100pF + 1TTL Gate

Input Pulse Levels : 0.6V, 2.4V

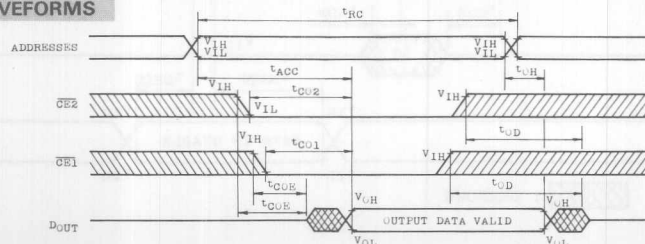
Timing Measurement Reference Levels

Input : 0.8V and 2.2V

Output : 0.8V and 2.2V

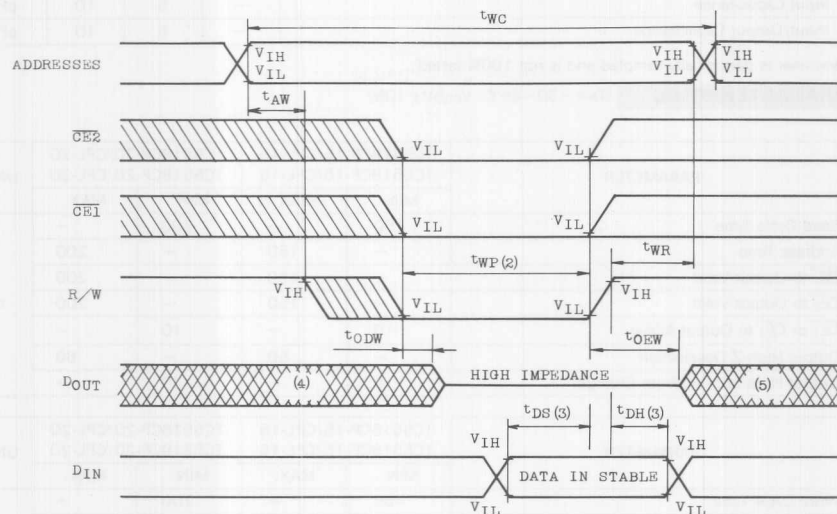
Input Pulse Rise and Fall Times : 10ns

TIMING WAVEFORMS

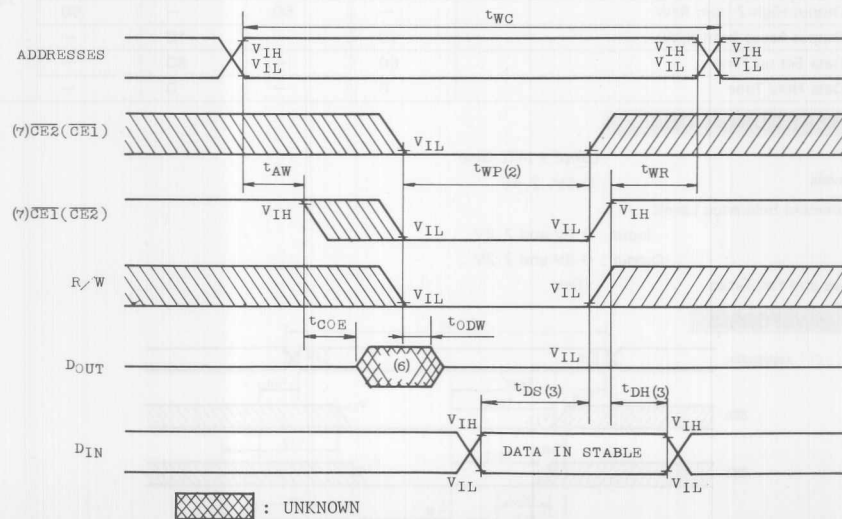


TC5518CP-15/CPL-15/CP-20/CPL-20
TC5518CF-15/CFL-15/CF-20/CFL-20

• Write Cycle 1 (2)



• Write Cycle 2 (2)



Note :

1. R/W is high for a read Cycle.
2. t_{WP} is specified as logical "AND" of $\overline{CE_1}$, $\overline{CE_2}$ and R/W.
 t_{WP} is measured from the latter of $\overline{CE_1}$, $\overline{CE_2}$ or R/W going low to the earlier of $\overline{CE_1}$, $\overline{CE_2}$ or R/W going high.
3. t_{DH} , t_{DS} are measured from the earlier of $\overline{CE_1}$, $\overline{CE_2}$ or R/W going high.
4. If the $\overline{CE_1}$ or $\overline{CE_2}$ low transition occurs simultaneously or latter from the R/W low transition in a Write Cycle 1, the output buffers remain in a high impedance state in this period.
5. If the $\overline{CE_1}$ or $\overline{CE_2}$ high transition occurs prior to or simultaneously with the R/W high transition in a Write Cycle 1, the output buffers remain in a high impedance state in this period.
6. If the R/W is low or the R/W low transition occurs prior to or simultaneously with the $\overline{CE_1}$ or $\overline{CE_2}$ low transition, the output buffers remain in a high impedance state in this period.
7. A write occurs during the overlap of a low $\overline{CE_1}$, low $\overline{CE_2}$ and low R/W.
In write cycle 2, write is controlled by either $\overline{CE_1}$ or $\overline{CE_2}$.

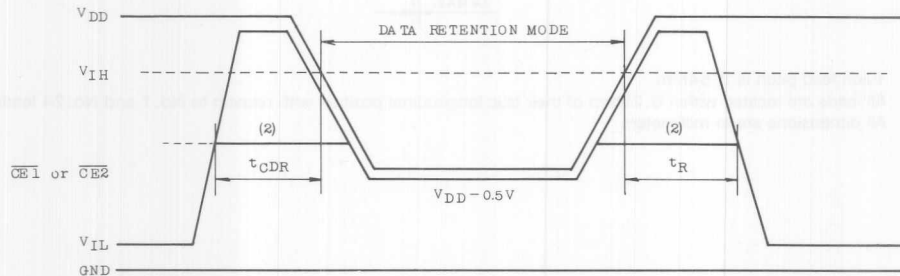
DATA RETENTION CHARACTERISTICS

($T_a = -30 \sim 85^\circ\text{C}$)

| SYMBOL | PARAMETER | | | MIN. | TYP. | MAX. | UNIT |
|------------------|--|---------------|----------------------|---------------------|-------|------|------|
| V _{DH} | Data Retention Power Supply Voltage | | | 2.0 | — | 5.5 | V |
| I _{DD2} | Standby Current | TC5518CPL/CFL | T _a =25°C | — | 0.005 | 0.2 | μA |
| | | | T _a =60°C | — | — | 1.0 | |
| | | TC5518CP/CF | T _a =25°C | — | 0.05 | 1.0 | |
| | | | T _a =60°C | — | — | 5.0 | |
| | | | T _a =85°C | — | — | 30 | |
| t _{CDR} | From Chip Deselection to Data Retention Mode | | | 0 | — | — | μS |
| t _R | Recovery Time | | | t _{RC} (1) | — | — | μS |

Note :

1. t_{RC} : Read Cycle Time

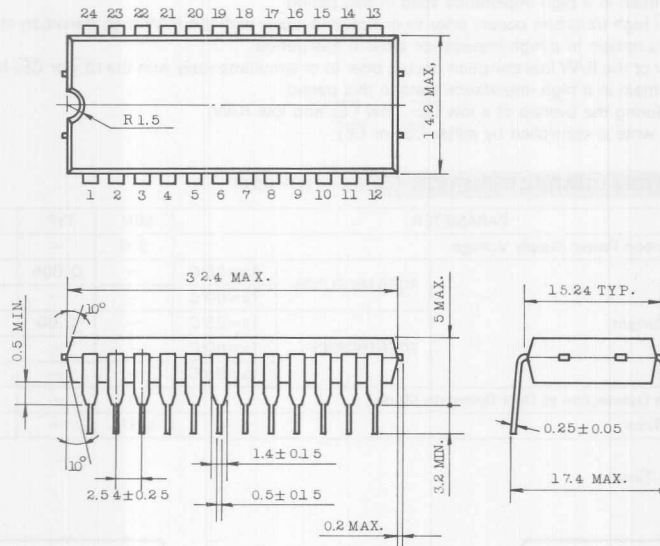


2. If the V_{IH} level of $\overline{CE_2}$ ($\overline{CE_1}$) is 2.2V, during the period that the V_{DD} voltage is going down from 4.5V to 2.7V, I_{DPS1} current flows.

TC5518CP-15/CPL-15/CP-20/CPL-20
TC5518CF-15/CFL-15/CF-20/CFL-20

OUTLINE DRAWINGS

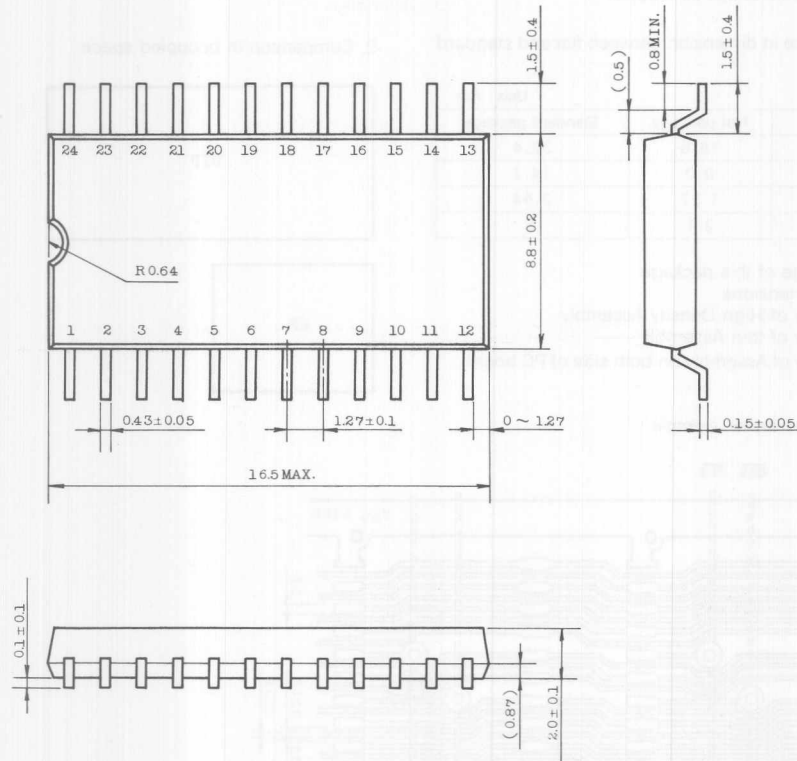
- Plastic DIP



Note : Each lead pitch is 2.54mm.
 All leads are located within 0.25mm of their true longitudinal position with respect to No. 1 and No. 24 leads.
 All dimensions are in millimeters.

TC5518CP-15/CPL-15/CP-20/CPL-20
TC5518CF-15/CFL-15/CF-20/CFL-20

● Plastic FP



Note : Each lead pitch is 1.27mm.
All leads are located within 0.1mm of their true longitudinal position with respect to No.1 and No.24 leads.

TC5518CP-15/CPL-15/CP-20/CPL-20 TC5518CF-15/CFL-15/CF-20/CFL-20

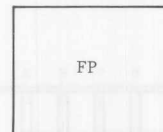
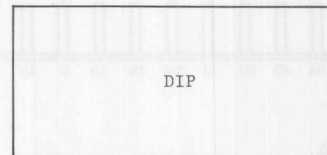
PACKAGE INFORMATION FOR FLAT PACKAGE

This new flat package is a very small and this compared with conventional standard dual-in-line package. Differences as follows.

1. Difference in dimension between flat and standard package.

| | Unit : mm | |
|------------|--------------|------------------|
| | Flat package | Standard package |
| Length | 16.5 | 32.4 |
| Width | 9.0 | 14.2 |
| Lead Pitch | 1.27 | 2.54 |
| Thickness | 2.1 | 5 |

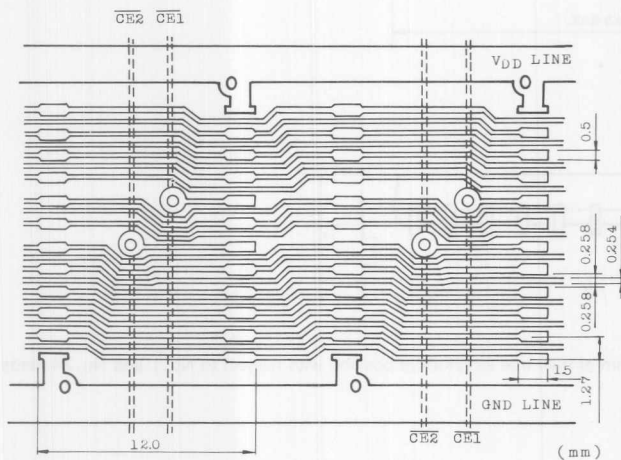
2. Comparison in occupied space



3. Advantage of this package

Small dimensions
Capability of High Density Assembly
Capability of thin Assembly —
Capability of Assembly on both side of PC board.

4. PC pattern layout example



Note : Toshiba does not assume any responsibility for use of any circuitry described ; no circuit patent licenses are implied, and Toshiba reserves the right, at any time without notice, to change said circuitry.
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TOSHIBA MOS MEMORY PRODUCTS

8,192 WORD × 8 BIT CMOS STATIC RAM
SILICON GATE CMOS

TC5564PL-15
TC5564PL-20

DESCRIPTION

TC5564PL is 65536 bits static random access memory organized as 8192 words by 8 bits using CMOS technology, and operates with a single 5V power supply.

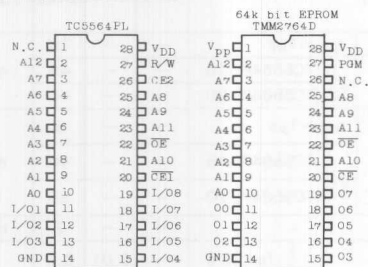
Advanced circuit techniques provides low power feature with a maximum operating current of 5mA/ MHz. Operation current depends on cycle time.

TC5564PL has three control inputs. Two chip enables(CE₁, CE₂) allow for device selection and data retention control. Output enable(OE) input provides fast memory access. When device is placed in standby mode with chip off state, standby current

FEATURES

- Standby Current
0.2μA(MAX.) at Ta=25°C
1.0μA(MAX.) at Ta=60°C
- Low Power Dissipation
27.5mW/MHz(MAX.) Operating
- 5V Single Power Supply
- 8,192 Word × 8Bit
- Fully Static Operation
- Data Retention Voltage : 2.0~5.5V

PIN CONNECTION (TOP VIEW)



PIN NAMES

| | |
|------------------------------------|--------------------------|
| A ₀ ~A ₁₂ | Address Inputs |
| R/W | Read/Write Control Input |
| OE | Output Enable Input |
| CE ₁ , CE ₂ | Chip Enable Inputs |
| I/O ₁ ~I/O ₈ | Data Input/Output |
| V _{DD} | Power (+5V) |
| GND | Ground |
| N. C. | No Connection |

is typically 0.01μA. So the TC5564PL is suitable for use in various microprocessor application systems where low power and battery back up are required. Ultra low standby power allow not only battery but capacitance backup.

Pin assignment of TC5564PL is pin compatible with the 64K bits EPROM(TMM2764D). RAM and EPROM are then interchangeable in the same socket, resulting in flexibility in the definition of the quantity of RAM versus EPROM in microprocessor application systems.

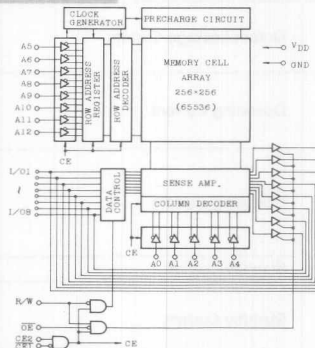
TC5564PL is offered in a standard dual-in-line 28pin plastic package, 0.6 inch width.

Access Time

| | TC5564PL-15 | TC5564PL-20 |
|-----------------------------------|-------------|-------------|
| Address Access Time (MAX) | 150ns | 200ns |
| CE ₁ Access Time (MAX) | 150ns | 200ns |
| CE ₂ Access Time (MAX) | 150ns | 200ns |
| Output Enable Time (MAX) | 70ns | 100ns |

- Directly TTL Compatible : All Inputs and Outputs
- Standard 28 Pin DIP
- Pin compatible with 2764 type EPROM

BLOCK DIAGRAM



OPERATING MODE

| Operation Mode | CE ₁ | CE ₂ | OE | R/W | I/O ₁ ~I/O ₈ | Power |
|-----------------|-----------------|-----------------|----|-----|------------------------------------|------------------|
| Read | L | H | L | H | DOUT | I _{DDO} |
| Write | L | H | * | L | DIN | I _{DDO} |
| Output Deselect | * | * | H | * | High-Z | I _{DDO} |
| Standby | H | * | * | * | " | I _{DDO} |
| | * | L | * | * | " | I _{DDO} |

TC5564PL-15

TC5564PL-20

MAXIMUM RATINGS

| SYMBOL | ITEM | RATING | UNIT |
|--------------|--------------------------|-----------------------|--------|
| V_{DD} | Power Supply Voltage | -0.3 ~ 7.0* | V |
| V_{IN} | Input Voltage | -0.3**~7.0 | V |
| $V_{I/O}$ | Input and Output Voltage | -0.5 ~ $V_{DD} + 0.5$ | V |
| P_D | Power Dissipation | 1.0 | W |
| T_{SOLDER} | Soldering Temperature | 260~10 | °C·Sec |
| T_{STG} | Storage Temperature | -55 ~ 150 | °C |
| T_{OPR} | Operating Temperature | -30 ~ 85 | °C |

* 8.5V at Pulse width 100ns

** -3.0V at Pulse width 50ns

D.C. RECOMMENDED OPERATING CONDITIONS

| SYMBOL | PARAMETER | MIN. | TYP | MAX. | UNIT |
|----------|-------------------------------|-------|-----|----------------|------|
| V_{DD} | Power Supply Voltage | 4.5 | 5.0 | 5.5 | V |
| V_{IH} | Input High Voltage | 2.2 | — | $V_{DD} + 0.3$ | V |
| V_{IL} | Input Low Voltage | -0.3* | — | 0.8 | V |
| V_{DH} | Data Retention Supply Voltage | 2.0 | — | 5.5 | V |

* -3.0V at Pulse width 50ns

D.C. and OPERATING CHARACTERISTICS (Ta = -30 ~ 85°C, $V_{DD} = 5V \pm 10\%$ Unless otherwise noted)

| SYMBOL | PARAMETER | CONDITIONS | MIN. | TYP. | MAX. | UNIT |
|------------|------------------------|---|----------------------|-------------|-----------|---------|
| I_{IL} | Input Leakage Current | $V_{IN} = 0 \sim V_{DD}$ | — | — | ± 1.0 | μA |
| I_{OH} | Output High Current | $V_{OH} = 2.4V$ | -1.0 | — | — | mA |
| I_{OL} | Output Low Current | $V_{OL} = 0.4V$ | 4.0 | — | — | mA |
| I_{LO} | Output Leakage Current | $\overline{CE}_1 = V_{IH}$ or $CE_2 = V_{IL}$ or $R/W = V_{IL}$, or $\overline{OE} = V_{IH}$ $V_{OUT} = 0 \sim V_{DD}$ | — | — | ± 1.0 | μA |
| I_{DDO1} | Operating Current | $\overline{CE}_1 = V_{IL}$ and $CE_2 = V_{IH}$ Other Input = V_{IH}/V_{IL} $I_{OUT} = 0mA$ | $t_{cycle} = 1\mu s$ | | 10 | mA |
| | | | MIN CYCLE | TC5564PL-15 | 45 | |
| | | | | TC5564PL-20 | 40 | |
| I_{DDO2} | Operating Current | $\overline{CE}_1 = 0.2V$ and $CE_2 = V_{DD} - 0.2V$ Other Input = $V_{DD} - 0.2V/0.2V$ $I_{OUT} = 0mA$ | $t_{cycle} = 1\mu s$ | | 5 | mA |
| | | | MIN CYCLE | TC5564PL-15 | 40 | |
| | | | | TC5564PL-20 | 35 | |
| I_{DDs1} | Standby Current | $\overline{CE}_1 = V_{IH}$ or $CE_2 = V_{IL}$ | — | — | 2 | mA |
| I_{DDs2} | Standby Current | $\overline{CE}_1 = V_{DD} - 0.2V$ or $CE_2 = 0.2V$ $V_{DD} = 2.0 \sim 5.5V$ | $T_a = 25^\circ C$ | | 0.01 | μA |
| | | | $T_a = 60^\circ C$ | | 1.0 | |

Note : In standby mode with $\overline{CE}_1 \geq V_{DD} - 0.2V$, these specification limits are guaranteed under the condition of $CE_2 \geq V_{DD} - 0.2V$ or $CE_2 \leq 0.2V$.

CAPACITANCE (Ta = 25°C, f = 1MHz)

| SYMBOL | PARAMETER | CONDITIONS | MAX. | UNIT |
|-----------|--------------------|-----------------|------|------|
| C_{IN} | Input Capacitance | $V_{IN} = GND$ | 10 | pF |
| C_{OUT} | Output Capacitance | $V_{OUT} = GND$ | 10 | pF |

Note : This parameter is periodically sampled and is not 100% tested.

A. C. CHARACTERISTICS

($T_a = -30 \sim 85^\circ\text{C}$, $V_{DD} = 5V \pm 10\%$)

Read Cycle

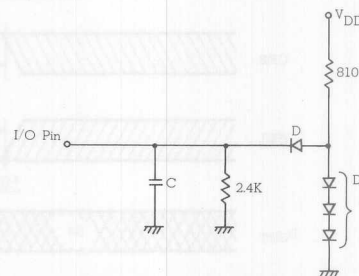
| SYMBOL | PARAMETER | TC5564PL-15 | | TC5564PL-20 | | UNIT |
|-----------|---|-------------|------|-------------|------|------|
| | | MIN. | MAX. | MIN. | MAX. | |
| t_{RC} | Read Cycle Time | 150 | — | 200 | — | ns |
| t_{ACC} | Address Access Time | — | 150 | — | 200 | |
| t_{CO1} | \overline{CE}_1 Access Time | — | 150 | — | 200 | |
| t_{CO2} | \overline{CE}_2 Access Time | — | 150 | — | 200 | |
| t_{OE} | Output Enable to Output in Valid | — | 70 | — | 100 | |
| t_{COE} | Chip Enable (\overline{CE}_1), \overline{CE}_2 to Output in Low-Z | 10 | — | 10 | — | |
| t_{OEE} | Output Enable to Output Low-Z | 5 | — | 5 | — | |
| t_{OD} | Chip Enable (\overline{CE}_1 , \overline{CE}_2) to Output in High-Z | — | 70 | — | 100 | |
| t_{ODO} | Output Enable to Output High-Z | — | 60 | — | 80 | |
| t_{OH} | Output Data Hold Time | 20 | — | 20 | — | |

Write Cycle

| SYMBOL | PARAMETER | TC5564PL-15 | | TC5564PL-20 | | UNIT |
|-----------|--------------------------------|-------------|------|-------------|------|------|
| | | MIN. | MAX. | MIN. | MAX. | |
| t_{WC} | Write Cycle Time | 150 | — | 200 | — | ns |
| t_{WP} | Write Pulse Width | 100 | — | 150 | — | |
| t_{CW} | Chip Selection to End of Write | 120 | — | 180 | — | |
| t_{AW} | Address Set up Time | 0 | — | 0 | — | |
| t_{WR} | Write Recovery Time | 0 | — | 0 | — | |
| t_{ODW} | R/W to Output High-Z | — | 70 | — | 100 | |
| t_{OEW} | R/W to Output Low-Z | 10 | — | 10 | — | |
| t_{DS} | Data Set Up Time | 70 | — | 80 | — | |
| t_{DH} | Data Hold Time | 0 | — | 0 | — | |

A. C. TEST CONDITIONS

Input Pulse Levels : 2.4V/0.6V
 Timing Measurement Reference levels : Input ; 2.2V/0.8V
 : Output; 2.2V/0.8V
 Input Pulse Rise and Fall Times : 5ns
 Output Load : See Fig. 1

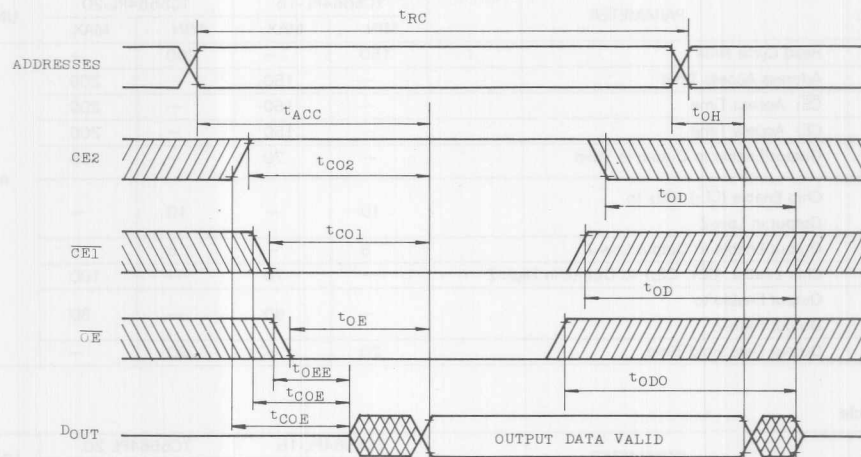


C : 100pF (Including jig)
 D : 1S1588 or Equivalent
 Fig. 1 Output Load

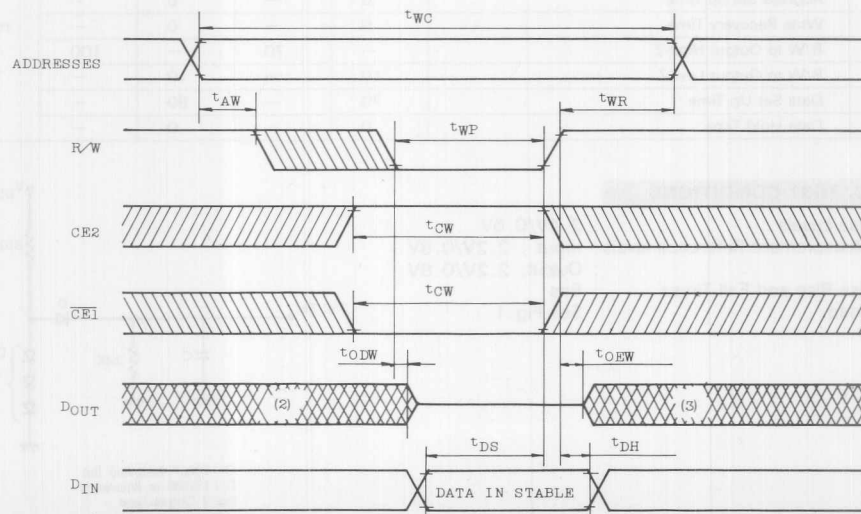
TC5564PL-15 TC5564PL-20

TIMING WAVEFORMS

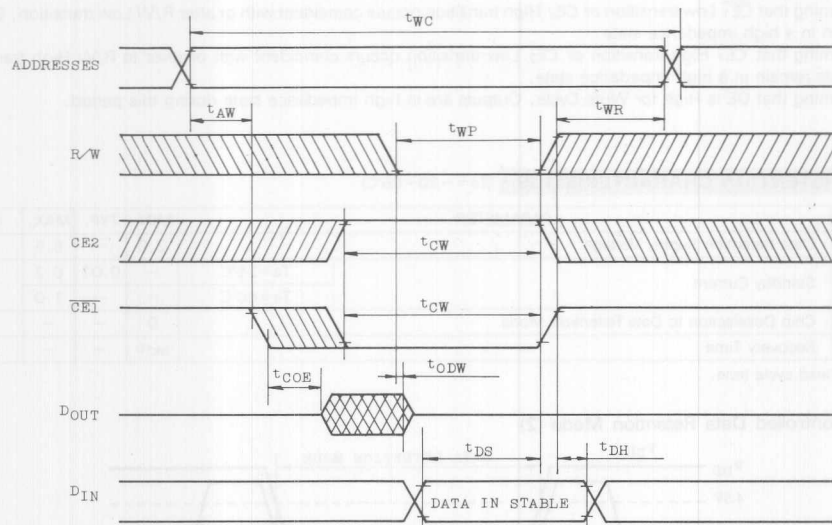
• READ CYCLE (1)



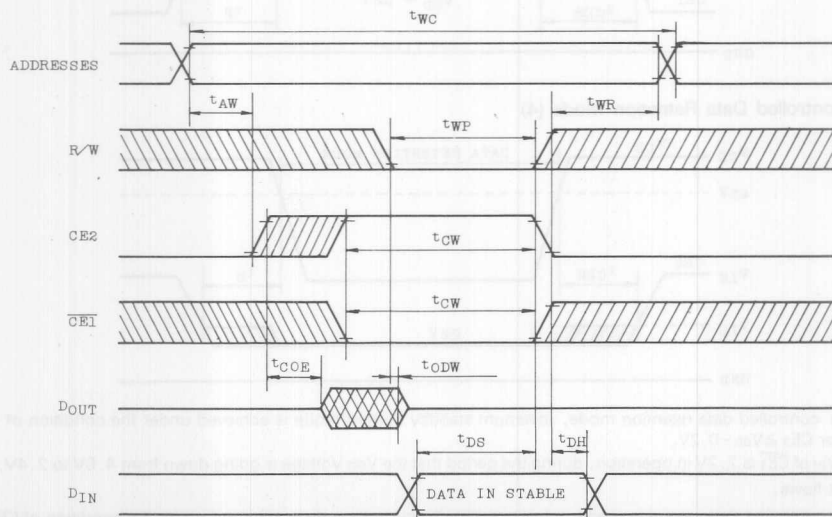
• WRITE CYCLE 1 (R/W Controlled Write)



● WRITE CYCLE 2 (4) (\overline{CE}_1 Controlled Write)



● WRITE CYCLE 3 (4) (CE_2 Controlled Write)



TC5564PL-15

TC5564PL-20

Note :

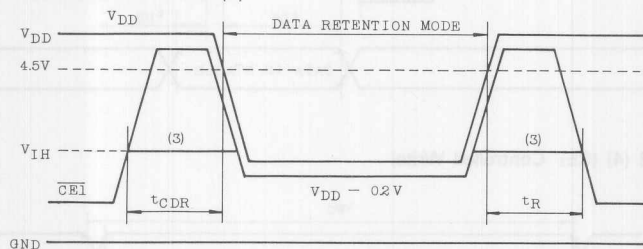
1. R/W is High for Read Cycle.
2. Assuming that \overline{CE}_1 Low transition or CE_2 High transition occurs coincident with or after R/W Low transition, Outputs remain in a high impedance state.
3. Assuming that \overline{CE}_1 High transition or CE_2 Low transition occurs coincident with or prior to R/W High transition, outputs remain in a high impedance state.
4. Assuming that OE is High for Write Cycle, Outputs are in high impedance state during this period.

DATA RETENTION CHARACTERISTICS (Ta = -30 ~ 85°C)

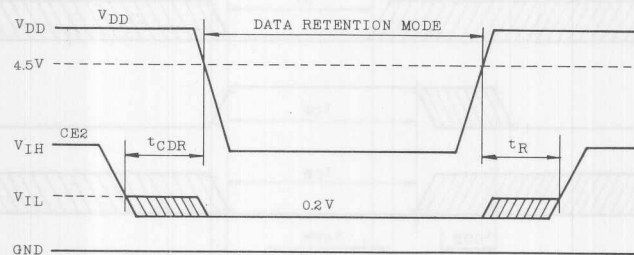
| SYMBOL | PARAMETER | MIN. | TYP. | MAX. | UNIT |
|------------|---|-------------|------|------|---------|
| V_{DH} | Data Retention Supply Voltage | 2.0 | — | 5.5 | V |
| I_{DDS2} | Standby Current | Ta = 25°C | — | 0.01 | 0.2 |
| | | Ta = 60°C | — | — | 1.0 |
| t_{CDR} | Chip Deselection to Data Retention Mode | 0 | — | — | μ s |
| t_R | Recovery Time | $t_{rc(1)}$ | — | — | μ s |

Note (1) : Read cycle time.

• \overline{CE}_1 Controlled Data Retention Mode (2)



• CE_2 Controlled Data Retention Mode (4)



Note :

2. In \overline{CE}_1 controlled data retention mode, minimum standby current mode is achieved under the condition of $CE_2 \leq 0.2V$ or $CE_2 \geq V_{DD} - 0.2V$.
3. If the V_{IH} of \overline{CE}_1 is 2.2V in operation, during the period that the V_{DD} Voltage is going down from 4.5V to 2.4V, I_{DDs1} current flows.
4. In CE_2 controlled data retention mode, minimum standby current mode is achieved under the condition of $CE_2 \leq 0.2V$.

DEVICE INFORMATION

The TC5564PL is an asynchronous RAM using address activated circuit technology, thus the internal operation is synchronous. Then once row address change occur, the precharge operation is executed by internal pulse generated from row address transient. Therefore the peak current flows

only row address change, as is shown in the following figure.

This peak current may induce the noise on $V_{DD}/$ GND line. Thus the use of about $0.1\mu\text{F}$ decoupling capacitor every device is recommended to eliminate such noise.

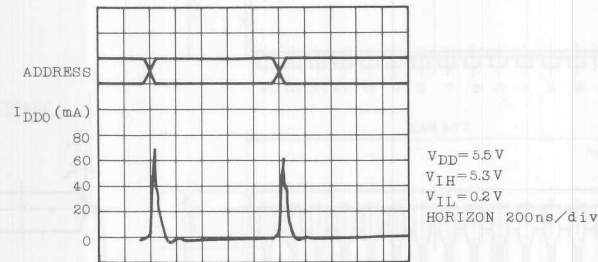
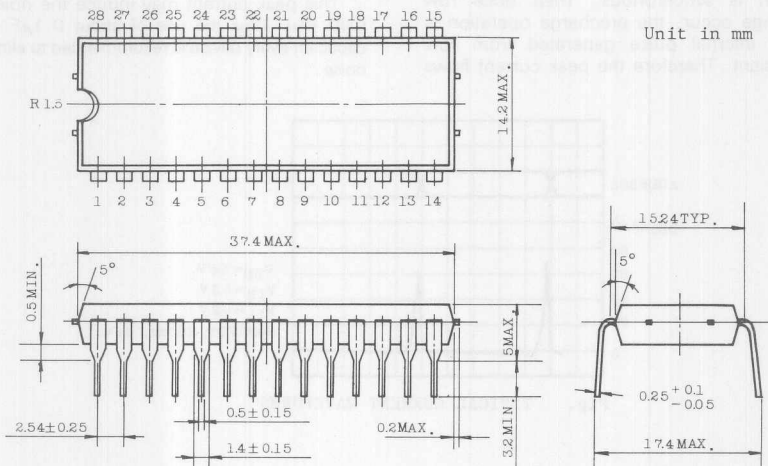


Fig. TYPICAL CURRENT WAVEFORMS

TC5564PL-15 TC5564PL-20

OUTLINE DRAWINGS



NOTES : Each lead pitch is 2.54mm.

All leads are located within 0.25mm of their true longitudinal position with respect to No.1 and No.28 leads.

Note : Toshiba does not assume any responsibility for use of any circuitry described ; no circuit patent licenses are implied, and Toshiba reserves the right, at any time without notice, to change said circuitry.

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TOSHIBA MOS MEMORY PRODUCTS

8,192 WORD \times 8 BIT CMOS STATIC RAM
SILICON GATE CMOS

TC5565PL-12, TC5565PL-15
TC5565FL-12, TC5565FL-15

DESCRIPTION

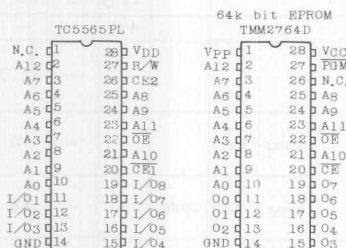
The TC5565P is 65,536 bit static random access memory organized as 8,192 words by 8 bits using CMOS technology, and operates from a single 5V supply. Advanced circuit techniques provide both high speed and low power features with a maximum operating current of 5mA/MHz and maximum access time of 120ns/150ns.

When $\overline{CE_2}$ is a logical low or $\overline{CE_1}$ is a logical high, the device is placed in low power standby mode in which standby current is $2\mu A$ typically. The TC5565P has three control inputs. Two chip enables ($\overline{CE_1}$, $\overline{CE_2}$) allow for device selection and data retention control, and an output enable input (\overline{OE}) pro-

FEATURES

- Low Power Dissipation
27.5mW/MHz(Max.) Operating
- Standby Current : 100mA(MAX.)
- 5V Single Power Supply
- Power Down Features : CE₂, CE₁
- Fully Static Operation
- Data Retention Supply Voltage : 2.0~5.5V

PIN CONNECTION (TOP VIEW)



PIN NAMES

| | |
|------------------------------------|--------------------------|
| A ₀ ~A ₁₂ | Address Inputs |
| R/W | Read/Write Control Input |
| OE | Output Enable Input |
| CE ₁ , CE ₂ | Chip Enable Inputs |
| I/O ₁ ~I/O ₈ | Data Input/Output |
| V _{DD} | Power (+5V) |
| GND | Ground |
| N. C. | No Connection |

vides fast memory access. Thus the TC5565P is suitable for use in various microprocessor application systems where high speed, low power, and battery back up are required.

The TC5565P also features pin compatibility with the 64k bit EPROM (TMM2764D). RAM and EPROM are then interchangeable in the same socket, resulting in flexibility in the definition of the quantity of RAM versus EPROM in microprocessor application systems.

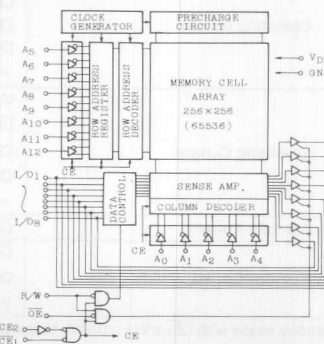
The TC5565P is offered in a dual-in-line 28 pin standard plastic package.

- Access Time

| | TC5565PL-12 TC5565FL-12 | TC5565PL-15 TC5565FL-15 |
|---------------------------------------|----------------------------|----------------------------|
| Address Access Time (MAX.) | 120ns | 150ns |
| CE ₁ Access Time (MAX.) | 120ns | 150ns |
| CE ₂ Access Time (MAX.) | 120ns | 150ns |
| Output Enable Time (MAX.) | 60ns | 70ns |

- Directly TTL Compatible : All Inputs and Outputs
- Standard 28 Pin DIP : TC5565PL-12/PL-15
- Plastic Flat Package : TC5565FL-12/FL-15
- Pin Compatible with 2764 type EPROM

BLOCK DIAGRAM



TC5565PL-12, TC5565PL-15 TC5565FL-12, TC5565FL-15

OPERATION MODE

| OPERATION MODE | \overline{CE}_1 | CE_2 | \overline{OE} | R/W | I/O ₁ ~I/O ₈ | POWER |
|-----------------|-------------------|--------|-----------------|-----|------------------------------------|------------------|
| Read | L | H | L | H | D _{OUT} | I _{DDO} |
| Write | L | H | * | L | D _{IN} | I _{DDO} |
| Output Deselect | L | H | H | H | High-Z | I _{DDO} |
| Standby | H | * | * | * | High-Z | I _{DDS} |
| | * | L | * | * | High-Z | I _{DDS} |

* : H or L

MAXIMUM RATINGS

| SYMBOL | ITEM | RATING | UNIT |
|---------------------|--------------------------|---------------------------|--------|
| V _{DD} | Power Supply Voltage | -0.3~7.0 | V |
| V _{IN} | Input Voltage | -0.3*~7.0 | V |
| V _{I/O} | Input and Output Voltage | -0.5~V _{DD} +0.5 | V |
| P _D | Power Dissipation | 1.0/0.6** | W |
| T _{SOLDER} | Soldering Temperature | 260~10 | °C·Sec |
| T _{STG} | Storage Temperature | -55~150 | °C |
| T _{OPR} | Operating Temperature | 0~70 | °C |

*.....-2.0V at Pulse width 10ns

**...Flat package

D. C RECOMMENDED OPERATING CONDITIONS

| SYMBOL | PARAMETER | MIN. | TYP. | MAX. | UNIT |
|-----------------|-------------------------------|------|------|----------------------|------|
| V _{DD} | Power Supply Voltage | 4.5 | 5.0 | 5.5 | V |
| V _{IH} | Input High Voltage | 2.2 | — | V _{DD} +0.3 | V |
| V _{IL} | Input Low Voltage | -0.3 | — | 0.8 | V |
| V _{DH} | Data Retention Supply Voltage | 2.0 | — | 5.5 | V |

D. C and OPERATING CHARACTERISTICS (Ta=0~70°C, V_{DD}=5V±10%)

| SYMBOL | PARAMETER | TEST CONDITION | MIN. | TYP. | MAX. | UNIT |
|--------------------|------------------------|--|--------------------------|------|------|------|
| I _{IL} | Input Leakage Current | V _{IN} =0~V _{DD} | — | — | ±1.0 | μA |
| I _{OH} | Output High Current | V _{OH} =2.4V | -1.0 | — | — | mA |
| I _{OL} | Output Low Current | V _{OL} =0.4V | 4.0 | — | — | mA |
| I _{LO} | Output Leakage Current | $\overline{CE}_1 = V_{IH}$ or $CE_2 = V_{IH}$ or R/W = V _{IL} or $\overline{OE} = V_{IH}$ V _{OUT} =0~V _{DD} | — | — | ±1.0 | μA |
| I _{DDO1} | Operating Current | V _{DD} =5.5V $\overline{CE}_1 = V_{IL}$ CE ₂ =V _{IH} Other Input = V _{IH} /V _{IL} | t _{cycle} = 1μs | — | 10 | mA |
| | | | | | | |
| I _{DDO2} | Operating Current | V _{DD} =5.5V $\overline{CE}_1 = 0.2V$ CE ₂ =V _{DD} -0.2V Other Input = V _{DD} -0.2V/0.2V | t _{cycle} = 1μs | — | 5 | mA |
| | | | | | | |
| I _{DDS1} | Standby Current | $\overline{CE}_1 = V_{IH}$ or CE ₂ =V _{IL} | — | — | 3 | mA |
| *I _{DDS2} | Standby Current | $\overline{CE}_1 = V_{DD} - 0.2V$ or CE ₂ =0.2V V _{DD} =2.0~5.5V | — | 2 | 100 | μA |

Note : In standby mode with $\overline{CE}_1 \geq V_{DD} - 0.2V$, these specification limits are guaranteed under the condition of CE₂ ≥ V_{DD} - 0.2V or CE₂ ≤ 0.2V.

TC5565PL-12, TC5565PL-15 TC5565FL-12, TC5565FL-15

CAPACITANCE (Ta=25°C)

| SYMBOL | PARAMETER | TEST CONDITION | MAX. | UNIT |
|------------------|--------------------|-----------------------|------|------|
| C _{IN} | Input Capacitance | V _{IN} =GND | 10 | pF |
| C _{OUT} | Output Capacitance | V _{OUT} =GND | 10 | pF |

Note : This parameter periodically sampled is not 100% tested.

A. C. CHARACTERISTICS (Ta=0~70°C, V_{DD}=5V±10%)

Read Cycle

| SYMBOL | PARAMETER | TEST CONDITION | TC5565PL-12 TC5565FL-12 | | TC5565PL-15 TC5565FL-15 | | UNIT |
|------------------|--|---|----------------------------|------|----------------------------|------|------|
| | | | MIN. | MAX. | MIN. | MAX. | |
| t _{RC} | Read Cycle Time | V _{IN} =2.4V/0.6V | 120 | — | 150 | — | ns |
| t _{ACC} | Address Access Time | V _{IH} =2.2V | — | 120 | — | 150 | ns |
| t _{CO1} | $\overline{CE_1}$ Access Time | V _{IL} =0.8V | — | 120 | — | 150 | ns |
| t _{CO2} | CE ₂ Access Time | t _r , t _f ≤5ns | — | 120 | — | 150 | ns |
| t _{OE} | Output Enable to Output in Valid | V _{OH} =2.2V | — | 60 | — | 70 | ns |
| t _{COE} | Chip Enable (CE ₁ , CE ₂) to Output in Low-Z | V _{OL} =0.8V | 10 | — | 10 | — | ns |
| t _{OEE} | Output Enable to Output Low-Z | Output Load : C _L (100pF)and 1•TTL Gate | 5 | — | 5 | — | ns |
| t _{OD} | Chip Enable (CE ₁ , CE ₂) to Output in High-Z | | — | 60 | — | 70 | ns |
| t _{ODO} | Output Enable to Output in High-Z | | — | 50 | — | 60 | ns |
| t _{OH} | Output Data Hold Time | | 20 | — | 20 | — | ns |

Write Cycle

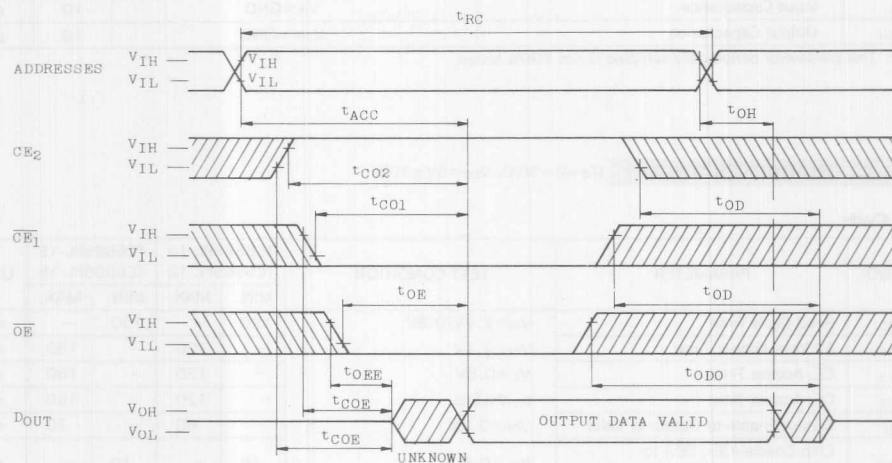
| SYMBOL | PARAMETER | TEST CONDITION | TC5565PL-12 TC5565FL-12 | | TC5565PL-15 TC5565FL-15 | | UNIT |
|------------------|--|--------------------------------------|----------------------------|------|----------------------------|------|------|
| | | | MIN. | MAX. | MIN. | MAX. | |
| t _{WC} | Write Cycle Time | V _{IN} =2.4V/0.6V | 120 | — | 150 | — | ns |
| t _{WP} | Write Pulse Width | V _{IH} =2.2V | 80 | — | 100 | — | ns |
| t _{CW} | Chip Selecion to End of Write | V _{IL} =0.8V | 100 | — | 120 | — | ns |
| t _{AS} | Address Set up Time | t _r , t _f ≤5ns | 0 | — | 0 | — | ns |
| t _{WR} | Write Recovery Time | | 0 | — | 0 | — | ns |
| t _{WRI} | Write Recovery Time (CE ₁ , CE ₂) | | 10 | — | 10 | — | ns |
| t _{ODW} | R/W to Output High-Z | | — | 50 | — | 70 | ns |
| t _{OEW} | R/W to Output Low-Z | | 10 | — | 10 | — | ns |
| t _{DS} | Data Set Up Time | | 50 | — | 60 | — | ns |
| t _{DH} | Data Hold Time | | 0 | — | 0 | — | ns |
| t _{DHI} | Data Hold Time (CE ₁ , CE ₂) | | 10 | — | 10 | — | ns |

Note : Input Pulse Levels=V_{IN}
Timing Measurement Reference Levels=V_{IH}, V_{IL}

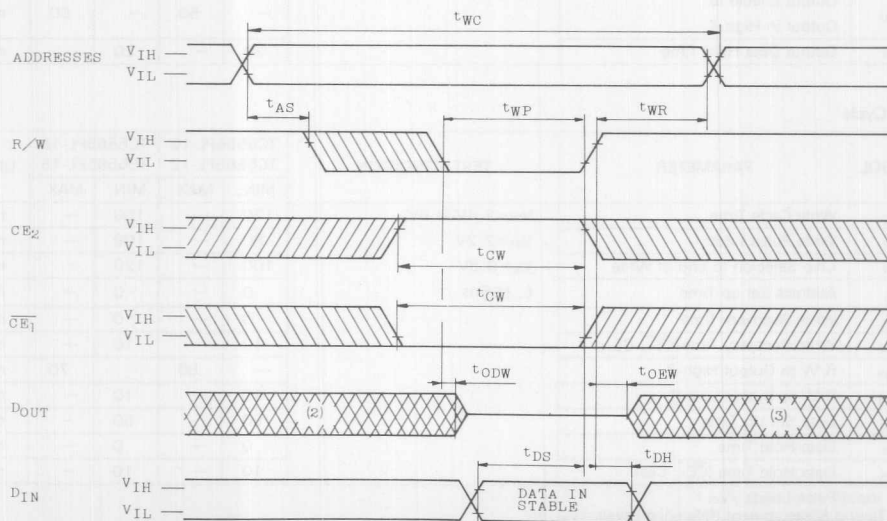
TC5565PL-12, TC5565PL-15 TC5565FL-12, TC5565FL-15

TIMING WAVEFORMS

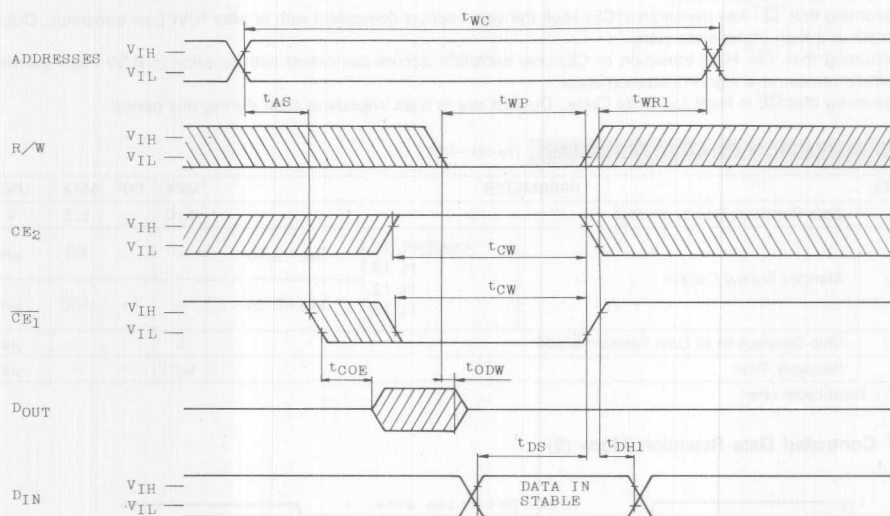
● READ CYCLE (1)



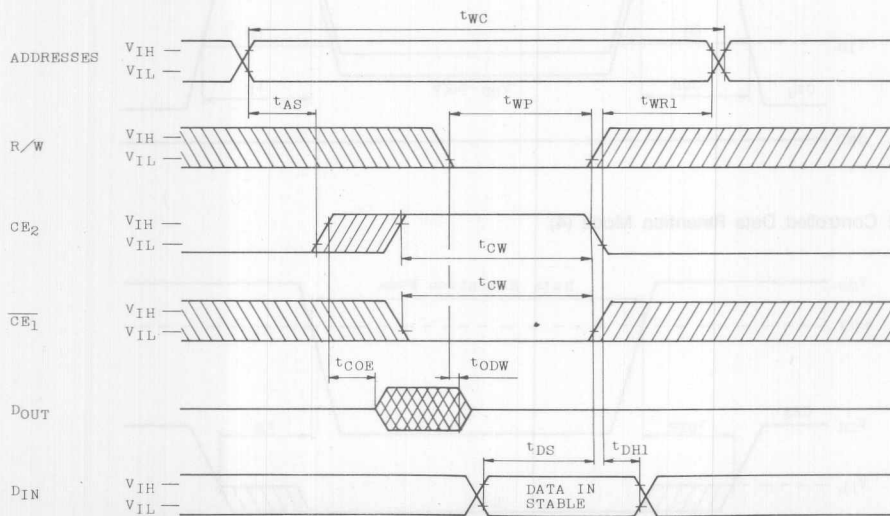
● WRITE CYCLE 1 (4) (R/W Controlled Write)



● WRITE CYCLE 2 (4) ($\overline{CE1}$ Controlled Write)



● WRITE CYCLE 3 (4) ($CE2$ Controlled Write)



TC5565PL-12, TC5565PL-15 TC5565FL-12, TC5565FL-15

Note :

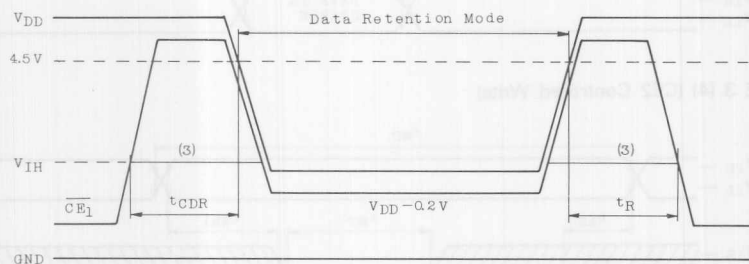
1. R/W is High for Read cycle,
2. Assuming that $\overline{CE_1}$ low transition of CE_2 High transition occurs coincident with or after R/W Low transition, Outputs remain in a high impedance state.
3. Assuming that $\overline{CE_1}$ High transition or CE_2 Low transition occurs coincident with or prior to R/W High transition, Outputs remain in a high impedance state.
4. Assuming that \overline{OE} is High for Write Cycle, Outputs are in high impedance state during this period.

DATA RETENTION CHARACTERISTICS (Ta=0~70°C)

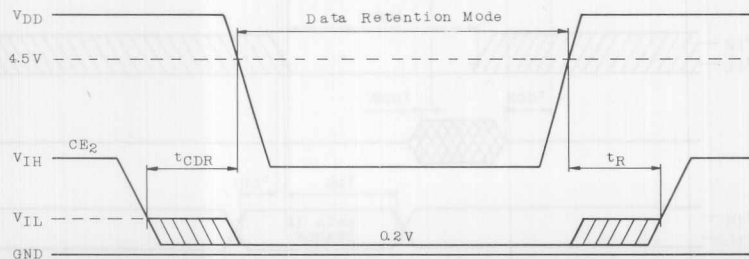
| SYMBOL | PARAMETER | | | MIN. | TYP. | MAX. | UNIT |
|------------|---|----------------------|---------------|-------------|------|------|---------|
| V_{DH} | Data Retention Supply Voltage | | | 2.0 | — | 5.5 | V |
| I_{DPS2} | Standby Supply Current | TC5565PL-12 PL-15 | $V_{DD}=3.0V$ | — | — | 50 | μA |
| | | FL-12 FL-15 | $V_{DD}=5.5V$ | — | — | 100 | μA |
| t_{CDR} | Chip Deselection to Data Retention Mode | | | 0 | — | — | μs |
| t_R | Recovery Time | | | $t_{RC}(1)$ | — | — | μs |

Note (1) : Read cycle time.

● $\overline{CE_1}$ Controlled Data Retention Mode (2)



● CE_2 Controlled Data Retention Mode (4)



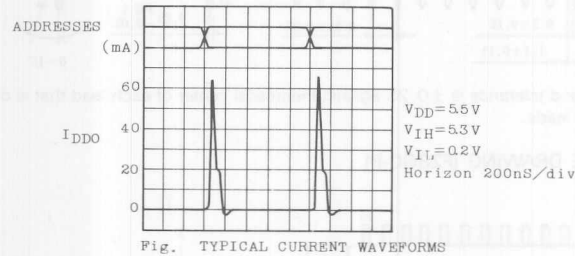
Note :

2. In $\overline{CE_1}$ controlled data retention mode, minimum standby current mode is achieved under the condition of $CE_2 \leq 0.2V$ or $CE_2 \geq V_{DD} - 0.2V$.
3. If the V_{IH} of $\overline{CE_1}$ is 2.2V in operation, I_{DD1} current flows the period that the V_{DD} voltage is going down from 4.5V to 2.4V.
4. In CE_2 controlled data retention mode, minimum standby current mode is achieved under the condition of $CE_2 \leq 0.2V$.

DEVICE INFORMATION

The TC5565P is an asynchronous RAM using address activated circuit technology, thus the internal operation is synchronous. Then once row address change occur, the percharge operation is executed by internal pulse generated from row address transient. Therefore the peak current flows only after row address change, as shown in the following figure.

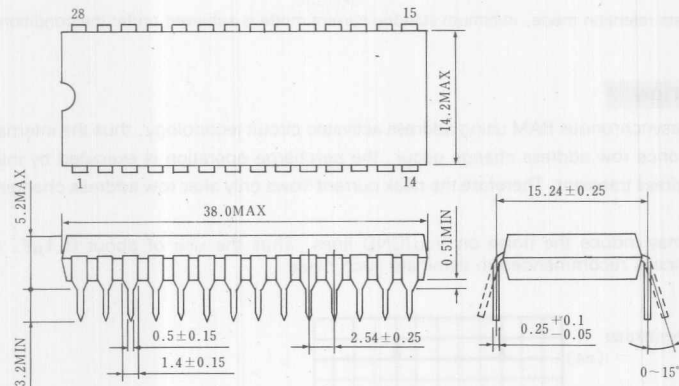
This peak current may induce the noise on V_{DD}/GND lines. Thus the use of about 0.1 μF . decoupling capacitor for every device is recommended to eliminate such noise.



TC5565PL-12, TC5565PL-15 TC5565FL-12, TC5565FL-15

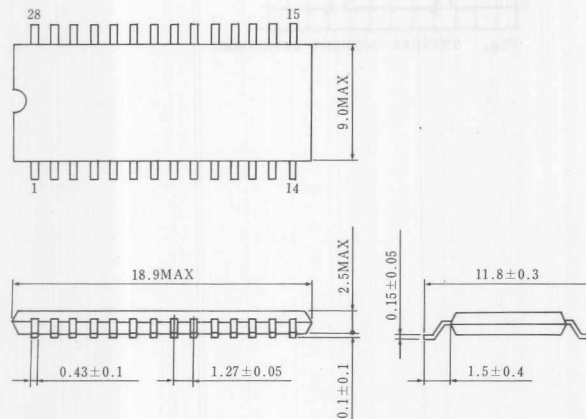
OUTLINE DRAWINGS

● DIP 28 PIN OUTLINE DRAWING (6D28A-P)



Note : Lead pitch is 2.54 and tolerance is ± 0.25 against theoretical center of each lead that is obtained on the basis of No.1 and No.28 leads.

● MFP 28 PIN OUTLINE DRAWING (F28GC-P)



Note : Lead pitch is 1.27 and tolerance is ± 0.12 against theoretical center of each lead that is obtained on the basis of No.1 and No.28 leads.

Note : Toshiba does not assume any responsibility for use of any circuitry described ; no circuit patent licenses are implied, and Toshiba reserves the right, at any time without notice, to change said circuitry.

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TOSHIBA MOS MEMORY PRODUCTS

8,192 WORD \times 8 BIT
CMOS STATIC RAM
SILICON GATE CMOS

TC5565PL-12L, TC5565PL-15L
TC5565FL-12L, TC5565FL-15L

DESCRIPTION

The TC5565P/F is 65,536 bit static random access memory organized as 8,192 words by 8 bits using CMOS technology, and operates from a single 5V supply. Advanced circuit techniques provide both high speed and low power features with a maximum operating current of 5mA/MHz and maximum access time of 120ns/150ns. When \overline{CE}_2 is a logical low or \overline{CE}_1 is a logical high, the device is placed in low power standby mode in which standby current is 0.6 μ A typically. The TC5565P/F has three control inputs. Two chip enables (\overline{CE}_1 , \overline{CE}_2) allow for device selection and data retention control, and an output

enable input (\overline{OE}) provides fast memory access. Thus the TC5565P/F is suitable for use in various microprocessor application systems where high speed, low power, and battery back up are required.

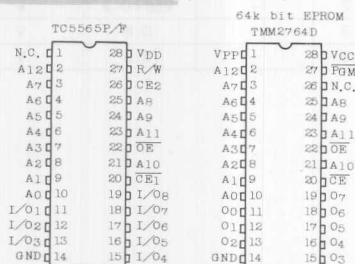
The TC5565P also features pin compatibility with the 64k bit EPROM (TMM2764D). RAM and EPROM are then interchangeable in the same socket, resulting in flexibility in the definition of the quantity of RAM versus EPROM in microprocessor application systems.

The TC5565P is offered in a dual-in-line 28 pin standard plastic package.

FEATURES

- Low Power Dissipation
27.5mW/MHz(Max.) Operating
- Standby Current : 1 μ A(Max.) $T_a=25^\circ\text{C}$
- 5V Single Power Supply
- Power Down Features : \overline{CE}_2 , \overline{CE}_1
- Fully Static Operation
- Data Retention Supply Voltage
: 2.0~5.5V

PIN CONNECTION (TOP VIEW)



PIN NAMES

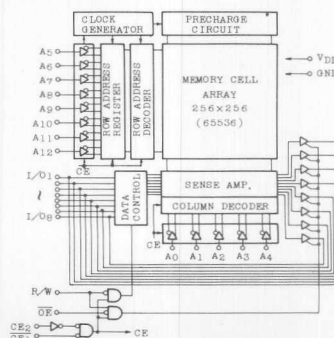
| | |
|---------------------------------------|--------------------------|
| A0~A12 | Address Inputs |
| R/W | Read/Write Control Input |
| \overline{OE} | Output Enable Input |
| \overline{CE}_1 , \overline{CE}_2 | Chip Enable Inputs |
| I/O1~I/O8 | Data Input/Output |
| VDD | Power (+5V) |
| GND | Ground |
| N. C. | No Connection |

Access Time

| | TC5565PL-12L TC5565FL-12L | TC5565PL-15L TC5565FL-15L |
|--------------------------------------|------------------------------|------------------------------|
| Address Access Time (MAX.) | 120ns | 150ns |
| \overline{CE}_1 Access Time (MAX.) | 120ns | 150ns |
| \overline{CE}_2 Access Time (MAX.) | 120ns | 150ns |
| Output Enable Time (MAX.) | 60ns | 70ns |

- Directly TTL Compatible : All Inputs and Outputs
- Standard 28 Pin DIP : TC5565PL-12L/PL-15L
- Plastic Flat Package : TC5565FL-12L/FL-15L
- Pin Compatible with 2764 type EPROM

BLOCK DIAGRAM



TC5565PL-12L, TC5565PL-15L TC5565FL-12L, TC5565FL-15L

OPERATION MODE

| OPERATION MODE | CE ₁ | CE ₂ | OE | R/W | I/O ₁ ~I/O ₈ | POWER |
|-----------------|-----------------|-----------------|----|-----|------------------------------------|------------------|
| Read | L | H | L | H | D _{OUT} | I _{DDO} |
| Write | L | H | * | L | D _{IN} | I _{DDO} |
| Output Deselect | L | H | H | H | High-Z | I _{DDO} |
| Standby | H | * | * | * | High-Z | I _{DDs} |
| | * | L | * | * | High-Z | I _{DDs} |

* : H or L

MAXIMUM RATINGS

| SYMBOL | ITEM | RATING | UNIT |
|---------------------|--------------------------|---------------------------|--------|
| V _{DD} | Power Supply Voltage | -0.3~7.0 | V |
| V _{IN} | Input Voltage | -0.3*~7.0 | V |
| V _{I/O} | Input and Output Voltage | -0.5~V _{DD} +0.5 | V |
| P _D | Power Dissipation | 1.0/0.6** | W |
| T _{SOLDER} | Soldering Temperature | 260*10 | °C*Sec |
| T _{STG} | Storage Temperature | -55~150 | °C |
| T _{OPR} | Operating Temperature | 0~70 | °C |

*-2.0V at Pulse width 10ns

**Flat package

D. C RECOMMENDED OPERATING CONDITIONS

| SYMBOL | PARAMETER | MIN. | TYP | MAX. | UNIT |
|-----------------|-------------------------------|------|-----|----------------------|------|
| V _{DD} | Power Supply Voltage | 4.5 | 5.0 | 5.5 | V |
| V _{IH} | Input High Voltage | 2.2 | — | V _{DD} +0.3 | V |
| V _{IL} | Input Low Voltage | -0.3 | — | 0.8 | V |
| V _{DH} | Data Retention Supply Voltage | 2.0 | — | 5.5 | V |

D. C and OPERATING CHARACTERISTICS (Ta=0~70°C, VDD=5V±10%)

| SYMBOL | PARAMETER | TEST CONDITION | MIN. | TYP. | MAX. | UNIT |
|--------|------------------------|---|-------------------|------|------|------|
| IIL | Input Leakage Current | VIN=0~VDD | — | — | ±1.0 | μA |
| IOH | Output High Current | VOH=2.4V | -1.0 | — | — | mA |
| IOL | Output Low Current | VOL=0.4V | 4.0 | — | — | mA |
| ILO | Output Leakage Current | CE1=VIH or CE2=VIL or R/W=VIL or OE=VIH VOUT=0~VDD | — | — | ±1.0 | μA |
| IDD01 | operating Current | VDD=5.5V CE1=VIL CE2=VIH Other Input=VIH/VIL | tcycle=1μs | — | 10 | mA |
| | | | tcycle=Min. cycle | — | 45 | |
| IDD02 | Operating Current | VDD=5.5V CE1=0.2V CE2=VDD-0.2V Other Input =VDD-0.2V/0.2V | tcycle=1μs | — | 5 | mA |
| | | | tcycle=Min. cycle | — | 40 | |
| IDDs1 | Standby Current | CE1=VIH or CE2=VIL | — | — | 3 | mA |
| *IDDs2 | Standby Current | CE1=VDD-0.2V or CE2=0.2V | Ta=25°C | — | 0.6 | μA |
| | | | Ta=0~70°C | — | 30 | |

Note: In standby mode with CE1≥VDD-0.2V, these specification limits are guaranteed under the condition of CE2≥VDD-0.2V or CE2≤0.2V.

CAPACITANCE (Ta=25°C)

| SYMBOL | PARAMETER | TEST CONDITION | MAX. | UNIT |
|--------|--------------------|----------------|------|------|
| CIN | Input Capacitance | VIN=GND | 10 | pF |
| COUT | Output Capacitance | VOUT=GND | 10 | pF |

Note: This parameter periodically sampled is not 100% tested.

TC5565PL-12L, TC5565PL-15L TC5565FL-12L, TC5565FL-15L

A. C. CHARACTERISTICS

(Ta=0~70°C, VDD=5V±10%)

Read Cycle

| SYMBOL | PARAMETER | TEST CONDITION | TC5565PL-12L TC5565FL-12L | | TC5565PL-15L TC5565FL-15L | | UNIT |
|------------------|--|--|------------------------------|------|------------------------------|------|------|
| | | | MIN. | MAX. | MIN. | MAX. | |
| t _{RC} | Read Cycle Time | V _{IN} =2.4V/0.6V | 120 | — | 150 | — | ns |
| t _{ACC} | Address Access Time | V _{IH} =2.2V | — | 120 | — | 150 | ns |
| t _{CO1} | CE ₁ Access Time | V _{IL} =0.8V | — | 120 | — | 150 | ns |
| t _{CO2} | CE ₂ Access Time | t _{tr} , t _f ≤5ns | — | 120 | — | 150 | ns |
| t _{OE} | Output Enable to Output in Valid | V _{OH} =2.2V | — | 60 | — | 70 | ns |
| t _{COE} | Chip Enable (CE ₁ , CE ₂) to Output in Low-Z | V _{OL} =0.8V | 10 | — | 10 | — | ns |
| t _{OEE} | Output Enable to Output Low-Z | Output Load : C _L (100pF) and I-TTL Gate | 5 | — | 5 | — | ns |
| t _{OD} | Chip Enable (CE ₁ , CE ₂) to Output in High-Z | | — | 60 | — | 70 | ns |
| t _{ODO} | Output Enable to Output in High-Z | | — | 50 | — | 60 | ns |
| t _{OH} | Output Data Hold Time | | 10 | — | 10 | — | ns |

Write Cycle

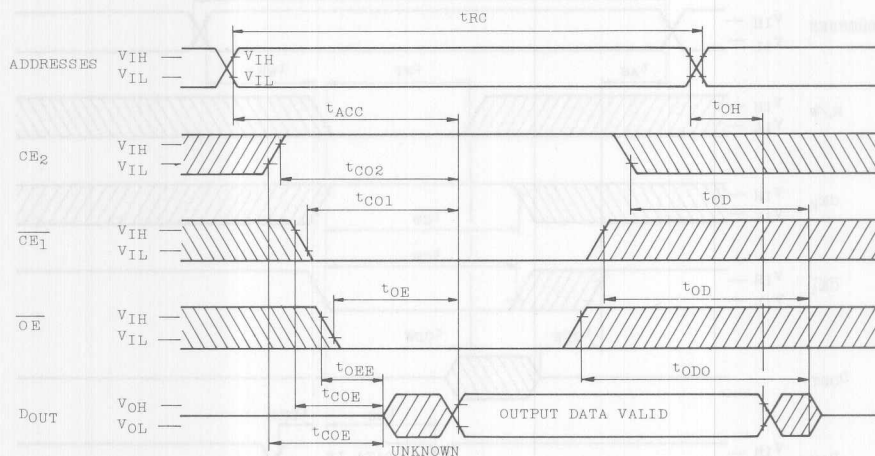
| SYMBOL | PARAMETER | TEST CONDITION | TC5565PL-12L TC5565FL-12L | | TC5565PL-15L TC5565FL-15L | | UNIT |
|------------------|--|---------------------------------------|------------------------------|------|------------------------------|------|------|
| | | | MIN. | MAX. | MIN. | MAX. | |
| t _{WC} | Write Cycle Time | V _{IN} =2.4V/0.6V | 120 | — | 150 | — | ns |
| t _{WP} | Write Pulse Width | V _{IH} =2.2V | 80 | — | 100 | — | ns |
| t _{CW} | Chip Selection to End of Write | V _{IL} =0.8V | 100 | — | 120 | — | ns |
| t _{AS} | Address Set up Time | t _{tr} , t _f ≤5ns | 0 | — | 0 | — | ns |
| t _{WR} | Write Recovery Time | | 0 | — | 0 | — | ns |
| t _{WRI} | Write Recovery Time (CE ₁ , CE ₂) | | 10 | — | 10 | — | ns |
| t _{ODW} | R/W to Output High-Z | | — | 50 | — | 70 | ns |
| t _{OEW} | R/W to Output Low-Z | | 10 | — | 10 | — | ns |
| t _{DS} | Data Set Up Time | | 50 | — | 60 | — | ns |
| t _{DH} | Data Hold Time | | 0 | — | 0 | — | ns |
| t _{DHI} | Data Hold Time (CE ₁ , CE ₂) | | 10 | — | 10 | — | ns |

Note : Input Pulse Levels=V_{IN}

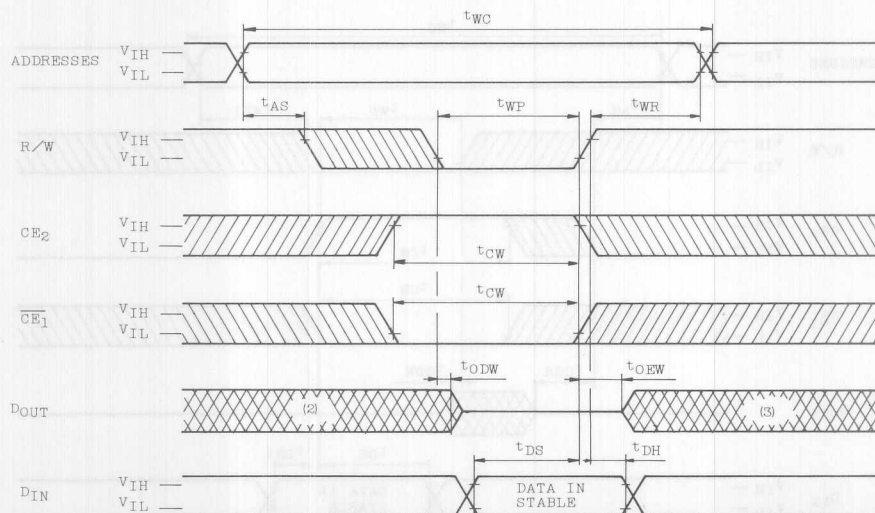
Timing Measurement Reference Levels=V_{IH}, V_{IL}

TIMING WAVEFORMS

● READ CYCLE (1)

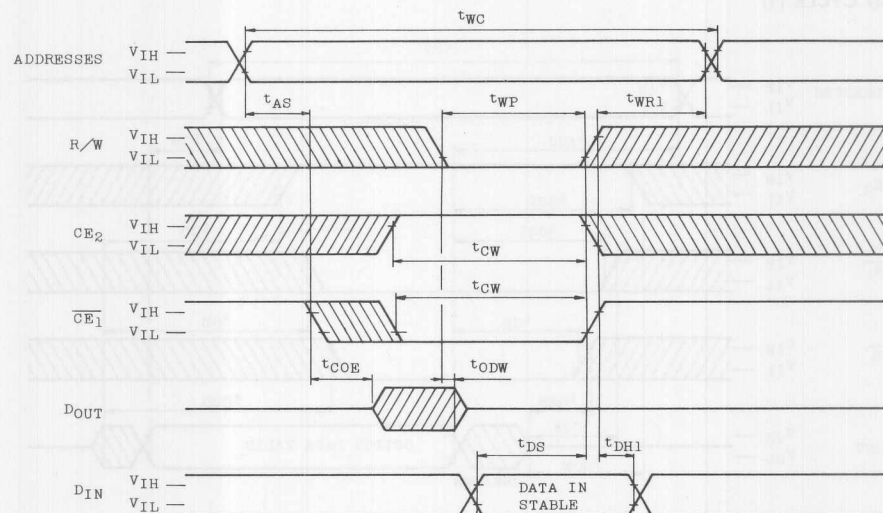


● WRITE CYCLE 1 (4) (R/W Controlled Write)

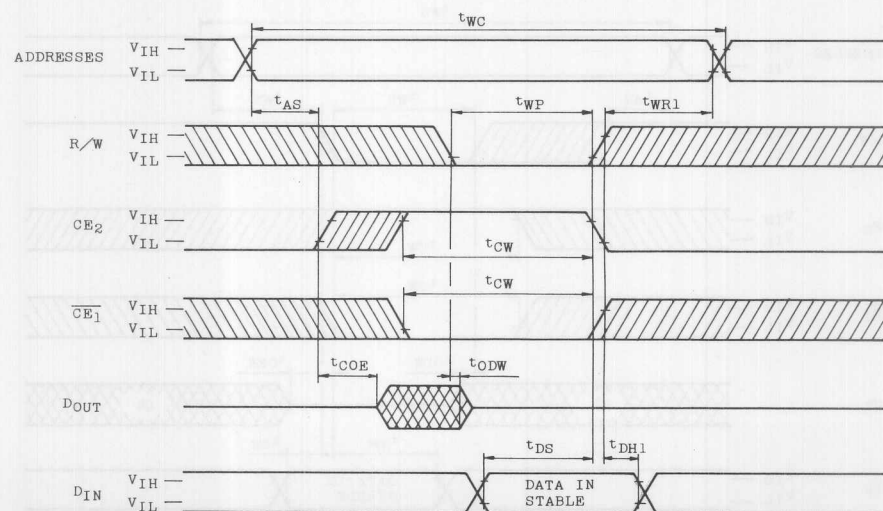


TC5565PL-12L, TC5565PL-15L
TC5565FL-12L, TC5565FL-15L

● WRITE CYCLE 2 (4) (\overline{CE}_1 Controlled Write)



● WRITE CYCLE 3 (4) (CE_2 Controlled Write)



Note :

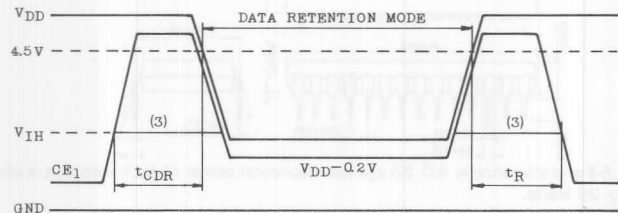
1. R/W is High for Read Cycle.
2. Assuming that \overline{CE}_1 Low transition of \overline{CE}_2 High transition occurs coincident with or after R/W Low transition, Outputs remain in a high impedance state.
3. Assuming that \overline{CE}_1 High transition or \overline{CE}_2 Low transition occur coincident with or prior to R/W High transition, Outputs remain in a high impedance state.
4. Assuming that \overline{OE} is High for Write Cycle, Outputs are in high impedance state during this period.

DATA RETENTION CHARACTERISTICS ($T_a = 0 \sim 70^\circ\text{C}$)

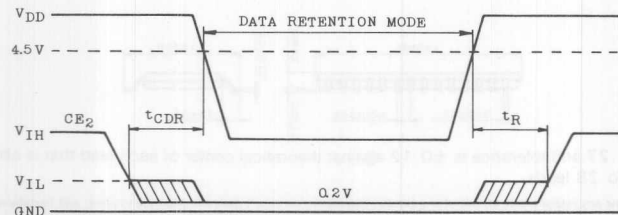
| SYMBOL | PARAMETER | MIN. | TYP. | MAX. | UNIT |
|------------|---|------------------------|------|------|---------------|
| V_{DH} | Data Retention Supply Voltage | 2.0 | — | 5.5 | V |
| I_{DDS2} | Stand by Supply Current | $V_{DD} = 3.0\text{V}$ | — | 15 | μA |
| | | $V_{DD} = 5.5\text{V}$ | — | 30 | |
| t_{CDR} | Chip Deselection to Data Retention Mode | 0 | — | — | μs |
| t_R | Recovery Time | $t_{RC}(1)$ | — | — | μs |

Note (1) : Read cycle time.

● \overline{CE}_1 Controlled Data Retention Mode (2)



● \overline{CE}_2 Controlled Data Retention Mode (4)



TC5565PL-12L, TC5565PL-15L **TC5565FL-12L, TC5565FL-15L**

Note :

2. In \overline{CE}_1 controlled data retention mode, minimum standby current mode is achieved under the condition of $CE_2 \leq 0.2V$ or $CE_2 \geq V_{DD} - 0.2V$.
3. If the V_{IH} of \overline{CE}_1 is 2.2V in operation, I_{DD1} current flows during the period that the V_{DD} voltage is going down from 4.5V to 2.4V.
4. In CE_2 controlled data retention mode, minimum standby current mode is achieved under the condition of $CE_2 \leq 0.2V$.

DEVICE INFORMATION

The TC5565P/F is an synchronous RAM using address activated circuit technology, thus the internal operation is synchronous. Then once row address change occur, the percharge operation is executed by internal pulse generated from row address transient. Therefore the peak current flows only after row address change, as shown in the following figure. This peak current may induce the noise on V_{DD}/GND lines. Thus the use of about 0.1 μF decoupling capacitor for every device is recommended to eliminate such noise.

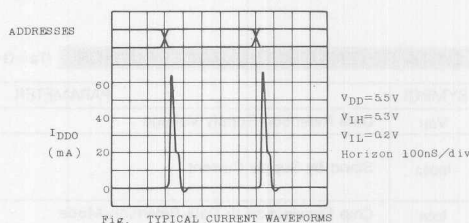
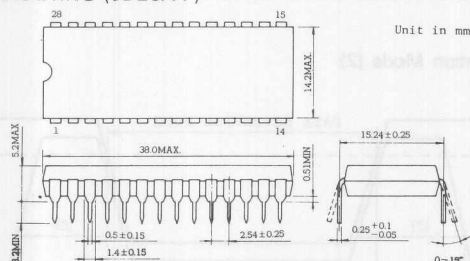


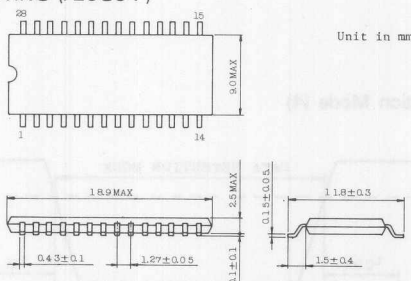
Fig. 1. TYPICAL CURRENT WAVEFORMS

● DIP 28 PIN OUTLINE DRAWING (6D28A-P)



Note : Lead pitch is 2.54 and tolerance is ± 0.25 against theoretical center of each lead that is obtained on the basis of No. 1 and No. 28 leads.

● MFP 28 PIN OUTLINE DRAWING (F28GC-P)



Note : Lead pitch is 1.27 and tolerance is ± 0.12 against theoretical center of each lead that is obtained on the basis of No. 1 and No. 28 leads.

Note : Toshiba does not assume any responsibility for use of any circuitry described ; no circuit patent licenses are implied, and Toshiba reserves the right, at any time without notice, to change said circuitry.

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TOSHIBA MOS MEMORY PRODUCTS

65,536 WORD \times 1 BIT CMOS STATIC RAM
SILICON GATE CMOS

TC5561P-55
TC5561P-70

PRELIMINARY

DESCRIPTION

The TC5561P is a 65,536 bit high speed static random access memory organized as 65,536 words by 1 bit using CMOS technology, and Operated from a single 5-volt supply.

Toshiba's high performance device technology provides both high speed and low power features with a maximum access time of 55ns/70ns and maximum operating current of 100mA at minimum cycle time.

The TC5561P also features an automatic stand-by mode. When deselected by Chip Enable (CE), the

operating current is reduced from 100mA to 100 μ A.

The TC5561P is suitable for use in main memory of high speed computer and pattern memory, where high speed/low power/high density are required.

The TC5561P is moulded in a 22 pin standard plastic package with 0.3 inch width for high density assembly.

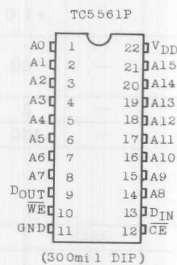
The TC5561P is fabricated with ion implanted COMS silicon gate MOS technology for high performance and high reliability.

FEATURES

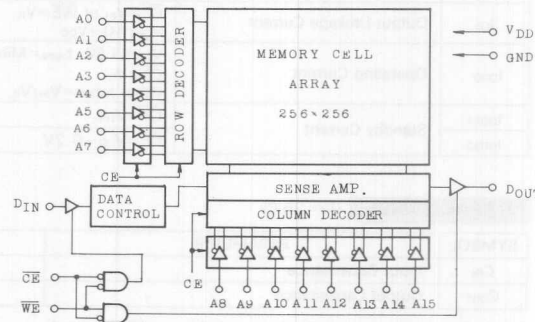
- Fast access time : TC5561P-55 55ns(MAX.)
TC5561P-70 70ns(MAX.)
- Low power dissipation : Operation 100mA(MAX.)
Standby 100 μ A(MAX.)
- 5V single power supply

- Fully static operation
- Directly TTL compatible : All Input and Output
- I/O separate
- Package : 22 pin standard plastic package, 300mil width

PIN CONNECTION (TOP VIEW)



BLOCK DIAGRAM



PIN NAMES

| | |
|---------------------------------|--------------------|
| A ₀ ~A ₁₅ | Address Inputs |
| D _{IN} | Data Input |
| D _{OUT} | Data Output |
| CE | Chip Enable Input |
| WE | Write Enable Input |
| V _{DD} | Power (+5V) |
| GND | Ground |

TC5561P-55

TC5561P-70

MAXIMUM RATINGS

| SYMBOL | ITEM | RATING | UNIT |
|---------------------|--------------------------|---------------------------|--------|
| V _{DD} | Power Supply Voltage | -0.3~7.0 | V |
| V _{IN} | Input Voltage | -2.0~7.0 | V |
| V _{I/O} | Input and Output Voltage | -0.5~V _{DD} +0.5 | V |
| P _D | Power Dissipation | 650 | mW |
| T _{SOLDER} | Soldering Temperature | 260 ± 10 | °C·sec |
| T _{STG} | Storage Temperature | -65~150 | °C |
| T _{OPR} | Operating Temperature | 0~70 | °C |

D. C. RECOMMENDED OPERATING CONDITIONS

| SYMBOL | PARAMETER | MIN. | TYP. | MAX. | UNIT |
|-----------------|----------------------|------|------|----------------------|------|
| V _{DD} | Power Supply Voltage | 4.5 | 5.0 | 5.5 | V |
| V _{IH} | Input High Voltage | 2.2 | — | V _{DD} +0.3 | V |
| V _{IL} | Input Low Voltage | -3.0 | — | 0.8 | V |

D. C. and OPERATING CHARACTERISTICS (Ta=0~70°C, V_{DD}=5V±10%)

| SYMBOL | PARAMETER | TEST CONDITION | MIN. | TYP. | MAX. | UNIT |
|--------------------|------------------------|---|------|------|------|------|
| I _{IN} | Input Leakage Current | V _{IN} =0~V _{DD} | — | — | ±1.0 | μA |
| I _{OH} | Output High Current | V _{OH} =2.4V | -8 | — | — | mA |
| I _{OL} | Output Low Current | V _{OL} =0.4V | 8 | — | — | mA |
| I _{LO} | Output Leakage Current | CE=V _{IH} or WE=V _{IL} V _{OUT} =0~V _{DD} | — | — | ±1.0 | μA |
| I _{DDO} | Operating Current | V _{DD} =5.5V, t _{cycle} =Min cycle, CE=V _{IL} Other Input=V _{IH} /V _{IL} | — | — | 100 | mA |
| I _{DD} S1 | Standby Current | CE=V _{IH} | — | — | 2 | mA |
| I _{DD} S2 | | CE=V _{DD} -0.2V | — | — | 100 | μA |

CAPACITANCE (Ta=25°C)

| SYMBOL | PARAMETER | TEST CONDITION | MAX. | UNIT |
|------------------|--------------------|-----------------------|------|------|
| C _{IN} | Input Capacitance | V _{IN} =GND | 10 | pF |
| C _{OUT} | Output Capacitance | V _{OUT} =GND | 10 | pF |

Note : This parameter periodically sampled is not 100% tested.

A. C. CHARACTERISTICS

($T_a = 0 \sim 70^\circ\text{C}$, $V_{DD} = 5\text{V} \pm 10\%$)

Read Cycle

| SYMBOL | PARAMETER | TC5561P-55 | | TC5561P-70 | | UNIT |
|-----------|----------------------------------|------------|------|------------|------|------|
| | | MIN. | MAX. | MIN. | MAX. | |
| t_{RC} | Read Cycle Time | 55 | — | 70 | — | ns |
| t_{ACC} | Address Access Time | — | 55 | — | 70 | |
| t_{CO} | Chip Enable Access Time | — | 55 | — | 70 | |
| t_{COE} | Chip Enable to Output in Low-Z | 5 | — | 5 | — | |
| t_{COD} | Chip Disable to Output in High-Z | — | 30 | — | 30 | |
| t_{OH} | Output Data Hold Time | 5 | — | 5 | — | |

Write Cycle

| SYMBOL | PARAMETER | TC5561P-55 | | TC5561P-70 | | UNIT |
|------------|----------------------------------|------------|------|------------|------|------|
| | | MIN. | MAX. | MIN. | MAX. | |
| t_{WC} | Write Cycle Time | 55 | — | 70 | — | ns |
| t_{WP} | Write Pulse Width | 35 | — | 35 | — | |
| t_{CW} | Chip Enable to End of Write | 35 | — | 35 | — | |
| t_{AS} | Address Set up Time | 0 | — | 0 | — | |
| t_{WR} | Write Recovery Time | 0 | — | 0 | — | |
| t_{ODW} | \overline{WE} to Output Low-Z | — | 30 | — | 30 | |
| t_{ODEW} | \overline{WE} to Output High-Z | 5 | — | 5 | — | |
| t_{DS} | Data Set up Time | 35 | — | 35 | — | |
| t_{DH} | Data Hold Time | 0 | — | 0 | — | |

A. C. TEST CONDITIONS

| | |
|--|------------|
| Input Pulse Levels | 0~3.5V |
| Input Rise and Fall Times | 5ns |
| Input and Output Timing Reference Levels | 1.5V |
| Output Load | See Fig. 1 |

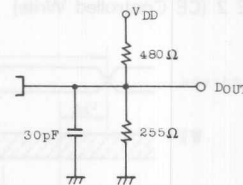
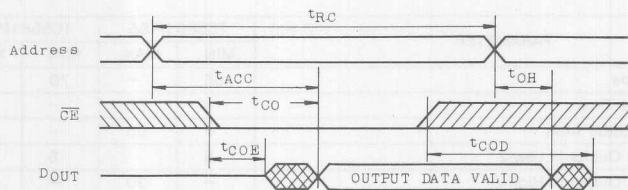


Fig.1 Output Load

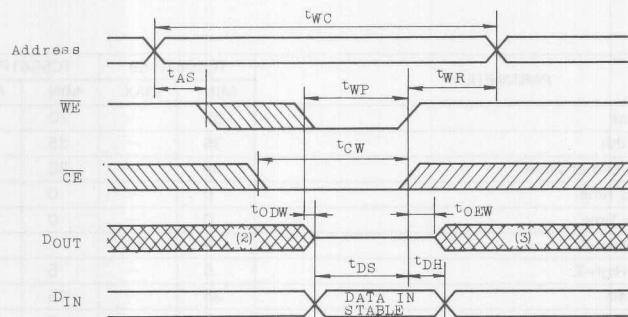
TC5561P-55 TC5561P-70

TIMING WAVEFORMS

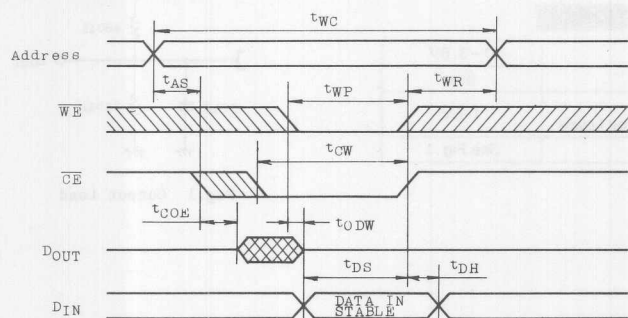
● READ CYCLE (1)



● WRITE CYCLE 1 (\overline{WE} Controlled Write)



● WRITE CYCLE 2 (\overline{CE} Controlled Write)

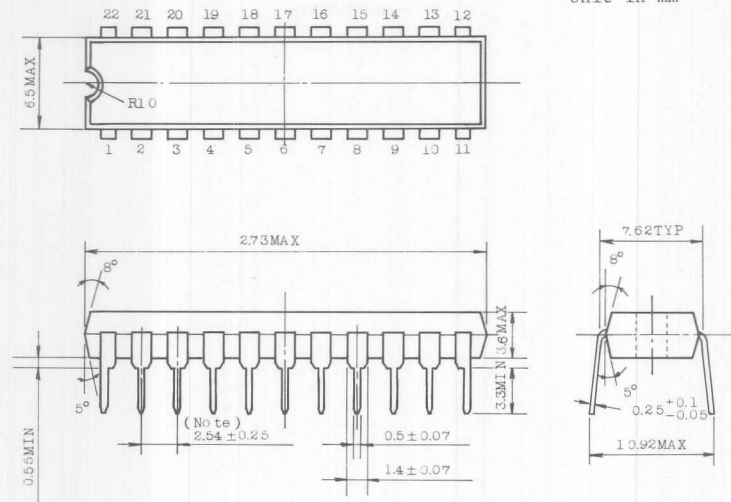


Note :

1. \overline{WE} is High for Read Cycle.
2. Assuming that \overline{CE} Low transition occurs coincident with or after \overline{WE} Low transition, Outputs remain in a high impedance state.
3. Assuming that \overline{CE} High transition occurs coincident with or prior to \overline{WE} High transition, Outputs remain in a high impedance state.
4. The operating temperature(T_a) is guaranteed with transverse air flow exceeding 400 linear feet per minute.

OUTLINE DRAWINGS

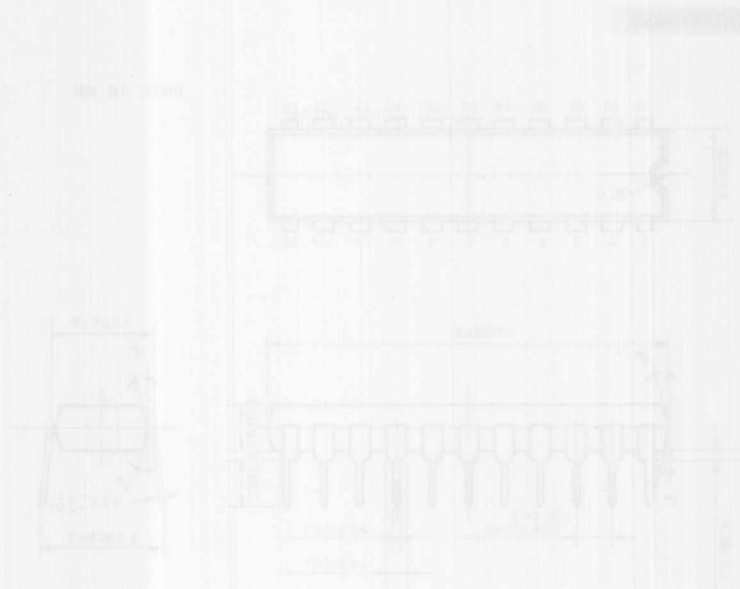
Unit in mm



Note : Each lead pitch is 2.54mm.

All leads are located within 0.25mm of the true longitudinal position with respect to No.1 and No.22 leads.

TC5561P-55 TC5561P-70



Note : Toshiba does not assume any responsibility for use of any circuitry described ; no circuit patent licenses are implied, and Toshiba reserves the right, at any time without notice, to change said circuitry.
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TOSHIBA MOS MEMORY PRODUCTS

65,536 WORD × 1 BIT CMOS STATIC RAM
SILICON GATE CMOS

TC5562P-45
TC5562P-55

PRELIMINARY

DESCRIPTION

The TC5562P is a 65,536 bit high speed static random access memory organized as 65,536 words by 1 bit using CMOS technology, and operated from a single 5-volt supply.

Toshiba's high performance device technology provides both high speed and low power features with a maximum access time of 45ns/55ns and maximum operating current of 100mA at minimum cycle time.

The TC5562P also features and automatic stand-

by mode. When deselected by chip Enable (\overline{CE}), the operating current is reduced from 100mA to 20mA.

The TC5562P is suitable for use in main memory of high speed/high density are required.

The TC5562P is moulded in a 22 pin standard plastic package with 0.3 inch width for high density assembly.

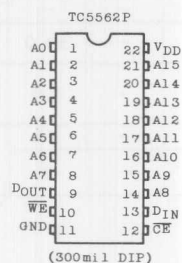
The TC5562P is fabricated with ion implanted COMS silicon gate MOS technology for high performance and high reliability.

FEATURES

- Fast access time : TC5562P-45 45ns(MAX.)
TC5562P-55 55ns(MAX.)
- Low power dissipation : Operation 100mA(MAX.)
Standby 20mA(MAX.)
- 5V single power supply

- Fully Static operation
- Directly TTL compatible : All Input and Output
- I/O separate
- Package : 22 pin standard plastic package, 300mil width

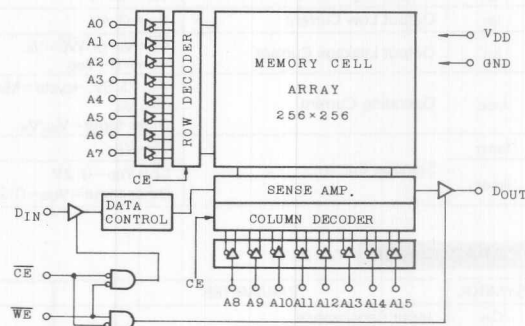
PIN CONNECTION (TOP VIEW)



PIN NAMES

| | |
|-----------------|--------------------|
| A0~A15 | Address Inputs |
| DIN | Data Input |
| DOUT | Data Output |
| \overline{CE} | Chip Enable Input |
| WE | Write Enable Input |
| VDD | Power (+5V) |
| GND | Ground |

BLOCK DIAGRAM



TC5562P-45

TC5562P-55

MAXIMUM RATINGS

| SYMBOL | ITEM | RATING | UNIT |
|---------------------|--------------------------|---------------------------|--------|
| V _{DD} | Power Supply Voltage | -0.3~7.0 | V |
| V _{IN} | Input Voltage | -2.0~7.0 | V |
| V _{I/O} | Input and Output Voltage | -0.5~V _{DD} +0.5 | V |
| P _D | Power Dissipation | 650 | mW |
| T _{SOLDER} | Soldering Temperature | 260 ± 10 | °C·sec |
| T _{STG} | Storage Temperature | -65~150 | °C |
| T _{OPR} | Operating Temperature | 0~70 | °C |

D. C. RECOMMENDED OPERATING CONDITIONS

| SYMBOL | PARAMETER | MIN. | TYP. | MAX. | UNIT |
|-----------------|-------------------------------|------|------|----------------------|------|
| V _{DD} | Power Supply Voltage | 4.5 | 5.0 | 5.5 | V |
| V _{IH} | Input High Voltage | 2.2 | — | V _{DD} +0.3 | V |
| V _{IL} | Input Low Voltage | -3.0 | — | 0.8 | V |
| V _{DH} | Data Retention Supply Voltage | 2.0 | — | 5.5 | V |

D. C and OPERATING CHARACTERISTICS (Ta=0~70°C, V_{DD}=5V±10%)

| SYMBOL | PARAMETER | TEST CONDITION | MIN. | TYP. | MAX. | UNIT |
|-------------------|------------------------|---|------|------|------|------|
| I _{IL} | Input Leakage Current | V _{IN} =0~V _{DD} | — | — | ±1.0 | μA |
| I _{OH} | Output High Current | V _{OH} =2.4V | -8 | — | — | mA |
| I _{OL} | Output Low Current | V _{OL} =0.4V | 8 | — | — | mA |
| I _{LO} | Output Leakage Current | CE=V _{IH} or WE=V _{IL} V _{OUT} =0~V _{DD} | — | — | ±1.0 | μA |
| I _{DDO} | Operating Current | V _{DD} =5.5V, t _{cycle} =Min cycle, CE=V _{IL} Other Input=V _{IH} /V _{IL} | — | — | 100 | mA |
| I _{DDs1} | Standby Current | CE=V _{IH} | — | — | 20 | mA |
| I _{DDs2} | | CE=V _{DD} -0.2V Other Input=V _{DD} -0.2V or 0.2V | — | — | 2 | |

CAPACITANCE (Ta=25°C)

| SYMBOL | PARAMETER | TEST CONDITION | MAX. | UNIT |
|------------------|--------------------|-----------------------|------|------|
| C _{IN} | Input Capacitance | V _{IN} =GND | 10 | pF |
| C _{OUT} | Output Capacitance | V _{OUT} =GND | 10 | pF |

Note : This parameter periodically sampled is not 100% tested.

A. C. CHARACTERISTICS

(Ta=0~70°C, VDD=5V±10%)

Read Cycle

| SYMBOL | PARAMETER | TC5562P-45 | | TC5562P-55 | | UNIT |
|------------------|----------------------------------|------------|------|------------|------|------|
| | | MIN. | MAX. | MIN. | MAX. | |
| t _{RC} | Read Cycle Time | 45 | — | 55 | — | ns |
| t _{ACC} | Address Access Time | — | 45 | — | 55 | |
| t _{CO} | Chip Enable Access Time | — | 45 | — | 55 | |
| t _{COE} | Chip Enable to Output in Low-Z | 5 | — | 5 | — | |
| t _{COH} | Chip Disable to Output in High-Z | — | 25 | — | 30 | |
| t _{OH} | Output Data Hold Time | 5 | — | 5 | — | |

Write Cycle

| SYMBOL | PARAMETER | TC5562P-45 | | TC5562P-55 | | UNIT |
|------------------|-----------------------------|------------|------|------------|------|------|
| | | MIN. | MAX. | MIN. | MAX. | |
| t _{WC} | Write Cycle Time | 45 | — | 55 | — | ns |
| t _{WP} | Write Pulse Width | 30 | — | 35 | — | |
| t _{CW} | Chip Enable to End of Write | 30 | — | 35 | — | |
| t _{AS} | Address Set up Time | 0 | — | 0 | — | |
| t _{WR} | Write Recovery Time | 0 | — | 0 | — | |
| t _{ODW} | WE to Output Low-Z | — | 25 | — | 30 | |
| t _{OEW} | WE to Output High-Z | 5 | — | 5 | — | |
| t _{DS} | Data Set up Time | 30 | — | 35 | — | |
| t _{DH} | Data Hold Time | 0 | — | 0 | — | |

A. C. TEST CONDITIONS

| | |
|--|------------|
| Input Pulse Levels | 0~3.5V |
| Input Rise and Fall Times | 5ns |
| Input and Output Timing Reference Levels | 1.5V |
| Output Load | See Fig. 1 |

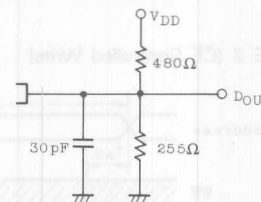
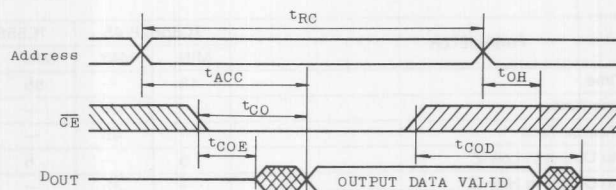


Fig.1 Output Load

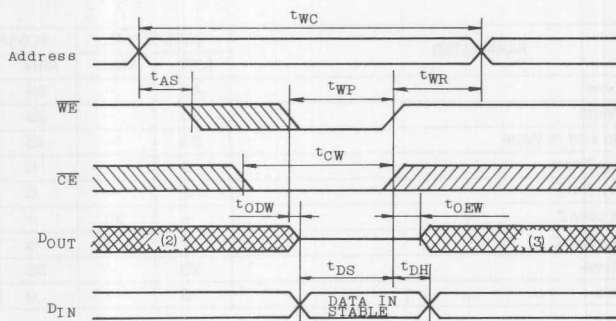
TC5562P-45 TC5562P-55

TIMING WAVEFORMS

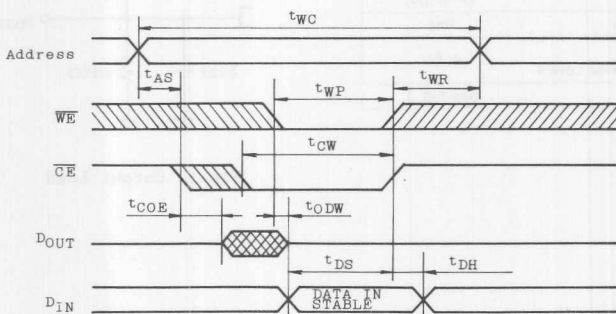
● READ CYCLE (1)



● WRITE CYCLE 1 (\overline{WE} Controlled Write)



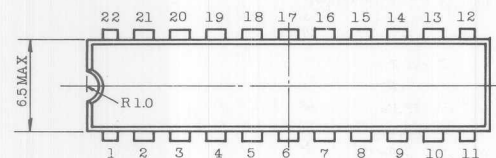
● WRITE CYCLE 2 (\overline{CE} Controlled Write)



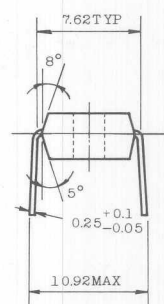
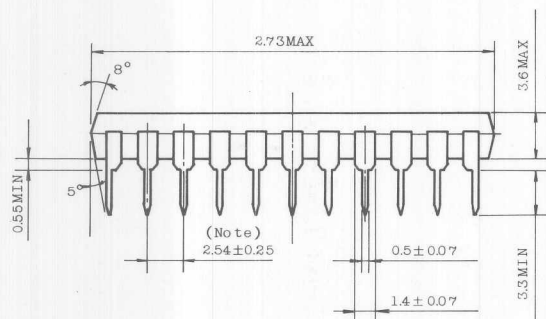
Note :

1. \overline{WE} is High for Read Cycle.
2. Assuming that \overline{CE} Low transition occurs coincident with or after \overline{WE} Low transition, Outputs remain in a high impedance state.
3. Assuming that \overline{CE} High transition occurs coincident with or prior \overline{WE} High transition, Outputs remain in a high impedance state.
4. The operating temperature(T_a) is guaranteed with transverse air flow exceeding 400 linear feet per minute.

OUTLINE DRAWINGS

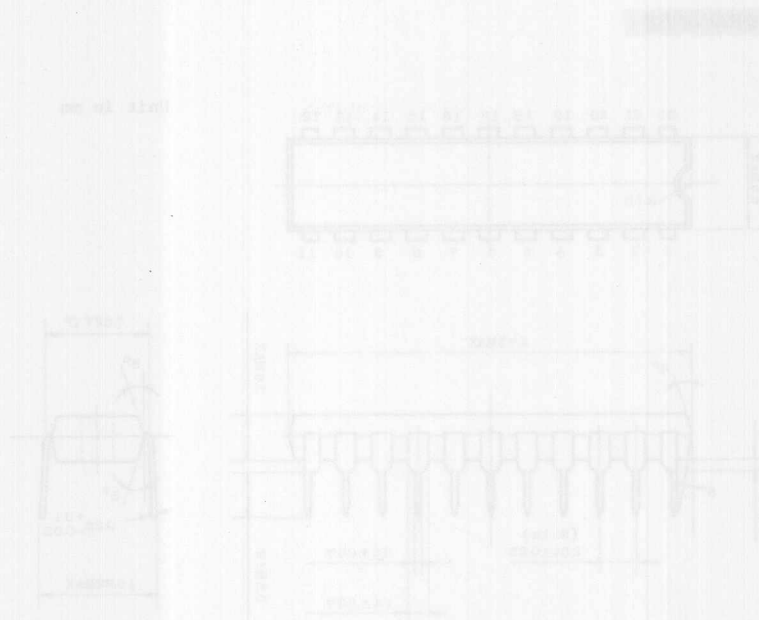


Unit in mm



Note : Each lead pitch is 2.54mm.
All leads are located within 0.25mm of the true longitudinal position with respect to No.1 and No.22 leads.

TC5562P-45 TC5562P-55



Note : Toshiba does not assume any responsibility for use of any circuitry described ; no circuit patent licenses are implied, and Toshiba reserves the right, at any time without notice, to change said circuitry.
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TOSHIBA MOS MEMORY PRODUCTS

32,768 WORD × 8 BIT CMOS STATIC RAM
SILICON GATE CMOS

TC55257P-10/PL-10
TC55257P-12/PL-12

DESCRIPTION

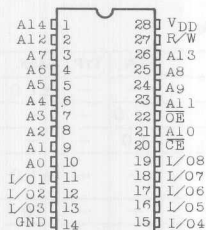
The TC55257P is 262,144 bit static random access memory organized as 32,768 words by 8 bits using CMOS technology, and operated a single 5V supply. Advanced circuit techniques provide both high speed and low power features with a maximum operating current of 5mA/MHz and minimum cycle time of 100ns/120ns.

When \overline{CE} is a logical high, the device is placed in low power standby mode in which standby current is

FEATURES

- Low Power Dissipation
27.5mW/MHz(Max.) Operating
- Standby Current
100 μ A(Max.): TC55257PL-10/PL-12
1mA(Max.) TC55257P-10/P-12
- 5V Single Power Supply
- Power Down Feature : \overline{CE}
- Data Retention Supply Voltage : 2.0~5.5V

PIN CONNECTION (TOP VIEW)



PIN NAMES

| | |
|-----------------|--------------------------|
| A0~A14 | Address Inputs |
| R/W | Read/Write Control Input |
| \overline{OE} | Output Enable Input |
| \overline{CE} | Chip Enable Input |
| I/O1~I/O8 | Data Input/Output |
| VDD | Power (+5V) |
| GND | Ground |

PRELIMINARY

2 μ A typically. The TC55257P has two control inputs. Chip enable input (\overline{CE}) allow for device selection and data retention control, and an output enable input (\overline{OE}) provides fast memory access. Thus the TC55257P is suitable for use in various microprocessor application systems where high speed, low power, and battery back up are required.

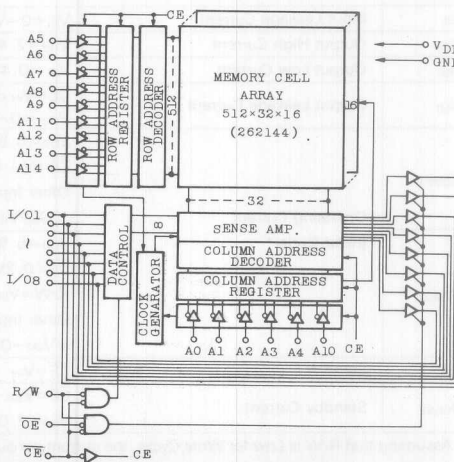
The TC55257P is offered in a dual-in-line 28 pin standard plastic package.

Access Time

| | TC55257P-10 TC55257PL-10 | TC55257P-12 TC55257PL-12 |
|------------------------------------|-----------------------------|-----------------------------|
| Access Time (MAX.) | 100ns | 120ns |
| \overline{CE} Access Time (MAX.) | 100ns | 120ns |
| Output Enable Time (MAX.) | 50ns | 60ns |

- Directly TTL Compatible : All Inputs and Outputs
- Standard 28 pin DIP

BLOCK DIAGRAM



TC55257P-10/PL-10

TC55257P-12/PL-12

OPERATION MODE

| OPERATION MODE | CE | OE | R/W | I/O ₁ ~I/O ₈ | POWER |
|-----------------|----|----|-----|------------------------------------|------------------|
| Read | L | L | H | D _{OUT} | I _{DDO} |
| Write | L | * | L | D _{IN} | I _{DDO} |
| Output Deselect | L | H | H | High-Z | I _{DDO} |
| Standby | H | * | * | High-Z | I _{DDs} |

*) H or L

MAXIMUM RATINGS

| SYMBOL | ITEM | RATING | UNIT |
|---------------------|--------------------------|---------------------------|--------|
| V _{DD} | Power Supply Voltage | -0.3~7.0 | V |
| V _{IN} | Input Voltage | -2.0~7.0 | V |
| V _{I/O} | Input and Output Voltage | -0.5~V _{DD} +0.5 | V |
| P _D | Power Dissipation | 1.0 | W |
| T _{SOLDER} | Soldering Temperature | 260~10 | °C·sec |
| T _{STG} | Storage Temperature | -55~150 | °C |
| T _{OPR} | Operating Temperature | 0~70 | °C |

D. C. RECOMMENDED OPERATING CONDITIONS

| SYMBOL | PARAMETER | MIN. | TYP. | MAX. | UNIT |
|-----------------|-------------------------------|------|------|----------------------|------|
| V _{DD} | Power Supply Voltage | 4.5 | 5.0 | 5.5 | V |
| V _{IH} | Input High Voltage | 2.2 | — | V _{DD} +0.3 | V |
| V _{IL} | Input Low Voltage | -0.3 | — | 0.8 | V |
| V _{DH} | Data Retention Supply Voltage | 2.0 | — | 5.5 | V |

D. C. and OPERATING CHARACTERISTICS (Ta=0~70°C, V_{DD}=5V±10%)

| SYMBOL | PARAMETER | TEST CONDITION | MIN. | TYP. | MAX. | UNIT |
|-------------------|------------------------------------|--|------------------------------------|------|------|------|
| I _{IL} | Input Leakage Current | V _{IN} =0~V _{DD} | — | — | ±1.0 | μA |
| I _{OH} | Output High Current | V _{OH} =2.4V | -1.0 | — | — | mA |
| I _{OL} | Output Low Current | V _{OL} =0.4V | 4.0 | — | — | mA |
| I _{LO} | Output Leakage Current | CE=V _{IH} or R/W=V _{IL} or OE=V _{IH} V _{OUT} =0~V _{DD} | — | — | ±1.0 | μA |
| I _{DDO1} | Operating Current (Read Cycle)* | V _{DD} =5.5V CE=V _{IL} , R/W=V _{IH} Other Input = V _{IH} /V _{IL} | t _{cycle} =1μs | — | — | 10 |
| | | | t _{cycle} = Min. cycle | — | — | 45 |
| I _{DDO2} | | V _{DD} =5.5V CE=0.2V R/W=V _{DD} -0.2V Other Input = V _{DD} -0.2V/0.2V | t _{cycle} =1μs | — | — | 5 |
| | | | t _{cycle} = Min. cycle | — | — | 40 |
| I _{DDs1} | Standby Current | CE=V _{IH} | — | — | 3 | mA |
| I _{DDs2} | Standby Current | CE=V _{DD} -0.2V | TC55257PL | — | 2 | 100 |
| | | V _{DD} =2.0~5.5V | TC55257P | — | — | 1.0 |

* Assuming that R/W is Low for Write Cycle, the current consumption is twice as much as that when R/W is High for Write Cycle.

TC55257P-10/PL-10

TC55257P-12/PL-12

CAPACITANCE (Ta=25°C, f=1MHz)

| SYMBOL | PARAMETER | TEST CONDITION | MAX. | UNIT |
|------------------|--------------------|-----------------------|------|------|
| C _{IN} | Input Capacitance | V _{IN} =GND | 10 | pF |
| C _{OUT} | Output Capacitance | V _{OUT} =GND | 10 | pF |

Note : This parameter periodically sampled is not 100% tested.

A. C. CHARACTERISTICS (Ta=0~70°C, V_{DD}=5V±10%)

Read Cycle

| SYMBOL | PARAMETER | TEST CONDITION | TC55257P-10 TC55257PL-10 | | TC55257P-12 TC55257PL-12 | | UNIT |
|------------------|--------------------------------------|---|-----------------------------|------|-----------------------------|------|------|
| | | | MIN. | MAX. | MIN. | MAX. | |
| t _{RC} | Read Cycle Time | V _{IN} =2.4V/0.6V | 100 | — | 120 | — | ns |
| t _{ACC} | Address Access Time | V _{IH} =2.2V | — | 100 | — | 120 | |
| t _{CO} | CE Access Time | V _{IL} =0.8V | — | 100 | — | 120 | |
| t _{OE} | Output Enable to Output in Valid | t _r , t _r ≤10ns | — | 50 | — | 60 | |
| t _{COE} | Chip Enable(CE)to Output in Low-Z | V _{OH} =2.2V | 10 | — | 10 | — | |
| t _{OEE} | Output Enable to Output Low-Z | V _{OL} =0.8V | 5 | — | 5 | — | |
| t _{OD} | Chip Enable (CE) to Output in High-Z | Output Load : C _L (100pF)and 1 TTL Gate | — | 50 | — | 60 | |
| t _{ODO} | Output Enable to Output in High-Z | | — | 40 | — | 50 | |
| t _{OH} | Output Data Hold Time | | 10 | — | 10 | — | |

Write Cycle

| SYMBOL | PARAMETER | TEST CONDITION | TC55257P-10 TC55257PL-10 | | TC55257P-12 TC55257PL-12 | | UNIT |
|------------------|--------------------------------|---------------------------------------|-----------------------------|------|-----------------------------|------|------|
| | | | MIN. | MAX. | MIN. | MAX. | |
| t _{WC} | Write Cycle Time | V _{IN} =2.4V/0.6V | 100 | — | 120 | — | ns |
| t _{WP} | Write Pulse Width | V _{IH} =2.2V | 70 | — | 80 | — | |
| t _{CW} | Chip Selection to End of Write | V _{IL} =0.8V | 90 | — | 100 | — | |
| t _{AS} | Address Set up Time | t _r , t _r ≤10ns | 0 | — | 0 | — | |
| t _{WR} | Write Recovery Time | | 0 | — | 0 | — | |
| t _{ODW} | R/W to Output High-Z | | — | 50 | — | 60 | |
| t _{OEW} | R/W to Output Low-Z | | 10 | — | 10 | — | |
| t _{DS} | Data Set Up Time | | 40 | — | 50 | — | |
| t _{DH} | Data Hold Time | | 0 | — | 0 | — | |

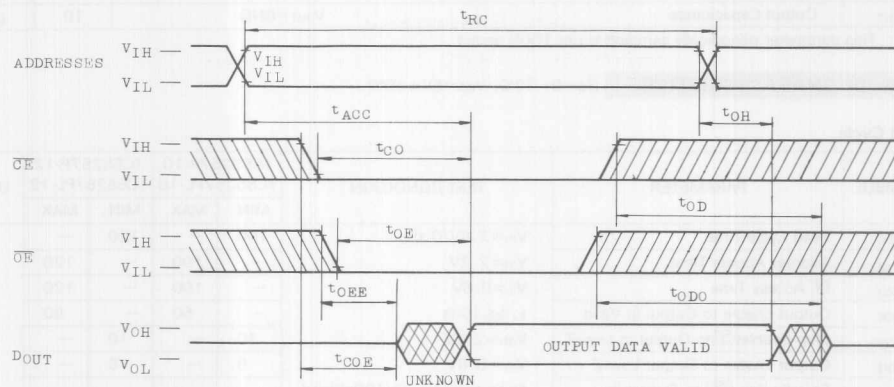
Note : Input pulse levels=V_{IN}
Timing Measurement Reference levels=V_{IH}, V_{IL}

TC55257P-10/PL-10

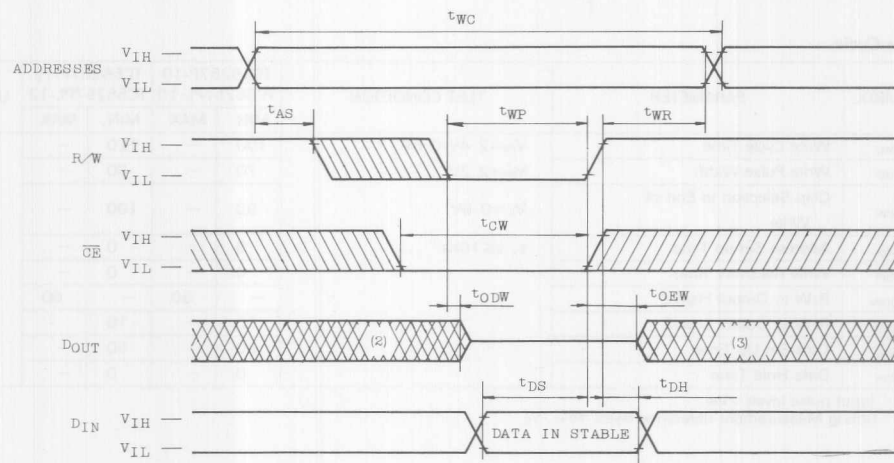
TC55257P-12/PL-12

TIMING WAVEFORMS

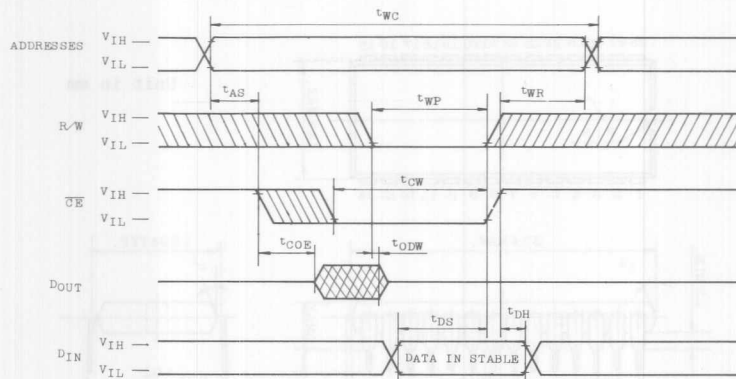
READ CYCLE (1)



WRITE CYCLE 1 (4) (R/W Controlled Write)



● WRITE CYCLE 2 (4) ($\overline{\text{CE}}$ Controlled Write)



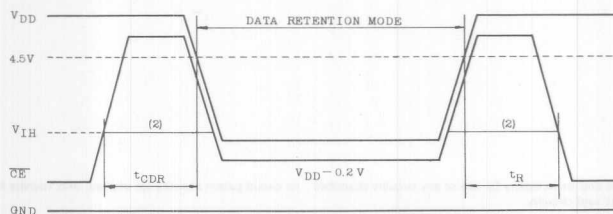
- Note:
1. R/W is High for Read cycle.
 2. Assuming that $\overline{\text{CE}}$ low transition occurs coincident with or after R/W Low transition, Outputs remain in a high impedance state.
 3. Assuming that $\overline{\text{CE}}$ High transition occurs coincident with or prior to R/W High transition, Outputs remain in a high impedance state.
 4. Assuming that $\overline{\text{CE}}$ is High for Write Cycle, Outputs are in high impedance state during this period.

DATA RETENTION CHARACTERISTICS (Ta=0~70°C)

| SYMBOL | PARAMETER | | MIN. | TYP. | MAX. | UNIT |
|------------|---|-----------|----------------------|------|------|---------------|
| V_{DH} | Data Retention Supply Voltage | | 2.0 | — | 5.5 | V |
| I_{DDS2} | Standby Supply Current | TC55257PL | $V_{DD}=3.0\text{V}$ | — | 50 | μA |
| | | | | — | 100 | |
| | | TC55257P | | | 1.0 | mA |
| t_{CDR} | Chip Deselection to Data Retention Mode | | 0 | — | — | μs |
| t_R | Recovery Time | | $t_{RC(1)}$ | — | — | |

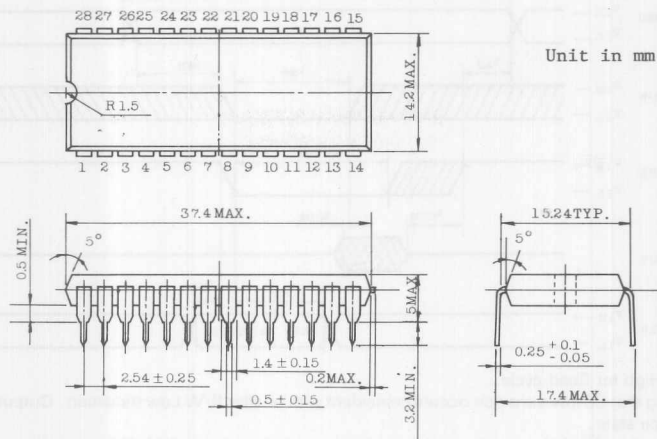
Note (1): Read cycle time.

$\overline{\text{CE}}$ Controlled Data Retention Mode



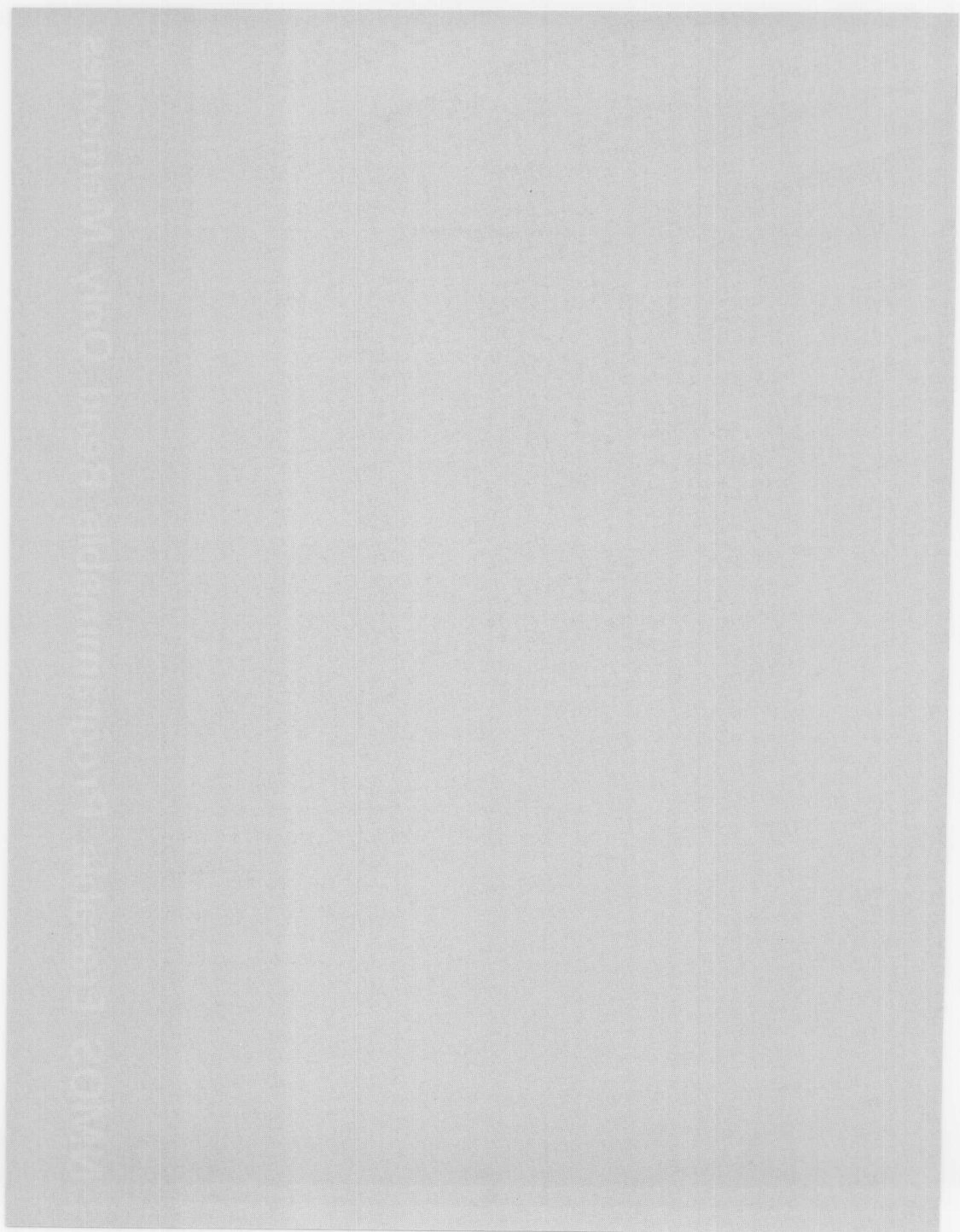
Note (2): If the V_{IH} of $\overline{\text{CE}}$ is 2.4V in operation, I_{DDS2} current flows during the period that the V_{DD} voltage is going down from 4.5V to 2.4V.

TC55257P-10/PL-10



NOTES : Each lead pitch is 2.54mm. All leads are located within 0.25mm of their true longitudinal position with respect to No. 1 and No. 28 leads.

Note : Toshiba does not assume any responsibility for use of any circuitry described ; no circuit patent licenses are implied, and Toshiba reserves the right, at any time without notice, to change said circuitry.
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TOSHIBA MOS MEMORY PRODUCTS

8,192 WORD×8 BIT UV ERASABLE AND
ELECTRICALLY PROGRAMMABLE READ ONLY MEMORY

TMM2764D-15, TMM2764D-2
TMM2764D

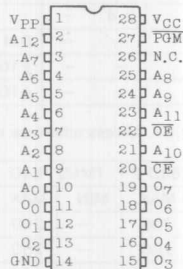
DESCRIPTION

The TMM2764D is a 8192 word×8 bit ultraviolet light erasable and electrically programmable read only memory. For read operation, the TMM2764D's access time is 150ns(TMM2764D-15)/200ns (TMM2764D-2)/250ns(TMM2764D), and the TMM2764D operates from a single 5-volt power supply and has a low power standby mode which reduces the power dissipation without increasing access time.

FEATURES

- Single 5-volt power supply
- Fast access time : TMM 2764D-15 : 150ns(Max.)
TMM2764D-2 : 200ns(Max.)
TMM2764D : 250ns(Max.)
- Power dissipation : 100mA (active current) Max.
25mA (standby current) Max.
- Low Power standby mode : \overline{CE}
- Output buffer control : \overline{OE}

PIN CONNECTION (TOP VIEW)



PIN NAMES

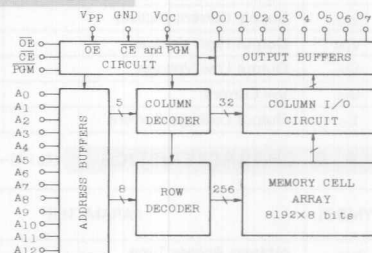
| | |
|---------------------------------|--------------------------------------|
| A ₀ ~A ₁₄ | Address Inputs |
| O ₀ ~O ₇ | Outputs (Inputs) |
| \overline{CE} | Chip Enable Input |
| \overline{OE} | Output Enable Input |
| PGM | Program Control Input |
| N. C. | No Connection |
| V _{PP} | Program Supply Voltage |
| V _{CC} | V _{CC} Supply Voltage (+5V) |
| GND | Ground |

The standby mode is achieved by applying a TTL-high level signal to the \overline{CE} input.

The maximum active current is 100mA and the maximum standby current is 25mA. For program operation, the programming is achieved by applying a 50ms active TTL low program pulse to the PGM input, and it is possible to program sequentially, individually, or at random.

- Fully static operation
- Programs with one 50ms pulse or high speed programming mode(2 types)
- Single location programming
- Three state outputs
- Inputs and outputs TTL compatible
- Pin compatible with i2764 and ROM TMM2364P

BLOCK DIAGRAM



MODE SELECTION

| MODE | PIN (27) | PGM (20) | \overline{CE} (22) | \overline{OE} (22) | V _{PP} (1) | V _{CC} (28) | O ₀ ~O ₇ (11~13, 15~19) | POWER |
|----------------|-------------|-------------|-------------------------|-------------------------|------------------------|-------------------------|--|---------|
| Read | | H | L | L | | | Data Out | |
| Output | | * | * | H | 5V | 5V | High Impedance | Active |
| Deselect | | * | * | H | | | High Impedance | |
| Standby | | * | H | * | | | High Impedance | Standby |
| Program | | L | L | * | | | Data In | |
| Program | | * | H | * | 21V | 5V | High Impedance | Active |
| Inhibit | | H | L | H | | | High Impedance | |
| Program Verify | | H | L | L | | | Data Out | |

Note * : H or L

TMM2764D-15, TMM2764D-2 TMM2764D

MAXIMUM RATINGS

| SYMBOL | ITEM | RATING | UNIT |
|---------------------|--------------------------------------|-----------|--------|
| V _{CC} | V _{CC} Power Supply Voltage | -0.6~7.0 | V |
| V _{PP} | Program Supply Voltage | -0.6~22.0 | V |
| V _{IN} | Input Voltage | -0.6~7.0 | V |
| V _{OUT} | Output Voltage | -0.6~7.0 | V |
| P _D | Power Dissipation | 1.5 | W |
| T _{SOLDER} | Soldering Temperature · Time | 260 · 10 | °C·sec |
| T _{STRG.} | Storage Temperature | -65~125 | °C |
| T _{OPR.} | Operating Temperature | 0~70 | °C |

READ OPERATION

D. C. RECOMMENDED OPERATING CONDITIONS

| SYMBOL | PARAMETER | MIN. | TYP. | MAX. | UNIT |
|-----------------|--------------------------------------|------|-----------------|----------------------|------|
| V _{IH} | Input High Voltage | 2.0 | — | V _{CC} +1.0 | V |
| V _{IL} | Input Low Voltage | -0.3 | — | 0.8 | V |
| V _{CC} | V _{CC} Power Supply Voltage | 4.75 | 5.00 | 5.25 | V |
| V _{PP} | V _{PP} Power Supply Voltage | 2.0 | V _{CC} | V _{CC} +0.6 | V |

D. C. and OPERATING CHARACTERISTICS (T_a=0~70°C, V_{CC}=5V±5%, Unless otherwise noted)

| SYMBOL | PARAMETER | TEST CONDITION | MIN. | TYP. | MAX. | UNIT |
|------------------|--------------------------|---|------|------|------|------|
| I _{LI} | Input Current | V _{IN} =0~V _{CC} | — | — | ±10 | μA |
| I _{CC1} | Supply Current (Standby) | \overline{CE} =V _{IH} | — | — | 25 | mA |
| I _{CC2} | Supply Current (Active) | \overline{CE} =V _{IL} | — | — | 100 | mA |
| V _{OH} | Output High Voltage | I _{OH} =-400μA | 2.4 | — | — | V |
| V _{OL} | Output Low Voltage | I _{OL} =2.1mA | — | — | 0.4 | V |
| I _{PP1} | V _{PP} Current | V _{PP} =0~V _{CC} +0.6 | — | — | ±10 | μA |
| I _{LO} | Output Leakage Current | V _{OUT} =0.4~V _{CC} | — | — | ±10 | μA |

A. C. CHARACTERISTICS (T_a=0~70°C, V_{CC}=5V±5%, V_{PP}=2.0V~V_{CC}+0.6V, Unless otherwise noted)

| SYMBOL | PARAMETER | TMM2764D-15 | | TMM2764D-2 | | TMM2764D | | UNIT |
|------------------|--------------------------------------|-------------|------|------------|------|----------|------|------|
| | | MIN. | MAX. | MIN. | MAX. | MIN. | MAX. | |
| t _{ACC} | Address Access Time | — | 150 | — | 200 | — | 250 | ns |
| t _{CE} | \overline{CE} to Output Valid | — | 150 | — | 200 | — | 250 | ns |
| t _{OE} | \overline{OE} to Output Valid | — | 70 | — | 70 | — | 100 | ns |
| t _{PGM} | \overline{PGM} to Output Valid | — | 70 | — | 70 | — | 100 | ns |
| t _{DF1} | \overline{CE} to Output in High-Z | 0 | 60 | 0 | 60 | 0 | 90 | ns |
| t _{DF2} | \overline{OE} to Output in High-Z | 0 | 60 | 0 | 60 | 0 | 90 | ns |
| t _{DF3} | \overline{PGM} to Output in High-Z | 0 | 60 | 0 | 60 | 0 | 90 | ns |
| t _{OH} | Output Data Hold Time | 0 | — | 0 | — | 0 | — | ns |

A. C. Test Conditions

- Output Load : 1 TTL Gate and C_L=100pF
- Input Pulse Rise and Fall Times : 10ns Max.
- Input Pulse Levels : 0.8V to 2.2V
- Timing Measurement Reference Level : Inputs 1V and 2V, Outputs 0.8V and 2.0V

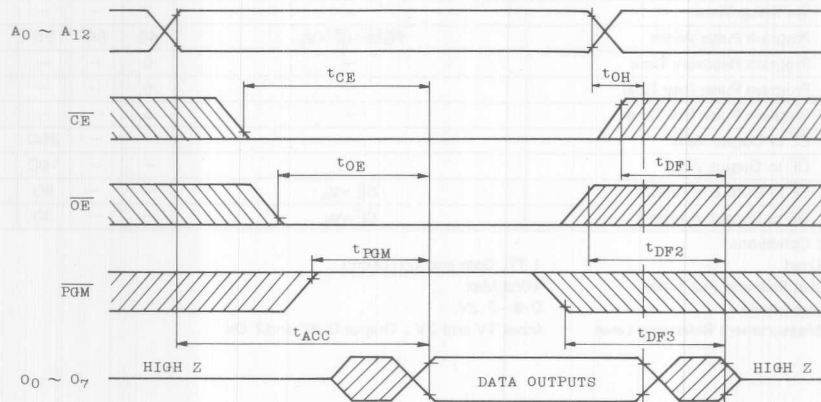
TMM2764D-15, TMM2764D-2 TMM2764D

CAPACITANCE * ($T_a = 25^\circ\text{C}$, $f = 1\text{MHz}$)

| SYMBOL | PARAMETER | TEST CONDITION | MIN. | TYP. | MAX. | UNIT |
|-----------|--------------------|-----------------------|------|------|------|------|
| C_{IN} | Input Capacitance | $V_{IN} = 0\text{V}$ | — | 4 | 6 | pF |
| C_{OUT} | Output Capacitance | $V_{OUT} = 0\text{V}$ | — | 8 | 12 | pF |

* This parameter is periodically sampled and is not 100% tested.

TIMING WAVEFORM (READ)



PROGRAM OPERATION

D. C RECOMMENDED OPERATING CONDITIONS

| SYMBOL | PARAMETER | MIN. | TYP. | MAX. | UNIT |
|----------|-------------------------------|------|------|----------------|------|
| V_{IH} | Input High Voltage | 2.0 | — | $V_{CC} + 1.0$ | V |
| V_{IL} | Input Low Voltage | -0.3 | — | 0.8 | V |
| V_{CC} | V_{CC} Power Supply Voltage | 4.75 | 5.0 | 5.25 | V |
| V_{PP} | V_{PP} Power Supply Voltage | 20.5 | 21.0 | 21.5 | V |

D. C. and OPERATING CHARACTERISTICS ($T_a = 25 \pm 5^\circ\text{C}$, $V_{CC} = 5\text{V} \pm 5\%$, $V_{PP} = 21\text{V} \pm 0.5\text{V}$)

| SYMBOL | PARAMETER | TEST CONDITION | MIN. | TYP. | MAX. | UNIT |
|-----------|-------------------------|----------------------------|------|------|----------|---------------|
| I_{LI} | Input Current | $V_{IN} = 0 \sim V_{CC}$ | — | — | ± 10 | μA |
| V_{OH} | Output High Voltage | $I_{OH} = -400\mu\text{A}$ | 2.4 | — | — | V |
| V_{OL} | Output Low Voltage | $I_{OL} = 2.1\text{mA}$ | — | — | 0.4 | V |
| I_{CC} | V_{CC} Supply Current | — | — | — | 100 | mA |
| I_{PP2} | V_{PP} Supply Current | $V_{PP} = 21.5\text{V}$ | — | — | 30 | mA |

TMM2764D-15, TMM2764D-2 TMM2764D

A. C. PROGRAMMING CHARACTERISTICS (Ta=25±5°C, Vcc=5V±5%, Vpp=21V±0.5V)

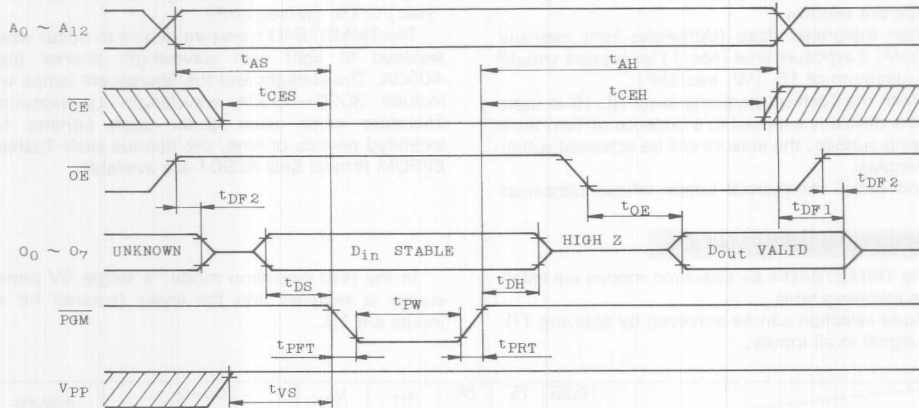
| SYMBOL | PARAMETER | TEST CONDITION | MIN. | TYP. | MAX. | UNIT |
|--------|-------------------------|----------------|------|------|------|------|
| tAS | Address Setup Time | — | 2 | — | — | μs |
| tAH | Address Hold Time | — | 2 | — | — | μs |
| tCES | CE Setup Time | — | 2 | — | — | μs |
| tCEH | CE Hold Time | — | 2 | — | — | μs |
| tDS | Data Setup Time | — | 2 | — | — | μs |
| tDH | Data Hold Time | — | 2 | — | — | μs |
| tPS | PGM Setup Time | — | 2 | — | — | μs |
| tPH | PGM Hold Time | — | 2 | — | — | μs |
| tOES | OE Setup Time | — | 2 | — | — | μs |
| tVS | Vpp Setup Time | — | 2 | — | — | μs |
| tpw | Program Pulse Width | PGM = CE = VIL | 45 | 50 | 55 | ms |
| tcp | Program Recovery Time | — | 0 | — | — | μs |
| tpRT | Program Pulse Rise Time | — | 5 | — | — | ns |
| tpFT | Program Pulse Fall Time | — | 5 | — | — | ns |
| tCE | CE to Output Valid | — | — | — | 250 | ns |
| tOE | OE to Output Valid | — | — | — | 100 | ns |
| tDF1 | CE to Output in High-Z | OE = VIL | — | — | 90 | ns |
| tDF2 | OE to Output in High-Z | CE = VIL | — | — | 90 | ns |

A. C. Test Conditions

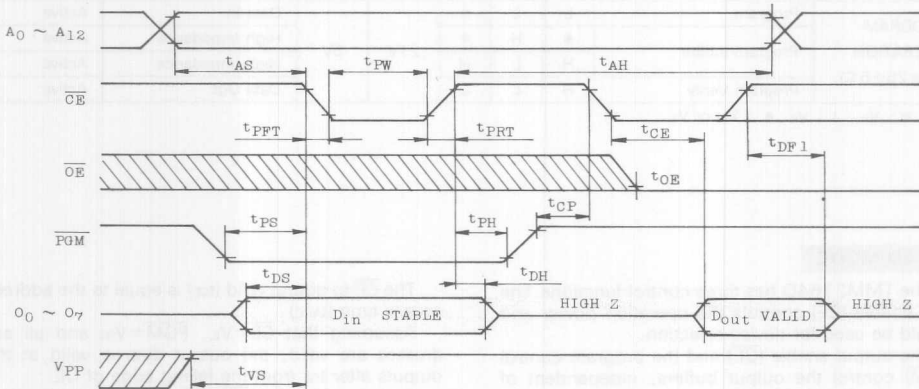
- Output Load : 1 TTL Gate and CL(100pF)
- Input Pulse Rise and Fall Times : 10ns Max.
- Input Pulse Levels : 0.8~2.2V
- Timing Measurement Reference Level : Input 1V and 2V ; Output 0.8V and 2.0V

TIMING WAVEFORMS (PROGRAM)

● PROGRAM OPERATION 1. ($V_{PP}=21V \pm 0.5V$)



● PROGRAM OPERATION 2. ($V_{PP}=21V \pm 0.5V$)



- Note :
1. V_{CC} must be applied simultaneously or before V_{PP} and cut off simultaneously or after V_{PP} .
 2. Removing the device from socket and setting the device in socket with $V_{PP}=21V$ may cause permanent damage to the device.
 3. The V_{PP} supply voltage is permitted up to 22V for program operation, so the voltage over 22V should not be applied to the V_{PP} terminal.

When the switching pulse voltage is applied to the V_{PP} terminal, the overshoot voltage of its pulse should not be exceeded 22V.

TMM2764D-15, TMM2764D-2 TMM2764D

ERASURE CHARACTERISTICS

The TMM2764D's erasure is achieved by applying shortwave ultraviolet light which has a wavelength of 2537Å (Angstroms) to the chip through the transparent window.

Then integrated dose (Ultraviolet light intensity $[W/cm^2] \times$ exposure time $[sec.]$) for erasure should be a minimum of 15 $[W \cdot sec/cm^2]$.

When the Toshiba sterilizing lamp GL-15 is used and the device is exposed at a distance of 1cm from the lamp surface, the erasure will be achieved within 60 minutes.

And using commercial lamps whose ultraviolet

light intensity is a 12000 $[\mu W/cm^2]$ will reduce the exposure time to about 20 minutes. (In this case, the integrated dose is $12000 [\mu W/cm^2] \times (20 \times 60) [sec] \cong 15 [W \cdot sec/cm^2]$.)

The TMM2764D's erasure begins to occur when exposed to light with wavelength shorter than 4000Å. The sunlight and the fluorescent lamps will include 3000~4000Å wavelength components. Therefore when used under such lighting for extended periods of time, the opaque seals-Toshiba EPROM Protect Seal AC901-are available.

OPERATION INFORMATION

The TMM2764D's six operation modes are listed in the following table.

Mode selection can be achieved by applying TTL level signal to all inputs.

In the read operation mode, a single 5V power supply is required and the levels required for all inputs are TTL.

| | | PGM (27) | CE (20) | OE (22) | V _{PP} (1) | V _{CC} (28) | O ₀ ~O ₇ (11~13, 15~19) | POWER |
|--|-----------------|-------------|------------|------------|------------------------|-------------------------|--|---------|
| READ OPERATION (T _a =0~70°C) | Read | H | L | L | 5V | 5V | Data Out | Active |
| | Output Deselect | * | * | H | | | High Impedance | Active |
| | Standby | * | H | * | | | High Impedance | Standby |
| PROGRAM OPERATION (T _a =25±5°C) | Program | L | L | * | 21V | 5V | Data In | Active |
| | Program Inhibit | * | H | * | | | High Impedance | Active |
| | Program Verify | H | L | H | | | High Impedance | Active |
| | | H | L | L | | | Data Out | Active |

Note H : V_{IL}, L : V_{IL}, * : V_{IH} or V_{IL}

READ MODE

The TMM2764D has three control functions. The chip enable (CE) controls the operation power and should be used for device selection.

The output enable (OE) and the program control (PGM) control the output buffers, independent of device selection.

Assuming that $\overline{CE} = \overline{OE} = V_{IL}$ and $\overline{PGM} = V_{IH}$, the output data is valid at the outputs after address access time from stabilizing of all addresses.

OUTPUT DESELECT MODE

Assuming that $\overline{CE} = V_{IH}$ or $\overline{OE} = V_{IH}$, the outputs will be in a high impedance state.

So two or more TMM2764D can be connected

The \overline{CE} to output valid (t_{ce}) is equal to the address access time (t_{acc}).

Assuming that $\overline{CE} = V_{IL}$, $\overline{PGM} = V_{IH}$ and all addresses are valid, the output data is valid at the outputs after t_{OE} from the falling edge of OE.

And assuming that $\overline{CE} = \overline{OE} = V_{IL}$ and all addresses are valid, the output data is valid at the outputs after t_{PGM} from the rising edge of PGM.

together on a common bus line.

When CE is decoded for device selection, all deselected devices are in low power standby mode.

TMM2764D-15, TMM2764D-2 TMM2764D

STANDBY MODE

The TMM2764D has a low power standby mode controlled by the \overline{CE} signal.

By applying a TTL high level to the \overline{CE} input, the TMM2764D is placed in the standby mode which

reduce the operating current from 100mA to 25mA, and then the outputs are in a high impedance state, independent of the \overline{OE} and the PGM inputs.

PROGRAM MODE

Initially, when received by customers, all bits of the TMM2764D are in the "1" state which is erased state.

Therefore the program operation is to introduce "0s" data into the desired bit locations by electrically programming.

The TMM2764D is set up in the program operation mode when applied the program voltage (+21V) to the V_{PP} terminal under $\overline{CE} = \overline{PGM} = \overline{OE} = V_{IH}$.

The program operation occurs during the overlap of the \overline{CE} low and the PGM low.

Then the programming is achieved by applying a

50ms (t_{pw}) active low program pulse to the \overline{CE} or the PGM input after the addresses and data are stable. This program pulse should be a single pulse with 50ms pulse width per address word, and its maximum value is 55ms.

The levels required for all inputs are TTL.

The TMM2764D can be programmed any location at anytime—either individually, sequentially, or at random.

The TMM2764D should not be programmed with D. C. signal applied to both \overline{CE} and PGM inputs.

PROGRAM VERIFY MODE

The Verify mode is to check that the desired data is correctly programmed on the programmed bits.

The verify is accomplished with \overline{OE} and \overline{CE} at V_{IL} and PGM at V_{IH} .

PROGRAM INHIBIT MODE

Under the condition that the program voltage (+21V) is applied to V_{PP} terminal, a high level \overline{CE} or \overline{PGM} input inhibits the TMM2764D from being programmed.

Programming of two or more TMM2764Ds in parallel with different data is easily accomplished.

That is, all inputs except for \overline{CE} or \overline{PGM} may be commonly connected, and a TTL low level program pulse is applied to the \overline{CE} and PGM of the desired device only and TTL high level signal is applied to the other devices.

HIGH SPEED PROGRAMMING MODE(2 TYPES)

The program time can be greatly decreased by using this high speed programming mode.

The device is set up in the high speed programming mode when the programming voltage (+21V) is applied to the V_{PP} terminal with $V_{CC} = 6V$ and $\overline{PGM} = V_{IH}$.

The programming is achieved by applying a single TTL low level 1ms pulse the PGM input after addresses and data are stable. Then the programmed data is verified by using Program Verify Mode.

If the programmed data is not correct, another

program pulse of 1ms is applied and then programmed data is verified. This should be repeated until the program operates correctly (max. A times)

After correctly programming the selected address, one additional program pulse with pulse width B times that needed for programming is applied.

When programming has been completed, the data in all addresses should be verified with $V_{CC} = V_{PP} = 5V$.

TYPE 1 : A=15, B=4

TYPE 2 : A=20, B=1

TMM2764D-15, TMM2764D-2 TMM2764D

HIGH SPEED PROGRAM OPERATION

D. C. RECOMMENDED OPERATING CONDITIONS

| SYMBOL | PARAMETER | MIN. | TYP. | MAX. | UNIT |
|----------|-------------------------------|------|------|----------------|------|
| V_{IH} | Input High Voltage | 2.0 | — | $V_{CC} + 1.0$ | V |
| V_{IL} | Input Low Voltage | -0.3 | — | 0.8 | V |
| V_{CC} | V_{CC} Power Supply Voltage | 4.75 | 5.0 | 5.25 | V |
| V_{PP} | V_{PP} Power Supply Voltage | 20.5 | 21.0 | 21.5 | V |

D. C. and OPERATING CHARACTERISTICS (Ta = 25 ± 5°C, $V_{CC} = 6V \pm 0.25V$, $V_{PP} = 21V \pm 0.5V$)

| SYMBOL | PARAMETER | TEST CONDITION | MIN. | TYP. | MAX. | UNIT |
|-----------|-------------------------|--------------------------|------|------|------|------|
| I_{LI} | Input Current | $V_{IN} = 0 \sim V_{CC}$ | — | — | ±10 | μA |
| V_{OH} | Output High Voltage | $I_{OH} = 400\mu A$ | 2.4 | — | — | V |
| V_{OL} | Output Low Voltage | $I_{OL} = 2.1mA$ | — | — | 0.4 | V |
| I_{CC} | V_{CC} Supply Current | — | — | — | 100 | mA |
| I_{PP2} | V_{PP} Supply Current | $V_{PP} = 21.5V$ | — | — | 30 | mA |

A. C. PROGRAMMING CHARACTERISTICS (Ta = 25 ± 5°C, $V_{CC} = 6V \pm 0.25V$, $V_{PP} = 21V \pm 0.5V$)

| SYMBOL | PARAMETER | TEST CONDITION | MIN. | TYP. | MAX. | UNIT |
|-----------|-------------------------------------|--------------------------|------|------|------|------|
| t_{AS} | Address Setup Time | — | 2 | — | — | μs |
| t_{AH} | Address Hold Time | — | 2 | — | — | μs |
| t_{CES} | \overline{CE} Setup Time | — | 2 | — | — | μs |
| t_{CEH} | \overline{CE} Hold Time | — | 2 | — | — | μs |
| t_{DS} | Data Setup Time | — | 2 | — | — | μs |
| t_{DH} | Data Hold Time | — | 2 | — | — | μs |
| t_{VS} | V_{PP} Setup Time | — | 2 | — | — | μs |
| t_{PW} | Program Pulse Width | — | 0.95 | 1.0 | 1.05 | ms |
| t_{OPW} | Additional Program Pulse Width | Note 1 | A | — | B | ms |
| t_{PRT} | Program Pulse Rise Time | — | 5 | — | — | ns |
| t_{PFT} | Program Pulse Fall Time | — | 5 | — | — | ns |
| t_{OE} | \overline{OE} to Output Valid | — | — | — | 100 | ns |
| t_{DF2} | \overline{OE} to Output in High Z | $\overline{CE} = V_{IL}$ | — | — | 90 | ns |

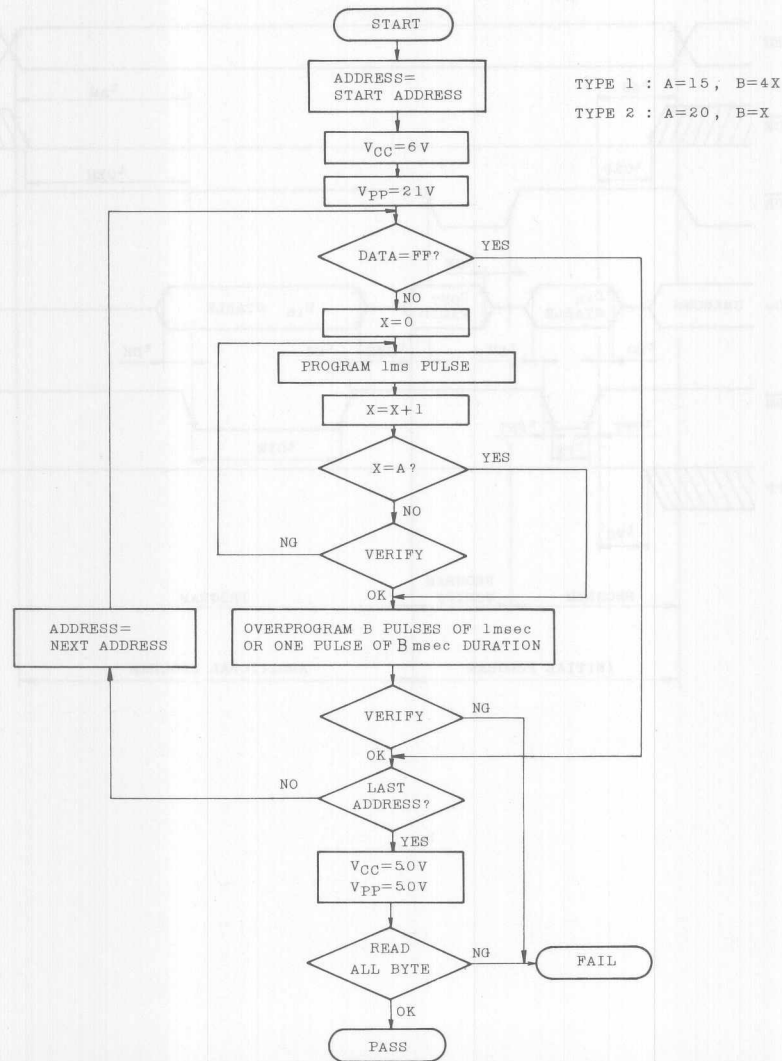
A. C. Test Conditions

- Output Load : 1 TTL Gate and $C_L(100pF)$
- Input Pulse Rise and Fall Time : 10ns Max.
- Input Pulse Levels : 0.8V and 2.2V
- Timing Measurement Reference Level : Input 1V and 2V ; Output 0.8V and 2.0V

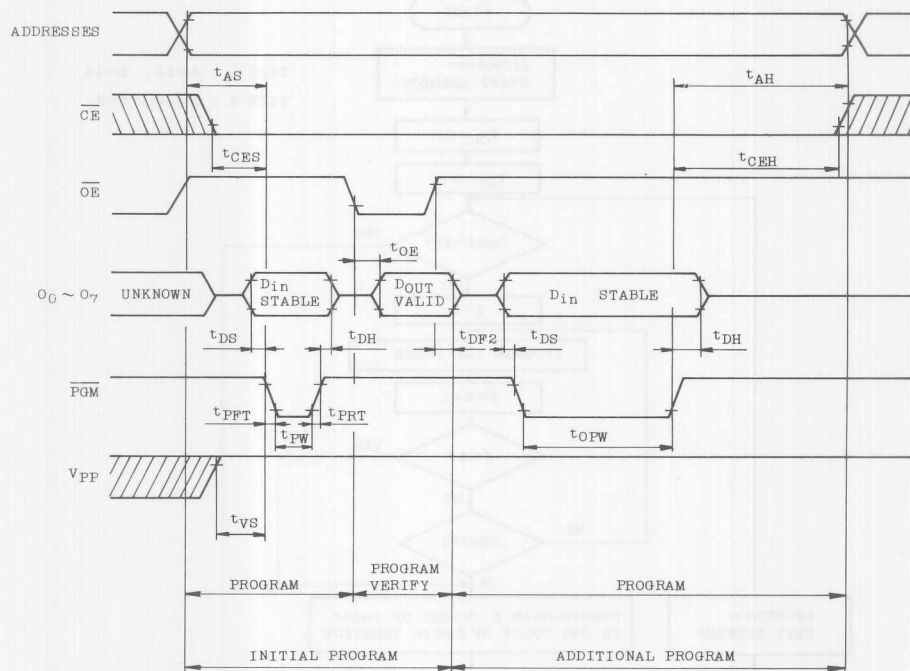
Note : 1. t_{OPW} depends on the program pulse width which is required in the initial Program.

(TYPE 1 : A=3.8, B=63 TYPE 2 : A=0.95, B=21)

HIGH SPEED PROGRAM MODE FLOW CHART



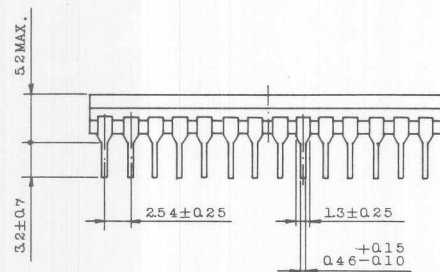
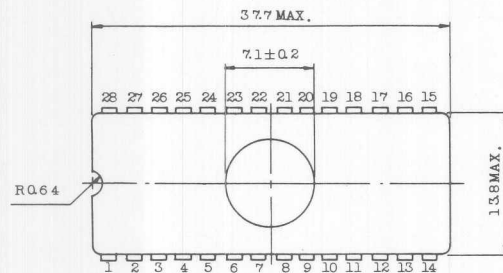
TIMING WAVEFORM (HIGH SPEED PROGRAM)



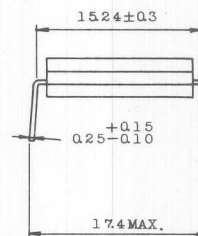
TMM2764D-15, TMM2764D-2 TMM2764D

OUTLINE DRAWINGS

Unit in mm



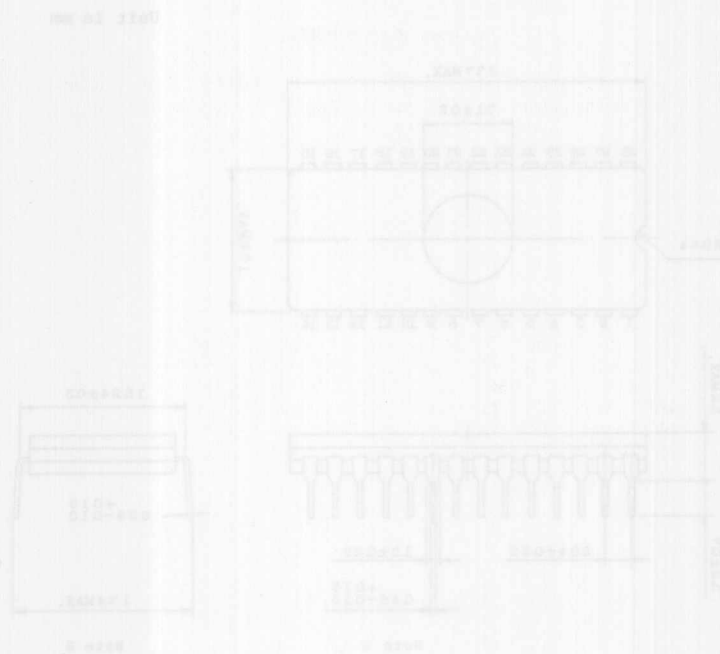
Note 1



Note 2

- Note: 1. Each lead pitch is 2.54mm. All leads are located within 0.25mm of their true longitudinal position with respect No.1 and No.28 leads.
2. This value is measured at the end of leads.
3. All dimensions are in millimeters.

TMM2764D-15, TMM2764D-2 TMM2764D



1. Each lead pitch is 0.5mm. All leads are spaced with 0.25mm of lead from the horizontal position with respect to the lead pitch.
2. The width of the lead is 0.2mm.
3. The width of the lead is 0.2mm.
4. All dimensions are in millimeters.

Note : Toshiba does not assume any responsibility for use of any circuitry described ; no circuit patent licenses are implied, and Toshiba reserves the right, at any time without notice, to change said circuitry.
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TOSHIBA MOS MEMORY PRODUCTS

8,192 WORD × 8 BIT UV ERASABLE AND ELECTRICALLY
PROGRAMMABLE READ ONLY MEMORY
N-CHANNEL SILICON STACKED GATE MOS

**TMM2764DI-15, TMM2764DI-2
TMM2764DI**

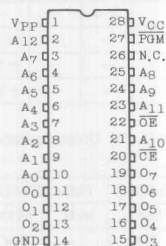
DESCRIPTION

The TMM2764DI is a 8192 word × 8 bit ultraviolet light erasable and electrically programmable read only memory. For read operation, the TMM2764DI's access time is 150ns(TMM2764DI-15)/200ns(TMM2764DI-2)/250ns(TMM2764DI), and the TMM2764DI operates from a single 5-Volt power supply and has low power standby mode which reduces the power dissipation without increasing access time.

FEATURES

- Wide operating temperature range : -40~85°C
- Single 5-volt power supply
- Fast access time: TMM2764DI-15: 150ns(Max.)
TMM2764DI-2 : 200ns(Max.)
TMM2764DI : 250ns(Max.)
- Power dissipation : 100mA (active current) Max.
25mA (standby current) Max.
- Low power standby mode : \overline{CE}
- Output buffer control : \overline{OE}

PIN CONNECTION (TOP VIEW)



PIN NAMES

| | |
|-----------------|--------------------------|
| A0~A12 | Address Inputs |
| O0~O7 | Outputs (Inputs) |
| \overline{CE} | Chip Enable Input |
| \overline{OE} | Output Enable Input |
| PGM | Program Control Input |
| N. C. | No Connection |
| VPP | Program Supply Voltage |
| VCC | VCC Supply Voltage (+5V) |
| GND | Ground |

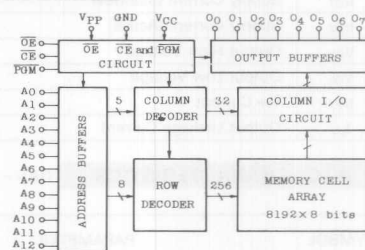
The standby mode is achieved applying a TTL-high level signal to the \overline{CE} input.

The maximum active current is 100mA and the maximum standby current is 25mA.

For program operation, the programming is achieved by applying a 50ms active TTL low program pulse to the PGM input, and it is possible to program sequentially, individually, or at random.

- Fully static operation
- Programs with one 50ms pulse or high speed programming mode(2 types)
- Single location programming
- Three state outputs
- Inputs and outputs TTL compatible
- Pin compatible with i2764 and ROM TMM2364P

BLOCK DIAGRAM



MODE SELECTION

| MODE | PIN | PGM (27) | \overline{CE} (20) | \overline{OE} (22) | VPP (1) | VCC (28) | O0~O7 (11~13, 15~19) | POWER |
|-----------------|-----|-------------|-------------------------|-------------------------|------------|-------------|-------------------------|---------|
| Read | | H | L | L | | | Data Out | Active |
| Output Deselect | | * | * | H | 5V | 5V | High Impedance | |
| Standby | | * | H | * | | | High Impedance | Standby |
| Program | | L | L | * | | | Data In | Active |
| Program Inhibit | | * | H | * | 21V | 5V | High Impedance | |
| Program Verify | | H | L | L | | | High Impedance | |
| | | | | | | | Data Out | |

Note * : H or L

TMM2764DI-15, TMM2764DI-2 TMM2764DI

MAXIMUM RATINGS

| SYMBOL | ITEM | RATING | UNIT |
|--------------|-------------------------------|------------------|-------------------------------------|
| V_{CC} | V_{CC} Power Supply Voltage | $-0.6 \sim 7.0$ | V |
| V_{PP} | Program Supply Voltage | $-0.6 \sim 22.0$ | V |
| V_{IN} | Input Voltage | $-0.6 \sim 7.0$ | V |
| V_{OUT} | Output Voltage | $-0.6 \sim 7.0$ | V |
| P_D | Power Dissipation | 1.5 | W |
| T_{SOLDER} | Soldering Temperature · Time | $260 \cdot 10$ | $^{\circ}\text{C} \cdot \text{sec}$ |
| T_{STRG} | Storage Temperature | $-65 \sim 125$ | $^{\circ}\text{C}$ |
| $T_{OPR.}$ | Operating Temperature | $-40 \sim 85$ | $^{\circ}\text{C}$ |

READ OPERATION

D. C. RECOMMENDED OPERATING CONDITIONS

| SYMBOL | PARAMETER | MIN. | TYP. | MAX. | UNIT |
|----------|-------------------------------|------|----------|----------------|------|
| V_{IH} | Input High Voltage | 2.2 | — | $V_{CC} + 1.0$ | V |
| V_{IL} | Input Low Voltage | -0.3 | — | 0.8 | V |
| V_{CC} | V_{CC} Power Supply Voltage | 4.75 | — | 5.25 | V |
| V_{PP} | V_{PP} Power Supply Voltage | 2.2 | V_{CC} | $V_{CC} + 0.6$ | V |

D. C. and OPERATING CHARACTERISTICS (Ta = -40~85°C, V_{CC} = 5V ± 5%, Unless otherwise noted)

| SYMBOL | PARAMETER | TEST CONDITION | MIN. | TYP. | MAX. | UNIT |
|-----------|--------------------------|--------------------------------|------|------|------|------|
| I_{LI} | Input Current | $V_{IN} = 0 \sim V_{CC}$ | — | — | ±10 | μA |
| I_{CC1} | Supply Current (Standby) | $\overline{CE} = V_{IH}$ | — | — | 25 | mA |
| I_{CC2} | Supply Current (Active) | $\overline{CE} = V_{IL}$ | — | — | 100 | mA |
| V_{OH} | Output High Voltage | $I_{OH} = -400 \mu\text{A}$ | 2.4 | — | — | V |
| V_{OL} | Output Low Voltage | $I_{OL} = 2.1 \text{ mA}$ | — | — | 0.4 | V |
| I_{PP1} | V_{PP} Current | $V_{PP} = 0 \sim V_{CC} + 0.6$ | — | — | ±10 | μA |
| I_{LO} | Output Leakage Current | $V_{OUT} = 0.4 \sim V_{CC}$ | — | — | ±10 | μA |

A. C. CHARACTERISTICS (Ta = -40~85°C, V_{CC} = 5V ± 5%, V_{PP} = 2.2V ~ V_{CC} + 0.6V, Unless otherwise noted)

| SYMBOL | PARAMETER | TMM2764DI-15 | | TMM2764DI-2 | | TMM2764DI | | UNIT |
|-----------|-------------------------------------|--------------|------|-------------|------|-----------|------|------|
| | | MIN. | MAX. | MIN. | MAX. | MIN. | MAX. | |
| t_{ACC} | Address Access Time | — | 150 | — | 200 | — | 250 | ns |
| t_{CE} | \overline{CE} to Output Valid | — | 150 | — | 200 | — | 250 | ns |
| t_{OE} | \overline{OE} to Output Valid | — | 70 | — | 70 | — | 100 | ns |
| t_{PGM} | PGM to Output Valid | — | 70 | — | 70 | — | 100 | ns |
| t_{DF1} | \overline{CE} to Output in High-Z | 0 | 60 | 0 | 60 | 0 | 90 | ns |
| t_{DF2} | \overline{OE} to Output in High-Z | 0 | 60 | 0 | 60 | 0 | 90 | ns |
| t_{DF3} | PGM to Output in High-Z | 0 | 60 | 0 | 60 | 0 | 60 | ns |
| t_{OH} | Output Data Hold Time | 0 | — | 0 | — | 0 | — | ns |

A. C. Test Conditions

- Output Load : 1 TTL Gate and $C_L = 100\text{pF}$
- Input Pulse Rise and Fall Times : 10ns Max.
- Input Pulse Levels : 0.6V to 2.4V
- Timing Measurement Reference Level : Inputs 1V and 2V, Outputs 0.8V and 2.0V

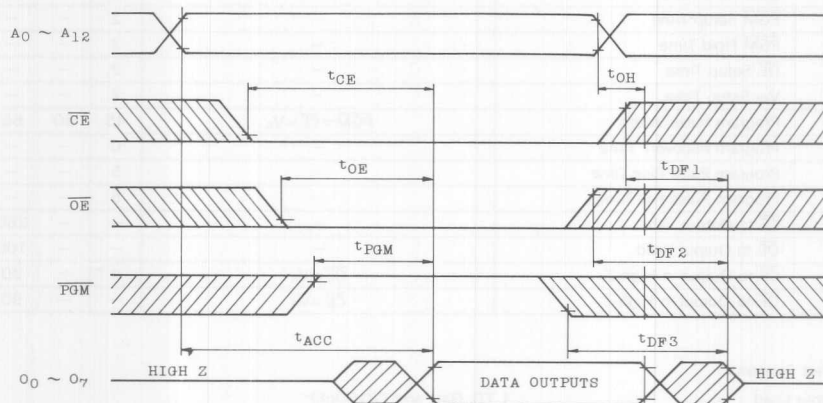
TMM2764DI-15, TMM2764DI-2 TMM2764DI

CAPACITANCE * (Ta=25°C, f=1MHz)

| SYMBOL | PARAMETER | CONDITION | MIN. | TYP. | MAX. | UNIT |
|------------------|--------------------|----------------------|------|------|------|------|
| C _{IN} | Input Capacitance | V _{IN} =0V | — | 4 | 6 | pF |
| C _{OUT} | Output Capacitance | V _{OUT} =0V | — | 8 | 12 | pF |

* This parameter is periodically sampled and is not 100% tested.

TIMING WAVEFORMS (READ)



PROGRAM OPERATION

D. C RECOMMENDED OPERATING CONDITIONS

| SYMBOL | PARAMETER | MIN. | TYP. | MAX. | UNIT |
|-----------------|--------------------------------------|------|------|----------------------|------|
| V _{IH} | Input High Voltage | 2.2 | — | V _{CC} +1.0 | V |
| V _{IL} | Input Low Voltage | -0.3 | — | 0.8 | V |
| V _{CC} | V _{CC} Power Supply Voltage | 4.75 | 5.0 | 5.25 | V |
| V _{PP} | V _{PP} Power Supply Voltage | 20.5 | 21.0 | 21.5 | V |

D. C. and OPERATING CHARACTERISTICS (Ta=25±5°C, V_{CC}=5V±5%, V_{PP}=21V±0.5V)

| SYMBOL | PARAMETER | TEST CONDITION | MIN. | TYP. | MAX. | UNIT |
|------------------|--------------------------------|------------------------------------|------|------|------|------|
| I _{LI} | Input Current | V _{IN} =0~V _{CC} | — | — | ±10 | μA |
| V _{OH} | Output High Voltage | I _{OH} =-400μA | 2.4 | — | — | V |
| V _{OL} | Output Low Voltage | I _{OL} =2.1mA | — | — | 0.4 | V |
| I _{CC} | V _{CC} Supply Current | — | — | — | 100 | mA |
| I _{PP2} | V _{PP} Supply Current | V _{PP} =21.5V | — | — | 30 | mA |

TMM2764DI-15, TMM2764DI-2 TMM2764DI

A. C. PROGRAMMING CHARACTERISTICS

(Ta = 25 ± 5°C, VCC = 5V ± 5%, VPP = 21V ± 0.5V)

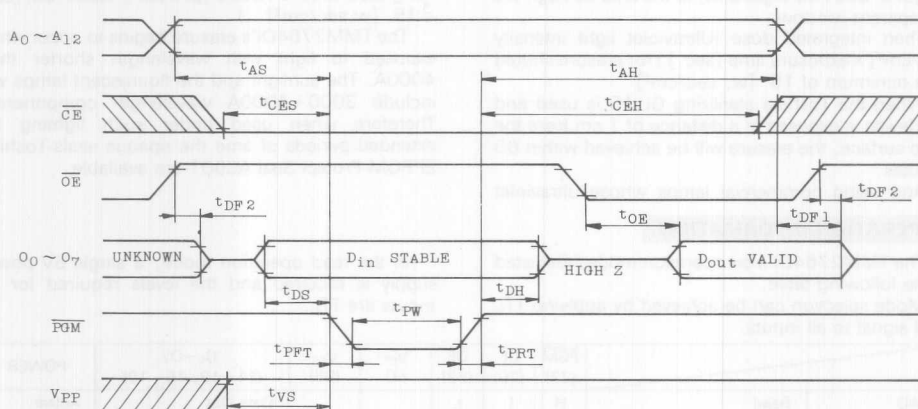
| SYMBOL | PARAMETER | TEST CONDITION | MIN. | TYP. | MAX. | UNIT |
|--------|-------------------------|----------------|------|------|------|------|
| tAS | Address Setup Time | — | 2 | — | — | μs |
| tAH | Address Hold Time | — | 2 | — | — | μs |
| tCES | CE Setup Time | — | 2 | — | — | μs |
| tCEH | CE Hold Time | — | 2 | — | — | μs |
| tDS | Data Setup Time | — | 2 | — | — | μs |
| tDH | Data Hold Time | — | 2 | — | — | μs |
| tPS | PGM Setup Time | — | 2 | — | — | μs |
| tPH | PGM Hold Time | — | 2 | — | — | μs |
| tOES | OE Setup Time | — | 2 | — | — | μs |
| tVS | VPP Setup Time | — | 2 | — | — | μs |
| tPW | Program Pulse Width | PGM = CE = VIL | 45 | 50 | 55 | ms |
| tCP | Program Recovery Time | — | 0 | — | — | μs |
| tPRT | Program Pulse Rise Time | — | 5 | — | — | ns |
| tPFT | Program Pulse Fall Time | — | 5 | — | — | ns |
| tCE | CE to Output Valid | — | — | — | 250 | ns |
| tOE | OE to Output Valid | — | — | — | 100 | ns |
| tDF1 | CE to Output in High-Z | OE = VIL | — | — | 90 | ns |
| tDF2 | OE to Output in High-Z | CE = VIL | — | — | 90 | ns |

A. C. Test Conditions

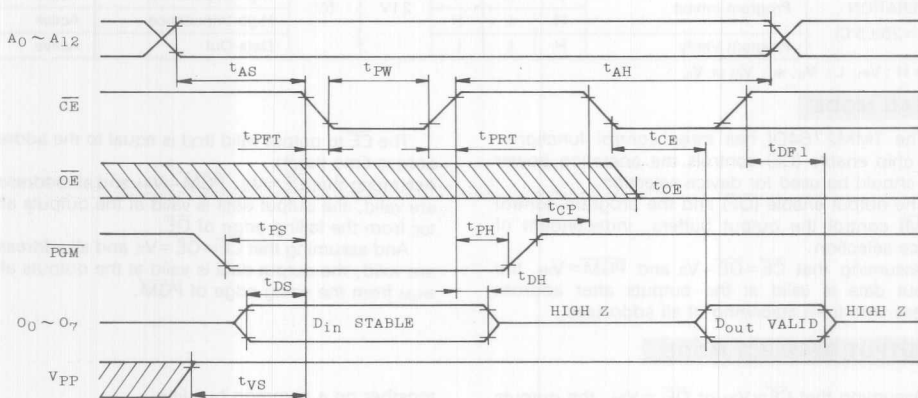
- Output Load : 1 TTL Gate and CL(100pF)
- Input Pulse Rise and Fall Time : 10ns Max.
- Input Pulse Levels : 0.6~2.4V
- Timing Measurement Reference Level : Input 1V and 2V ; Output 0.8V and 2.0V

TIMING WAVEFORMS (PROGRAM)

● PROGRAM OPERATION 1. ($V_{PP}=21V \pm 0.5V$)



● PROGRAM OPERATION 2. ($V_{PP}=21V \pm 0.5V$)



- Note:
1. V_{CC} must be applied simultaneously or before V_{PP} and cut off simultaneously or after V_{PP} .
 2. Removing the device from socket and setting the device in socket with $V_{PP}=21V$ may cause permanent damage to the device.
 3. The V_{PP} supply Voltage is permitted up to 22V for program operation, so the voltage over 22V should not be applied to the V_{PP} terminal.
When the switching pulse voltage is applied to the V_{PP} terminal, the overshoot voltage of its pulse should not be exceeded 22V.

The TMM2764DI's erasure is achieved by applying shortwave ultraviolet light which has a wavelength of 2537Å (Angstroms) to the chip through the transparent window.

Then integrated dose (Ultraviolet light intensity [W/cm^2] \times exposure time [sec.]) for erasure should be a minimum of 15 [$\text{W} \cdot \text{sec}/\text{cm}^2$]

When the Toshiba sterilizing GL-15 is used and the device is exposed at a distance of 1 cm from the lamp surface, the erasure will be achieved within 60 minutes.

And using commercial lamps whose ultraviolet

light intensity is a 12000 [$\mu\text{W}/\text{cm}^2$] will reduce the exposure time to about 20 minutes. (In this case, the integrated dose is $12000 [\mu\text{W}/\text{cm}^2] \times (20 \times 60) [\text{sec}] = 15 [\text{W} \cdot \text{sec}/\text{cm}^2]$.)

The TMM2764DI's erasure begins to occur when exposed to light with wavelength shorter than 4000Å. The sunlight and the fluorescent lamps will include 3000~4000Å wavelength components. Therefore when used under such lighting for extended periods of time, the opaque seals-Toshiba EPROM Protect Seal AC901-are available.

OPERATION INFORMATION

The TMM2764DI's six operation modes are listed in the following table.

Mode selection can be achieved by applying TTL level signal to all inputs.

In the read operation mode, a single 5V power supply is required and the levels required for all inputs are TTL.

| | | PGM (27) | CE (20) | OE (22) | V _{PP} (1) | V _{CC} (28) | O ₀ ~O ₇ (11~13, 15~19) | POWER |
|---|-----------------|-------------|------------|------------|------------------------|-------------------------|--|---------|
| READ OPERATION (T _a = -40~85°C) | Read | H | L | L | 5 V | 5V | Data Out | Active |
| | Output Deselect | * | * | H | | | High Impedance | Active |
| | Standby | * | H | * | | | High Impedance | Standby |
| PROGRAM OPERATION (T _a = 25±5°C) | Program | L | L | * | 21V | 5V | Data In | Active |
| | Program Inhibit | * | H | * | | | High Impedance | Active |
| | Program Verify | H | L | H | | | High Impedance | Active |
| | | H | L | L | | | Data Out | Active |

Note H : V_{IH}, L : V_{IL}, * : V_{IH} or V_{IL}

READ MODE

The TMM2764DI has three control functions. The chip enable (CE) controls the operation power and should be used for device selection.

The output enable (OE) and the program control (PGM) control the output buffers, independent of device selection.

Assuming that $\overline{\text{CE}} = \overline{\text{OE}} = \text{V}_{\text{IL}}$ and $\overline{\text{PGM}} = \text{V}_{\text{IH}}$, the output data is valid at the outputs after address access time from stabilizing of all addresses.

The $\overline{\text{CE}}$ to output valid (t_{CE}) is equal to the address access time (t_{ACC}).

Assuming that $\overline{\text{CE}} = \text{V}_{\text{IL}}$, $\overline{\text{PGM}} = \text{V}_{\text{IH}}$ and all addresses are valid, the output data is valid at the outputs after t_{OE} from the falling edge of $\overline{\text{OE}}$.

And assuming that $\overline{\text{CE}} = \overline{\text{OE}} = \text{V}_{\text{IL}}$ and all addresses are valid, the output data is valid at the outputs after t_{PGM} from the rising edge of $\overline{\text{PGM}}$.

OUTPUT DESELECT MODE

Assuming that $\overline{\text{CE}} = \text{V}_{\text{IH}}$ or $\overline{\text{OE}} = \text{V}_{\text{IH}}$, the outputs will be in a high impedance state.

So two or more TMM2764DI can be connected.

together on a common bus line.

When $\overline{\text{CE}}$ is decoded for device selection, all deselected devices are in low power standby mode.

STANDBY MODE

The TMM2764DI has a low power standby mode controlled by the $\overline{\text{CE}}$ signal.

By applying a TTL high level to the $\overline{\text{CE}}$ input, the TMM2764DI is placed in the standby mode which

reduce the operating current from 100mA to 25mA, and then the outputs are in a high impedance state, independent of the OE and the PGM inputs.

TMM2764DI-15, TMM2764DI-2 TMM2764DI

PROGRAM MODE

Initially, when received by customers, all bits of the TMM2764DI are in the "1" state which is erased state.

Therefore the program operation is to introduce "0s" data into the desired bit locations by electrically programming.

The TMM2764DI is set up in the program operation mode when applied the program voltage (+21V) to the V_{PP} terminal under $\overline{CE} = \overline{PGM} = \overline{OE} = V_{IH}$.

The program operation occurs during the overlap of the \overline{CE} low and the \overline{PGM} low.

Then the programming is achieved by applying a

50ms (t_{pw}) active low program pulse to the \overline{CE} or the \overline{PGM} input after the addresses and data are stable.

This program pulse should be a single pulse with 50ms pulse width per address word, and its maximum value is 55ms.

The levels required for all inputs are TTL.

The TMM 2764DI can be programmed any location at anytime — either individually, sequentially, or at random.

The TMM2764DI should not be programmed with D. C. signal applied to both \overline{CE} and \overline{PGM} inputs.

PROGRAM VERIFY MODE

The verify mode is to check that the desired data is correctly programmed on the programmed bits.

The verify is accomplished with \overline{OE} and \overline{CE} at V_{IL} and \overline{PGM} at V_{IH} .

PROGRAM INHIBIT MODE

Under the condition that the program voltage ($\pm 21V$) is applied to V_{PP} terminal, a high level \overline{CE} or \overline{PGM} input inhibits the TMM2764DI from being programmed.

Programming of two or more TMM2764DIs in parallel with different data is easily accomplished.

That is, all inputs except for \overline{CE} or \overline{PGM} may be commonly connected, and a TTL low level program pulse is applied to the \overline{CE} and \overline{PGM} of the desired device only and TTL high level signal is applied to the other devices.

HIGH SPEED PROGRAMMING MODE(2 TYPES)

The program time can be greatly decreased by using this high speed programming mode.

The device is set up in the high speed programming mode when the programming voltage (+21V) is applied to the V_{PP} terminal with $V_{CC} = 6V$ and $\overline{PGM} = V_{IH}$.

The programming is achieved by applying a single TTL low level 1ms pulse the \overline{PGM} input after addresses and data are stable. Then the programmed data is verified by using Program Verify Mode.

If the programmed data is not correct, another program pulse of 1ms is applied and then pro-

grammed data is verified. This should be repeated until the program operates correctly (max. A times)

After correctly programming the selected address, one additional program pulse with pulse width B times that needed for programming is applied.

When programming has been completed, the data in all addresses should be verified with $V_{CC} = V_{PP} = 5V$.

TYPE 1 : A=15, B=4

TYPE 2 : A=20, B=1

TMM2764DI-15, TMM2764DI-2 TMM2764DI

HIGH SPEED PROGRAM OPERATION

D. C. RECOMMENDED OPERATING CONDITIONS

| SYMBOL | PARAMETER | MIN. | TYP. | MAX. | UNIT |
|----------|-------------------------------|------|------|----------------|------|
| V_{IH} | Input High Voltage | 2.2 | — | $V_{CC} + 1.0$ | V |
| V_{IL} | Input Low Voltage | -0.3 | — | 0.8 | V |
| V_{CC} | V_{CC} Power Supply Voltage | 4.75 | 5.0 | 5.25 | V |
| V_{PP} | V_{PP} Power Supply Voltage | 20.5 | 21.0 | 21.5 | V |

D. C. and OPERATING CHARACTERISTICS (Ta=25±5°C, VCC=6V±0.25V, VPP=21V±0.5V)

| SYMBOL | PARAMETER | TEST CONDITION | MIN. | TYP. | MAX. | UNIT |
|-----------|-------------------------|--------------------|------|------|------|------|
| I_{LI} | Input Current | $V_{IN}=0-V_{CC}$ | — | — | ±10 | μA |
| V_{OH} | Output High Voltage | $I_{OH}=-400\mu A$ | 2.4 | — | — | V |
| V_{OL} | Output Low Voltage | $I_{OL}=2.1mA$ | — | — | 0.4 | V |
| I_{CC} | V_{CC} Supply Current | — | — | — | 100 | mA |
| I_{PP2} | V_{PP} Supply Current | $V_{PP}=21.5V$ | — | — | 30 | mA |

A. C. PROGRAMMING CHARACTERISTICS (Ta=25±5°C, VCC=6V±0.25V, VPP=21V±0.5V)

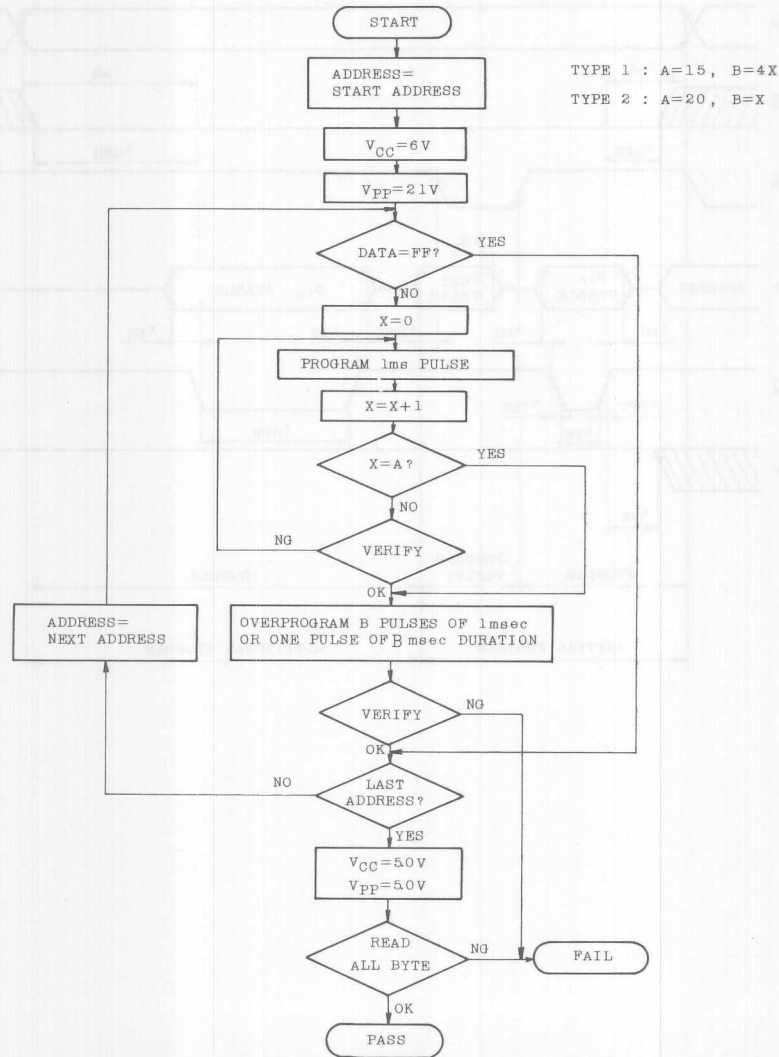
| SYMBOL | PARAMETER | TEST CONDITION | MIN. | TYP. | MAX. | UNIT |
|-----------|-------------------------------------|------------------------|------|------|------|------|
| t_{AS} | Address Setup Time | — | 2 | — | — | μs |
| t_{AH} | Address Hold Time | — | 2 | — | — | μs |
| t_{CES} | \overline{CE} Setup Time | — | 2 | — | — | μs |
| t_{CEH} | \overline{CE} Hold Time | — | 2 | — | — | μs |
| t_{DS} | Data Setup Time | — | 2 | — | — | μs |
| t_{DH} | Data Hold Time | — | 2 | — | — | μs |
| t_{VS} | V_{PP} Setup Time | — | 2 | — | — | μs |
| t_{PW} | Program Pulse Width | — | 0.95 | 1.0 | 1.05 | ms |
| t_{OPW} | Additional Program Pulse Width | Note 1 | A | — | B | ms |
| t_{PRT} | Program Pulse Rise Time | — | 5 | — | — | ns |
| t_{PFT} | Program Pulse Fall Time | — | 5 | — | — | ns |
| t_{OE} | \overline{OE} to Output Valid | — | — | — | 100 | ns |
| t_{OF2} | \overline{OE} to Output in High Z | $\overline{CE}=V_{IL}$ | — | — | 90 | ns |

A.C. Test Conditions

- Output Load : 1 TTL Gate and $C_L(100pF)$
- Input Pulse Rise and Fall Time : 10ns Max.
- Input Pulse Levels : 0.6V and 2.4V
- Timing Measurement Reference Level : Input 1V and 2V ; Output 0.8V and 2.0V

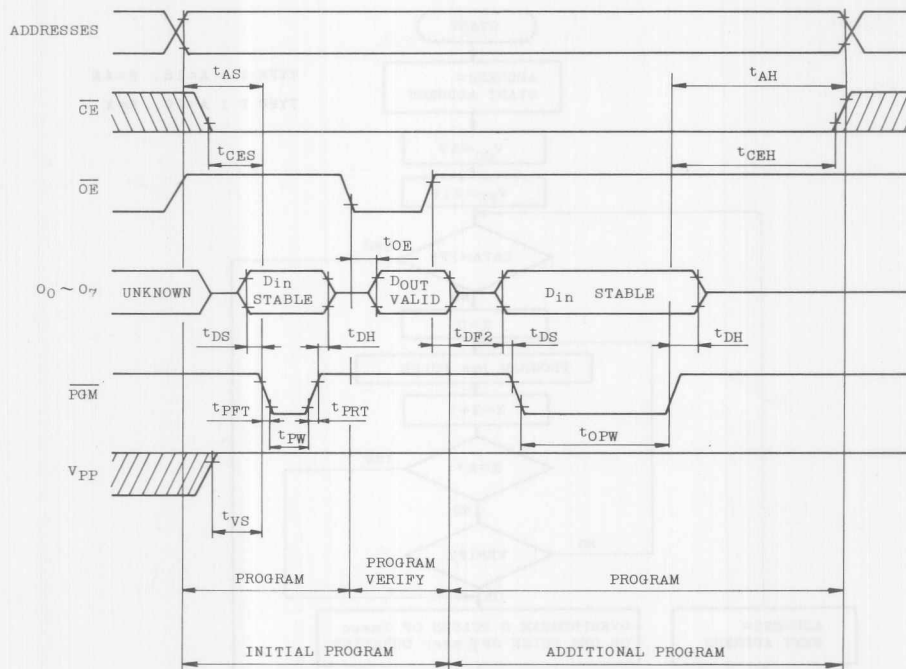
Note: 1. t_{OPW} depends on the program pulse width which is required in the initial Program.
(TYPE 1 : A=3.8, B=63, TYPE 2 : A=0.95, B=21)

HIGH SPEED PROGRAM MODE FLOW CHART



TMM2764DI-15, TMM2764DI-2 TMM2764DI

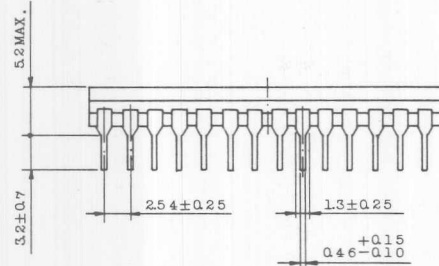
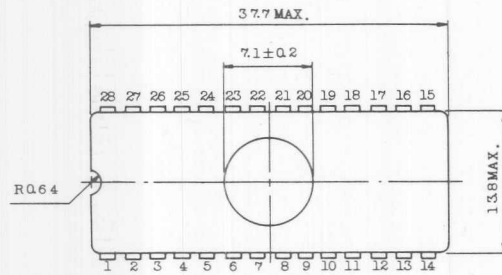
TIMING WAVEFORM (HIGH SPEED PROGRAM)



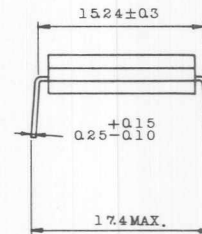
TMM2764DI-15, TMM2764DI-2 TMM2764DI

OUTLINE DRAWINGS

Unit in mm



Note 1



Note 2

- Note: 1. Each lead pitch is 2.54mm. All leads are located within 0.25mm of their true longitudinal position with respect No.1 and No.28 leads.
2. This value is measured at the end of leads.
3. All dimensions are in millimeters.

Note: Toshiba does not assume any responsibility for use of any circuitry described; no circuit patent licenses are implied, and Toshiba reserves the right, at any time without notice, to change said circuitry.

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TOSHIBA MOS MEMORY PRODUCTS

16,384 WORD × 8 BIT UV ERASABLE AND ELECTRICALLY
PROGRAMMABLE READ ONLY MEMORY
N-CHANNEL SILICON STACKED GATE MOS

**TMM27128D-15, TMM27128D-20
TMM27128D-25**

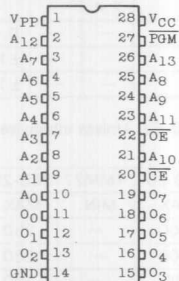
DESCRIPTION

The TMM27128D is a 16384 word × 8 bit ultra-violet light erasable and electrically programmable read only memory. For read operation, the TMM27128D's access time is 150ns/200ns/250ns, and the TMM27128D operates from a single 5-volt power supply and has a low power standby mode which reduces the power dissipation without increasing access time.

FEATURES

- Single-5Volt power supply
- Fast access time : TMM27128D-15 150ns
TMM27128D-20 200ns
TMM27128D-25 250ns
- Power dissipation : 100mA (active current) Max.
25mA (standby current) Max.
- Low power standby mode : \overline{CE}
- Output buffer control : \overline{OE}

PIN CONNECTION (TOP VIEW)



PIN NAMES

| | |
|-----------------|--------------------------|
| A0~A13 | Address Inputs |
| O0~O7 | Outputs (Inputs) |
| \overline{CE} | Chip Enable Input |
| \overline{OE} | Output Enable Input |
| PGM | Program Control Input |
| VPP | Program Supply Voltage |
| Vcc | Vcc Supply Voltage (+5V) |
| GND | Ground |

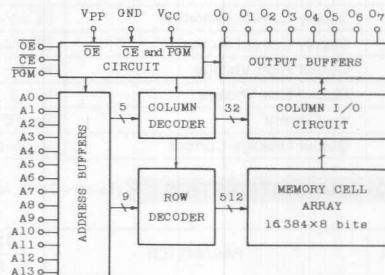
The standby mode is achieved by applying a TTL-high level signal to the \overline{CE} input.

The maximum active current is 100mA and the maximum standby current is 25mA.

For program operation, the programming is achieved by applying a 50ms active TTL low program pulse to the PGM input, and it is possible to program sequentially, in individually, or at random.

- Fully static operation
- Programs with one 50ms pulse or high speed programming mode(2 types)
- Single location programming
- Three state outputs
- Inputs and outputs TTL compatible
- Pin compatible with i27128

BLOCK DIAGRAM



MODE SELECTION

| MODE | PIN | PGM (27) | \overline{CE} (20) | \overline{OE} (22) | VPP (1) | Vcc (28) | O0~O7 (11~13, 15~19) | POWER |
|-----------------|-----|-------------|-------------------------|-------------------------|------------|-------------|-------------------------|---------|
| Read | | H | L | L | 5V | 5V | Data Out | Active |
| Output Deselect | | * | * | H | | | High Impedance | |
| Standby | | * | H | * | | | High Impedance | Standby |
| Program | | L | L | * | 21V | 5V | Data In | Active |
| Program Inhibit | | * | H | * | | | High Impedance | |
| Program Verify | | H | L | L | | | High Impedance | |
| | | H | L | L | | | Data Out | |

Note * : H or L

TMM27128D-15, TMM27128D-20

TMM27128D-25

| SYMBOL | ITEM | RATING | UNIT |
|---------------------|--------------------------------------|-----------|--------|
| V _{CC} | V _{CC} Power Supply Voltage | -0.6~7.0 | V |
| V _{PP} | Program Supply Voltage | -0.6~22.0 | V |
| V _{IN} | Input Voltage | -0.6~7.0 | V |
| V _{OUT} | Output Voltage | -0.6~7.0 | V |
| P _D | Power Dissipation | 1.5 | W |
| T _{SOLDER} | Soldering Temperature · Time | 260 · 10 | °C·sec |
| T _{STRG.} | Storage Temperature | -65~125 | °C |
| T _{OPR.} | Operating Temperature | 0~70 | °C |

READ OPERATION

D. C. RECOMMENDED OPERATING CONDITIONS

| SYMBOL | PARAMETER | MIN. | TYP. | MAX. | UNIT |
|-----------------|--------------------------------------|------|-----------------|----------------------|------|
| V _{IH} | Input High Voltage | 2.0 | — | V _{CC} +1.0 | V |
| V _{IL} | Input Low Voltage | -3.0 | — | 0.8 | V |
| V _{CC} | V _{CC} Power Supply Voltage | 4.75 | 5.00 | 5.25 | V |
| V _{PP} | V _{PP} Power Supply Voltage | 2.0 | V _{CC} | V _{CC} +0.6 | V |

D. C. and OPERATING CHARACTERISTICS (Ta=0~70°C, V_{CC}=5V±5%, Unless otherwise noted)

| SYMBOL | PARAMETER | TEST CONDITION | MIN. | TYP. | MAX. | UNIT |
|------------------|--------------------------|---|------|------|------|------|
| I _{LI} | Input Current | V _{IN} =0~V _{CC} | — | — | ±10 | μA |
| I _{CC1} | Supply Current (Standby) | \overline{CE} =V _{IH} | — | — | 25 | mA |
| I _{CC2} | Supply Current (Active) | \overline{CE} =V _{IL} | — | — | 100 | mA |
| V _{OH} | Output High Voltage | I _{OH} =-400μA | 2.4 | — | — | V |
| V _{OL} | Output Low Voltage | I _{OL} =2.1mA | — | — | 0.4 | V |
| I _{PP1} | V _{PP} Current | V _{PP} =0~V _{CC} +0.6 | — | — | ±10 | μA |
| I _{LO} | Output Leakage Current | V _{OUT} =0.4~V _{CC} | — | — | ±10 | μA |

A. C. CHARACTERISTICS (Ta=0~70°C, V_{CC}=5V±5%, V_{PP}=2.0V~V_{CC}+0.6V, Unless otherwise noted)

| SYMBOL | PARAMETER | TMM27128D-15 | | TMM27128D-20 | | TMM27128D-25 | | UNIT |
|------------------|-------------------------------------|--------------|------|--------------|------|--------------|------|------|
| | | MIN. | MAX. | MIN. | MAX. | MIN. | MAX. | |
| t _{ACC} | Address Access Time | — | 150 | — | 200 | — | 250 | ns |
| t _{CE} | \overline{CE} to Output Valid | — | 150 | — | 200 | — | 250 | ns |
| t _{OE} | \overline{OE} to Output Valid | — | 70 | — | 70 | — | 100 | ns |
| t _{PGM} | PGM to Output Valid | — | 70 | — | 70 | — | 100 | ns |
| t _{DF1} | \overline{CE} to Output in High-Z | 0 | 60 | 0 | 60 | 0 | 90 | ns |
| t _{DF2} | \overline{OE} to Output in High-Z | 0 | 60 | 0 | 60 | 0 | 90 | ns |
| t _{DF3} | PGM to Output in High-Z | 0 | 60 | 0 | 60 | 0 | 90 | ns |
| t _{OH} | Output Data Hold Time | 0 | — | 0 | — | 0 | — | ns |

A. C. Test Conditions

- Output Load : 1 TTL Gate and C_L=100pF
- Input Pulse Rise and Fall Times : 10ns Max.
- Input Pulse Levels : 0.8V to 2.2V
- Timing Measurement Reference Level : Inputs 1V and 2V, Outputs 0.8V and 2.0V

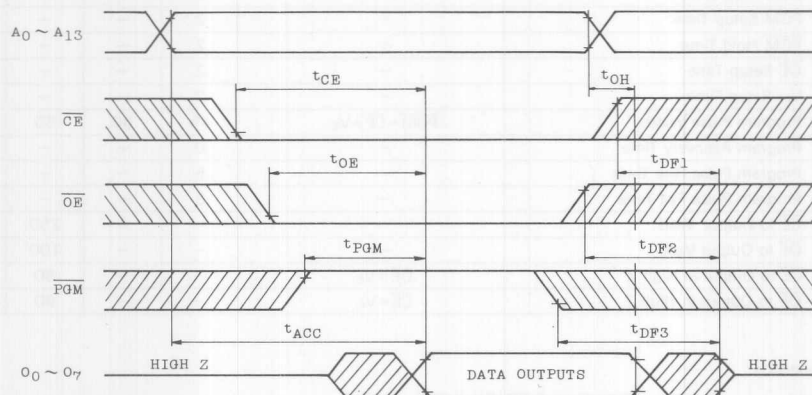
TMM27128D-15, TMM27128D-20 TMM27128D-25

CAPACITANCE * (Ta=25°C, f=1MHz)

| SYMBOL | PARAMETER | CONDITION | MIN. | TYP. | MAX. | UNIT |
|------------------|--------------------|----------------------|------|------|------|------|
| C _{IN} | Input Capacitance | V _{IN} =0V | — | 4 | 6 | pF |
| C _{OUT} | Output Capacitance | V _{OUT} =0V | — | 8 | 12 | pF |

* This parameter is periodically sampled is not 100% tested.

TIMING WAVEFORMS (READ)



PROGRAM OPERATION

D. C. RECOMMENDED OPERATING CONDITIONS

| SYMBOL | PARAMETER | MIN. | TYP. | MAX. | UNIT |
|-----------------|--------------------------------------|------|------|----------------------|------|
| V _{IH} | Input High Voltage | 2.0 | — | V _{CC} +1.0 | V |
| V _{IL} | Input Low Voltage | -0.3 | — | 0.8 | V |
| V _{CC} | V _{CC} Power Supply Voltage | 4.75 | 5.0 | 5.25 | V |
| V _{PP} | V _{PP} Power Supply Voltage | 20.5 | 21.0 | 21.5 | V |

D. C. and OPERATING CHARACTERISTICS (Ta=25±5°C, V_{CC}=5V±5%, V_{PP}=21V±0.5V)

| SYMBOL | PARAMETER | TEST CONDITION | MIN. | TYP. | MAX. | UNIT |
|------------------|--------------------------------|------------------------------------|------|------|------|------|
| I _{LI} | Input Current | V _{IN} =0~V _{CC} | — | — | ±10 | μA |
| V _{OH} | Output High Voltage | I _{OH} =-400μA | 2.4 | — | — | V |
| V _{OL} | Output Low Voltage | I _{OL} =2.1mA | — | — | 0.4 | V |
| I _{CC} | V _{CC} Supply Current | — | — | — | 100 | mA |
| I _{PP2} | V _{PP} Supply Current | V _{PP} =21.5V | — | — | 30 | mA |

TMM27128D-15, TMM27128D-20 TMM27128D-25

A. C. PROGRAMMING CHARACTERISTICS (Ta=25±5°C, Vcc=5V±5%, Vpp=21V±0.5V)

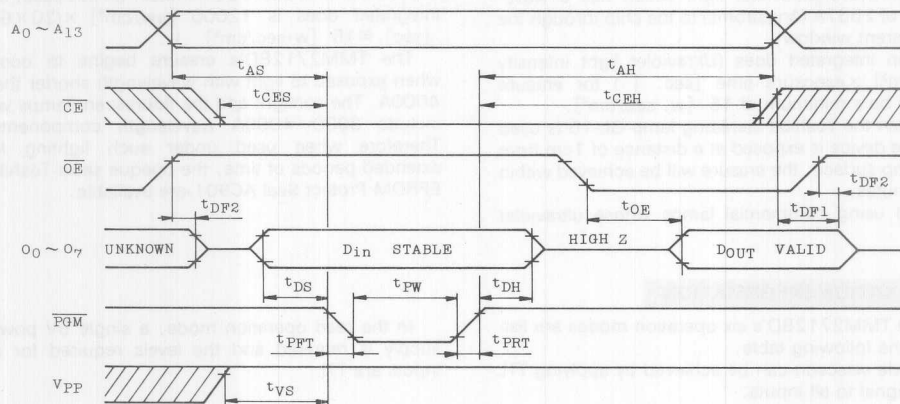
| SYMBOL | PARAMETER | TEST CONDITION | MIN. | TYP. | MAX. | UNITS |
|--------|-------------------------|----------------|------|------|------|-------|
| tAS | Address Setup Time | — | 2 | — | — | μs |
| tAH | Address Hold Time | — | 2 | — | — | μs |
| tCES | CE Setup Time | — | 2 | — | — | μs |
| tCEH | CE Hold Time | — | 2 | — | — | μs |
| tDS | Data Setup Time | — | 2 | — | — | μs |
| tDH | Data Hold Time | — | 2 | — | — | μs |
| tPS | PGM Setup Time | — | 2 | — | — | μs |
| tPH | PGM Hold Time | — | 2 | — | — | μs |
| tOES | OE Setup Time | — | 2 | — | — | μs |
| tVS | Vpp Setup Time | — | 2 | — | — | μs |
| tpW | Program Pulse Width | PGM=CE=VIL | 45 | 50 | 55 | ms |
| tCP | Program Recovery Time | — | 0 | — | — | μs |
| tpRT | Program Pulse Rise Time | — | 5 | — | — | ns |
| tpFT | Program Pulse Fall Time | — | 5 | — | — | ns |
| tCE | CE to Output Valid | — | — | — | 250 | ns |
| tOE | OE to Output Valid | — | — | — | 100 | ns |
| toF1 | CE to Output in High Z | OE=VIL | — | — | 90 | ns |
| toF2 | OE to Output in High Z | CE=VIL | — | — | 90 | ns |

A. C. Test Conditions

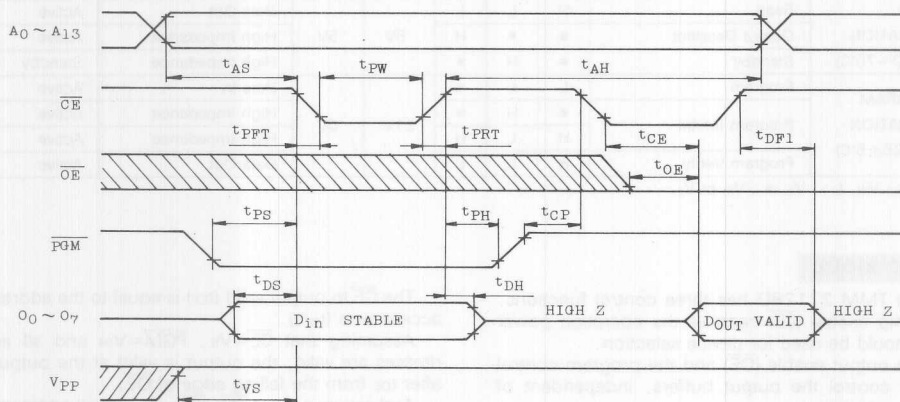
- Output Load : 1 TTL Gate and CL=100pF
- Input Pulse Rise and Fall Time : 10ns Max.
- Input Pulse Levels : 0.8V and 2.2V
- Timing Measurement Reference Level : Input 1V and 2V ; Output 0.8V and 2.0V

TIMING WAVEFORMS (PROGRAM)

● PROGRAM OPERATION 1. ($V_{PP}=21V \pm 0.5V$)



● PROGRAM OPERATION 2. ($V_{PP}=21V \pm 0.5V$)



- Note : 1. V_{CC} must be applied simultaneously or before V_{PP} and cut off simultaneously or after V_{PP} .
 2. Removing the device from socket and setting the device in socket with $V_{PP}=21V$ may cause permanent damage to the device.
 3. The V_{PP} supply voltage is permitted up to 22V for program operation, so the voltage over 22V should not be applied to the V_{PP} terminal.
 When the switching pulse voltage is applied to the V_{PP} terminal, the overshoot voltage of its pulse should not be exceeded 22V.

ERASE CHARACTERISTICS

The TMM27128D's erasure is achieved by applying shortwave ultraviolet light which has a wavelength of 2537Å (Angstroms) to the chip through the transparent window.

Then integrated does (Ultraviolet light intensity $[w/cm^2] \times \text{exposure time [sec.]}$) for erasure should be a minimum of 15 $[w. \text{ sec}/cm^2]$.

When the Toshiba sterilizing lamp GL-15 is used and the device is exposed at a distance of 1cm from the lamp surface, the erasure will be achieved within 60 minutes.

And using commercial lamps whose ultraviolet

light intensity is a 12000 $[\mu w/cm^2]$ will reduce the exposure time to about 20 minutes. (In this case, the integrated does is $12000 [\mu w/cm^2] \times (20 \times 60) [\text{sec}] \cong 15 [w \cdot \text{sec}/cm^2]$.)

The TMM27128D's erasure begins to occur when exposed to light with wavelength shorter than 4000Å. The sunlight and the fluorescent lamps will include 3000~4000Å wavelength components. Therefore when used under such lighting for extended periods of time, the opaque seals-Toshiba EPROM Protect Seal AC901-are available.

OPERATION INFORMATION

The TMM27128D's six operation modes are listed in the following table.

Mode selection can be achieved by applying TTL level signal to all inputs.

In the read operation mode, a single 5V power supply is required and the levels required for all inputs are TTL.

| | | PGM (27) | \overline{CE} (20) | \overline{OE} (22) | V_{PP} (1) | V_{CC} (28) | $O_0 \sim O_7$ (11~13, 15~19) | POWER |
|--|-----------------|-------------|-------------------------|-------------------------|-----------------|------------------|----------------------------------|---------|
| READ OPERATION ($T_a = 0 \sim 70^\circ C$) | Read | H | L | L | 5V | 5V | Data Out | Active |
| | Output Deselect | * | * | H | | | High Impedance | Active |
| | Standby | * | H | * | | | High Impedance | Standby |
| PROGRAM OPERATION ($T_a = 25 \pm 5^\circ C$) | Program | L | L | * | 21V | 5V | Data In | Active |
| | Program Inhibit | * | H | * | | | High Impedance | Active |
| | | H | L | H | | | High Impedance | Active |
| | Program Verify | H | L | L | | | Data Out | Active |

Note H : V_{IH} , L : V_{IL} , * : V_{IH} or V_{IL}

READ MODE

The TMM 27128D has three control functions. The chip enable (\overline{CE}) controls the operation power and should be used for device selection.

The output enable (\overline{OE}) and the program control (PGM) control the output buffers, independent of device selection.

Assuming that $\overline{CE} = \overline{OE} = V_{IL}$ and $\overline{PGM} = V_{IH}$, the output data is valid at the output after address access time from stabilizing of all addresses.

OUTPUT DESELECT MODE

Assuming that $\overline{CE} = V_{IH}$ or $\overline{OE} = V_{IH}$, the outputs will be in high impedance state.

So two or more TMM27128D can be connected

The \overline{CE} to output valid (t_{ce}) is equal to the address access time (t_{acc}).

Assuming that $\overline{CE} = V_{IL}$, $\overline{PGM} = V_{IH}$ and all addresses are valid, the output is valid at the outputs after t_{OE} from the falling edge of \overline{OE} .

And assuming that $\overline{CE} = \overline{OE} = V_{IL}$ and all addresses are valid, the output data is valid at the outputs after t_{PGM} from the rising edge of PGM.

together on a common bus line.

When \overline{CE} is decoded for device selection, all deselected devices are in low power standby mode.

STANDBY MODE

The TMM27128D has a low power standby mode controlled by the \overline{CE} signal.

By applying a TTL high level to the \overline{CE} input, the TMM27128D is placed in the standby mode which

reduce operating current from 100mA to 25mA, and then the outputs are in a high impedance state, independent of the \overline{OE} and the PGM inputs.

PROGRAM MODE

Initially, when received by customers, all bits of the TMM27128D are in the "1" state which is erased state.

Therefore the program operation is to introduce "0's" data into the desired bit locations by electrically programming.

The TMM27128D is set up in the program operation mode when applied the program voltage (+21V) to the V_{PP} terminal under $\overline{CE} = \overline{PGM} = \overline{OE} = V_{IH}$.

The program operation occurs during the overlap of the \overline{CE} low and the PGM low.

Then the programming is achieved by applying a

50ms (t_{PW}) active low program pulse to the \overline{CE} or the PGM input after the addresses and data stable.

This program pulse should be a single pulse with 50ms pulse width per address word, and its maximum value is 55ms.

The levels required for all inputs are TTL.

The TMM27128D can be programmed any location at anytime — either individually, sequentially, or at random.

The TMM27128D should not be programmed with D. C. signal applied to both \overline{CE} and PGM inputs.

PROGRAM VERIFY MODE

The verify mode is to check that the desired data is correctly programmed on the programmed bits.

The verify is accomplished with \overline{OE} and \overline{CE} at V_{IL} and PGM at V_{IH} .

PROGRAM INHIBIT MODE

Under the condition that the program voltage (+21V) is applied to V_{PP} terminal, a high level \overline{CE} or PGM input inhibits the TMM27128D from being programmed.

Programming of two or more TMM27128Ds in parallel with different data is easily accomplished.

That is, all inputs except for \overline{CE} or \overline{PGM} may be commonly connected, and a TTL low level program pulse is applied to the \overline{CE} and PGM of the desired device only and TTL high level signal is applied to the other devices.

HIGH SPEED PROGRAMMING MODE (2 TYPES)

The program time can be greatly decreased by using this high speed programming mode. The device is set up in the high speed programming mode when the programming voltage (+21V) is applied to the V_{PP} terminal with $V_{CC} = 6V$ and $\overline{PGM} = V_{IH}$.

The programming is achieved by applying a single TTL low level 1ms pulse the PGM input after addresses and data are stable. Then the programmed data is verified by using Program Verify Mode.

If the programmed data is not correct, another program pulse of 1ms is applied and then pro-

grammed data is verified. This should be repeated until the program operates correctly (max. A times).

After correctly programming the selected address, one additional program pulse with pulse width B times that needed for programming is applied.

When programming has been completed, the data in all addresses should be verified with $V_{CC} = V_{PP} = 5V$.

TYPE 1 : A=15, B=4

TYPE 2 : A=20, B=1

TMM27128D-15, TMM27128D-20 TMM27128D-25

HIGH SPEED RPROGRAM OPERATION

D. C. RECOMMENDED OPERATING CONDITIONS

| SYMBOL | PARAMETER | MIN. | TYP. | MAX. | UNIT |
|----------|-------------------------------|------|------|--------------|------|
| V_{IH} | Input High Voltage | 2.0 | — | $V_{CC}+1.0$ | V |
| V_{IL} | Input Low Voltage | -0.3 | — | 0.8 | V |
| V_{CC} | V_{CC} Power Supply Voltage | 4.75 | 5.0 | 5.25 | V |
| V_{PP} | V_{PP} Power Supply Voltage | 20.5 | 21.0 | 21.5 | V |

D. C. and OPERATING CHARACTERISTICS (Ta = 25 ± 5°C, VCC = 6V ± 0.25V, VPP = 21V ± 0.5V)

| SYMBOL | PARAMETER | TEST CONDITION | MIN. | TYP. | MAX. | UNIT |
|-----------|-------------------------|------------------------|------|------|------|------|
| I_{LI} | Input Current | $V_{IN}=0 \sim V_{CC}$ | — | — | ±10 | μA |
| V_{OH} | Output High Voltage | $I_{OH} = -400 \mu A$ | 2.4 | — | — | V |
| V_{OL} | Output Low Voltage | $I_{OL} = 2.1 mA$ | — | — | 0.4 | V |
| I_{CC} | V_{CC} Supply Current | — | — | — | 100 | mA |
| I_{PP2} | V_{PP} Supply Current | $V_{PP} = 21.5V$ | — | — | 30 | mA |

A. C. PROGRAMMING CHARACTERISTICS (Ta = 25 ± 5°C, VCC = 6V ± 0.25V, VPP = 21V ± 0.5V)

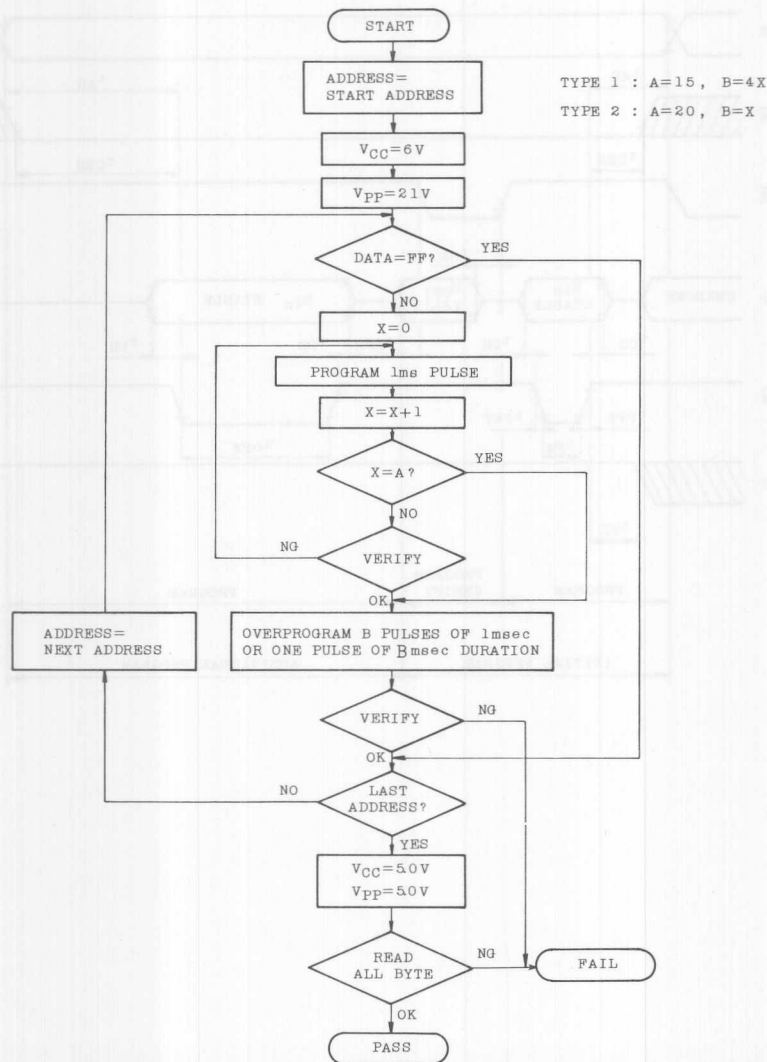
| SYMBOL | PARAMETER | TEST CONDITION | MIN. | TYP. | MAX. | UNIT |
|-----------|--------------------------------|----------------|------|------|------|------|
| t_{AS} | Address Setup Time | — | 2 | — | — | μs |
| t_{AH} | Address Hold Time | — | 2 | — | — | μs |
| t_{CES} | CE Setup Time | — | 2 | — | — | μs |
| t_{CEH} | CE Hold Time | — | 2 | — | — | μs |
| t_{DS} | Data Setup Time | — | 2 | — | — | μs |
| t_{DH} | Data Hold Time | — | 2 | — | — | μs |
| t_{VS} | V_{PP} Setup Time | — | 2 | — | — | μs |
| t_{PW} | Program Pulse Width | — | 0.95 | 1.0 | 1.05 | ms |
| t_{OPW} | Additional Program Pulse Width | Note 1 | A | — | B | ms |
| t_{PRT} | Program pulse Rise Time | — | 5 | — | — | ns |
| t_{PFT} | Program Pulse Fall Time | — | 5 | — | — | ns |
| t_{OE} | OE to Output Valid | — | — | — | 100 | ns |
| t_{DF2} | OE to Output in High-Z | CE = V_{IL} | — | — | 90 | ns |

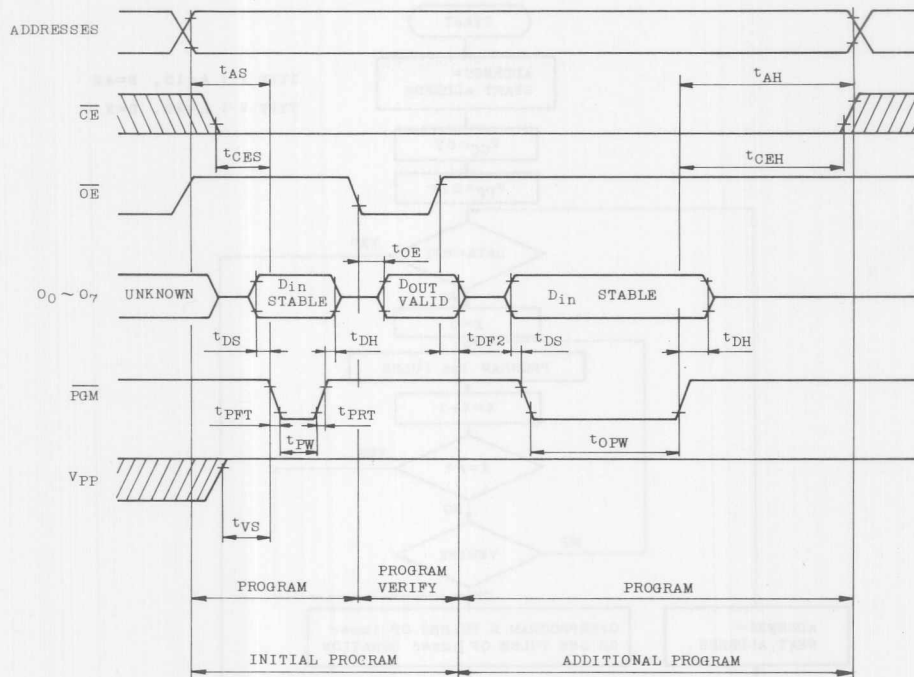
A. C. Test Conditions

- Output Load : 1 TTL Gate and $C_L(100pF)$
- Input Pulse Rise and Fall Time : 10ns Max.
- Input Pulse Levels : 0.8V and 2.2V
- Timing Measurement Reference Level : Input 1V and 2V ; Output 0.8V and 2.0V

Note : 1. t_{OPW} depends on the program pulse width which is required in the initial program.
(TYPE 1 : 3.8, B=63, TYPE 2 : A=0.95, B=21)

HIGH SPEED PROGRAM MODE FLOW CHART

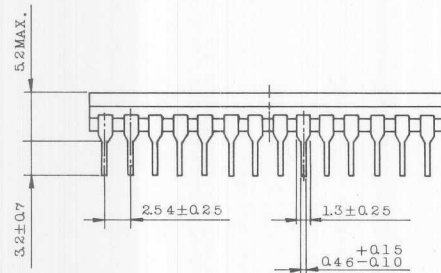
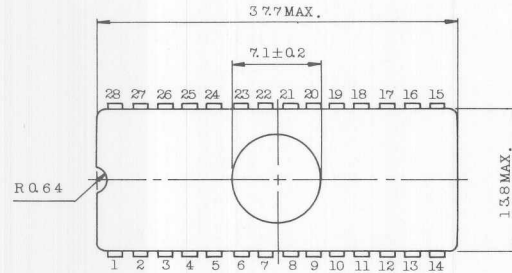




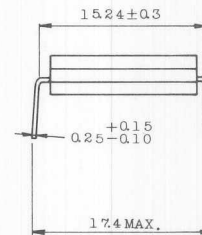
TMM27128D-15, TMM27128D-20 TMM27128D-25

OUTLINE DRAWINGS

Unit in mm



Note 1



Note 2

- Note : 1. Each lead pitch is 2.54mm. All leads are located within 0.25mm of their true longitudinal position with respect No.1 and No.28 leads.
2. This value is measured at the end of leads.
3. All dimensions are in millimeters.

TMM27128D-15, TMM27128D-20
TMM27128D-25



Note : Toshiba does not assume any responsibility for use of any circuitry described ; no circuit patent licenses are implied, and Toshiba reserves the right, at any time without notice, to change said circuitry.
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TOSHIBA MOS MEMORY PRODUCTS

16,384 WORD × 8 BIT UV ERASABLE AND
ELECTRICALLY PROGRAMMABLE READ ONLY MEMORY
N-CHANNEL SILICON STACKED GATE MOS

TMM27128DI-15, TMM27128DI-20
TMM27128DI-25

DESCRIPTION

The TMM27128DI is a 16384 word × 8 bit ultra-violet light erasable and electrically programmable read only memory.

For read operation, the TMM27128DI's access time is 150ns/200ns/250ns, and the TMM27128DI operates from a single 5-volt power supply and has a low power standby mode which reduces the power dissipation without increasing

access time. The standby mode is achieved by applying a TTL-high level signal to the CE input.

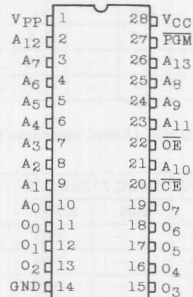
The maximum active current is 100mA and the maximum standby current is 25mA.

For Program operation, the programming is achieved by applying a 50ms active TTL low program pulse to the PGM input, and it is possible to program sequentially, individually, or at random.

FEATURES

- Wide operating temperature range : -40~85°C
- Single 5-volt power supply
- Fast access time : TMM27128DI-15 150ns
TMM27128DI-20 200ns
TMM27128DI-25 250ns
- Power dissipation : 100mA (active current) Max.
25mA (standby current) Max.
- Low power standby mode : \overline{CE}
- Output buffer control : \overline{OE}
- Fully static operation
- Programs with one 50ms pulse or high speed programming mode(2 types)
- Single location programming
- Three state outputs
- Inputs and outputs TTL compatible
- Pin compatible with i27128

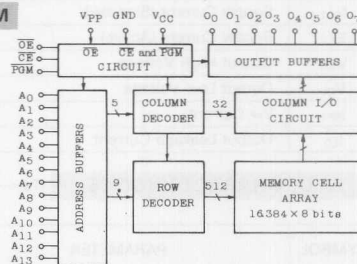
PIN CONNECTION (TOP VIEW)



PIN NAMES

| | |
|---------------------------------|--------------------------------------|
| A ₀ ~A ₁₃ | Address Inputs |
| O ₀ ~O ₇ | Outputs (Inputs) |
| \overline{CE} | Chip Enable Input |
| \overline{OE} | Output Enable Input |
| PGM | Program Control Input |
| V _{PP} | Program Supply Voltage |
| V _{CC} | V _{CC} Supply Voltage (+5V) |
| GND | Ground |

BLOCK DIAGRAM



MODE SELECTION

| MODE | PIN | PGM (27) | \overline{CE} (20) | \overline{OE} (22) | V _{PP} (1) | V _{CC} (28) | O ₀ ~O ₇ (11~13, 15~19) | POWER |
|-----------------|-----|-------------|-------------------------|-------------------------|------------------------|-------------------------|--|---------|
| Read | | H | L | L | 5V | 5V | Data Out | Active |
| Output Deselect | | * | * | H | | | High Impedance | |
| Standby | | * | H | * | | | High Impedance | Standby |
| Program | | L | L | * | | | Data In | Active |
| Program Inhibit | | * | H | * | 21V | 5V | High Impedance | |
| Program Verify | | H | L | H | | | High Impedance | |
| | | H | L | L | | | Data Out | |

Note * : H or L

TMM27128DI-15, TMM27128DI-20 TMM27128DI-25

MAXIMUM RATINGS

| SYMBOL | ITEM | RATING | UNIT |
|---------------------|--------------------------------------|-----------|--------|
| V _{CC} | V _{CC} Power Supply Voltage | -0.6~7.0 | V |
| V _{PP} | Program Supply Voltage | -0.6~22.0 | V |
| V _{IN} | Input Voltage | -0.6~7.0 | V |
| V _{OUT} | Output Voltage | -0.6~7.0 | V |
| P _D | Power Dissipation | 1.5 | W |
| T _{SOLDER} | Soldering Temperature · Time | 260 · 10 | °C·sec |
| T _{STRG.} | Storage Temperature | -65~125 | °C |
| T _{OPR.} | Operating Temperature | -40~85 | °C |

READ OPERATION

D. C. RECOMMENDED OPERATING CONDITIONS

| SYMBOL | PARAMETER | MIN. | TYP. | MAX. | UNIT |
|-----------------|--------------------------------------|------|-----------------|----------------------|------|
| V _{IH} | Input High Voltage | 2.2 | — | V _{CC} +1.0 | V |
| V _{IL} | Input Low Voltage | -0.3 | — | 0.8 | V |
| V _{CC} | V _{CC} Power Supply Voltage | 4.75 | 5.00 | 5.25 | V |
| V _{PP} | V _{PP} Power Supply Voltage | 2.2 | V _{CC} | V _{CC} +0.6 | V |

D. C. and OPERATING CHARACTERISTICS (Ta = -40~85°C, V_{CC} = 5V ± 5%, Unless otherwise noted)

| SYMBOL | PARAMETER | TEST CONDITION | MIN. | TYP. | MAX. | UNIT |
|------------------|--------------------------|---|------|------|------|------|
| I _{IJ} | Input Current | V _{IN} = 0 ~ V _{CC} | — | — | ±10 | μA |
| I _{CC1} | Supply Current (Standby) | \overline{CE} = V _{IH} | — | — | 25 | mA |
| I _{CC2} | Supply Current (Active) | \overline{CE} = V _{IL} | — | — | 100 | mA |
| V _{OH} | Output High Voltage | I _{OH} = -400 μA | 2.4 | — | — | V |
| V _{OL} | Output Low Voltage | I _{OL} = 2.1 mA | — | — | 0.4 | V |
| I _{PP1} | V _{PP} Current | V _{PP} = 0 ~ V _{CC} + 0.6 | — | — | ±10 | μA |
| I _{LO} | Output Leakage Current | V _{OUT} = 0.4 ~ V _{CC} | — | — | ±10 | μA |

A. C. CHARACTERISTICS (Ta = -40~85°C, V_{CC} = 5V ± 5%, V_{PP} = 2.2V ~ V_{CC} + 0.6V, Unless otherwise noted)

| SYMBOL | PARAMETER | TMM27128DI-15 | | TMM27128DI-20 | | TMM27128DI-25 | | UNIT |
|------------------|-------------------------------------|---------------|------|---------------|------|---------------|------|------|
| | | MIN. | MAX. | MIN. | MAX. | MIN. | MAX. | |
| t _{ACC} | Address Access Time | — | 150 | — | 200 | — | 250 | ns |
| t _{CE} | \overline{CE} to Output Valid | — | 150 | — | 200 | — | 250 | ns |
| t _{OE} | \overline{OE} to Output Valid | — | 70 | — | 70 | — | 100 | ns |
| t _{PGM} | PGM to Output Valid | — | 70 | — | 70 | — | 100 | ns |
| t _{DF1} | \overline{CE} to Output in High-Z | 0 | 60 | 0 | 60 | 0 | 90 | ns |
| t _{DF2} | \overline{OE} to Output in High-Z | 0 | 60 | 0 | 60 | 0 | 90 | ns |
| t _{DF3} | PGM to Output in High-Z | 0 | 60 | 0 | 60 | 0 | 90 | ns |
| t _{OH} | Output Data Hold Time | 0 | — | 0 | — | 0 | — | ns |

A. C. Test Conditions

- Output Load : 1 TTL Gate and C_L = 100pF
- Input Pulse Rise and Fall Times : 10ns Max.
- Input Pulse Levels : 0.6V to 2.4V
- Timing Measurement Reference Level : Inputs 1V and 2V, Outputs 0.8V and 2.0V

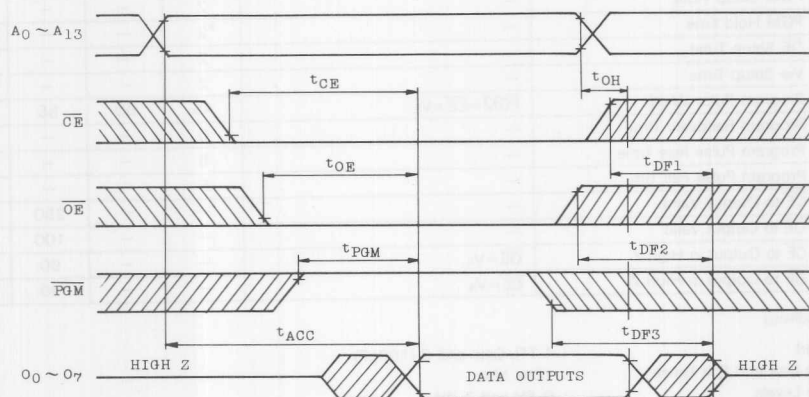
TMM27128DI-15, TMM27128DI-20 TMM27128DI-25

CAPACITANCE * (Ta=25°C, f=1MHz)

| SYMBOL | PARAMETER | TEST CONDITION | MIN. | TYP. | MAX. | UNIT |
|------------------|--------------------|----------------------|------|------|------|------|
| C _{IN} | Input Capacitance | V _{IN} =0V | — | 4 | 6 | pF |
| C _{OUT} | Output Capacitance | V _{OUT} =0V | — | 8 | 12 | pF |

* This parameter is periodically sampled is not 100% tested.

TIMING WAVEFORMS (READ)



PROGRAM OPERATION

D. C. RECOMMENDED OPERATING CONDITIONS

| SYMBOL | PARAMETER | MIN. | TYP. | MAX. | UNIT |
|-----------------|--------------------------------------|------|------|----------------------|------|
| V _{IH} | Input High Voltage | 2.2 | — | V _{CC} +1.0 | V |
| V _{IL} | Input Low Voltage | -0.3 | — | 0.8 | V |
| V _{CC} | V _{CC} Power Supply Voltage | 4.75 | 5.0 | 5.25 | V |
| V _{PP} | V _{PP} Power Supply Voltage | 20.5 | 21.0 | 21.5 | V |

D. C. and OPERATING CHARACTERISTICS (Ta=25±5°C, V_{CC}=5V±5%, V_{PP}=21V±0.5V)

| SYMBOL | PARAMETER | TEST CONDITION | MIN. | TYP. | MAX. | UNIT |
|------------------|--------------------------------|------------------------------------|------|------|------|------|
| I _I | Input Current | V _{IN} =0~V _{CC} | — | — | ±10 | μA |
| V _{OH} | Output High Voltage | I _{OH} =-400μA | 2.4 | — | — | V |
| V _{OL} | Output Low Voltage | I _{OL} =2.1mA | — | — | 0.4 | V |
| I _{CC} | V _{CC} Supply Current | — | — | — | 100 | mA |
| I _{PP2} | V _{PP} Supply Current | V _{PP} =21.5V | — | — | 30 | mA |

TMM27128DI-15, TMM27128DI-20 TMM27128DI-25

A. C. PROGRAMMING CHARACTERISTICS (Ta=25±5°C, Vcc=5V±5%, Vpp=21V±0.5V)

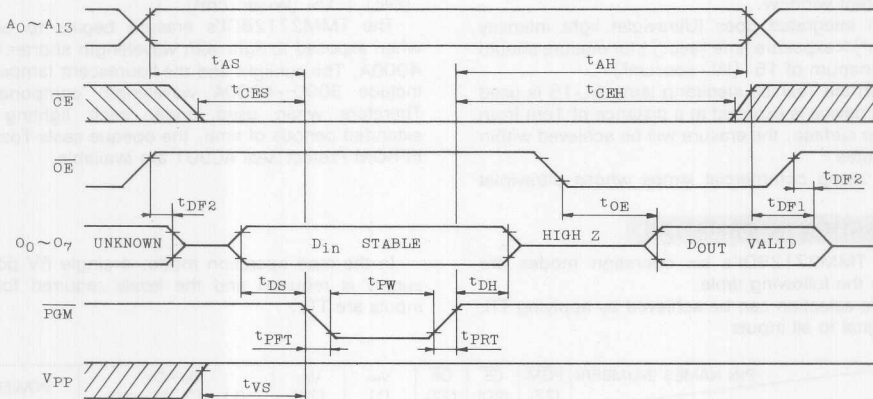
| SYMBOL | PARAMETER | TEST CONDITION | MIN. | TYP. | MAX. | UNIT |
|--------|-------------------------|----------------|------|------|------|------|
| tAS | Address Setup Time | — | 2 | — | — | μs |
| tAH | Address Hold Time | — | 2 | — | — | μs |
| tCES | CE Setup Time | — | 2 | — | — | μs |
| tCEH | CE Hold Time | — | 2 | — | — | μs |
| tDS | Data Setup Time | — | 2 | — | — | μs |
| tDH | Data Hold Time | — | 2 | — | — | μs |
| tPS | PGM Setup Time | — | 2 | — | — | μs |
| tPH | PGM Hold time | — | 2 | — | — | μs |
| tOES | OE Setup Time | — | 2 | — | — | μs |
| tVS | Vpp Setup Time | — | 2 | — | — | μs |
| tPW | Program Pulse Width | PGM=CE=VIL | 45 | 50 | 55 | ms |
| tCP | Program Recovery Time | — | 0 | — | — | μs |
| tPRT | Program Pulse Rise Time | — | 5 | — | — | ns |
| tPFT | Program Pulse Fall Time | — | 5 | — | — | ns |
| tCE | CE to Output Valid | — | — | — | 250 | ns |
| tOE | OE to Output Valid | — | — | — | 100 | ns |
| tDF1 | CE to Output in High Z | OE=VIL | — | — | 90 | ns |
| tDF2 | OE to Output in High Z | CE=VIL | — | — | 90 | ns |

A. C. Test Conditions

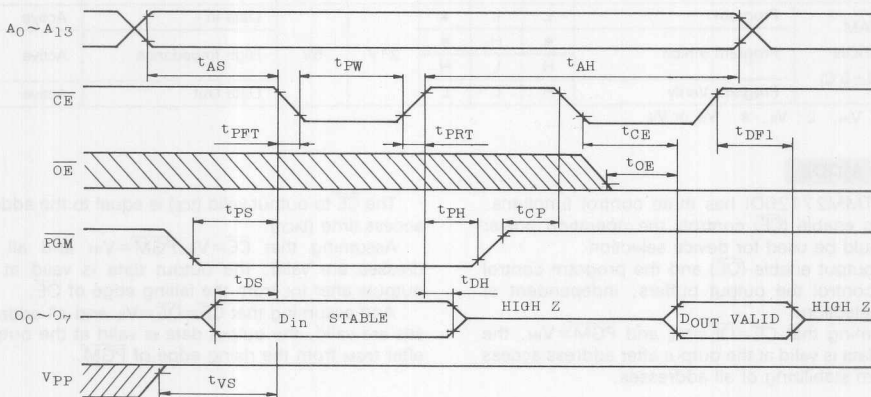
- Output Load : 1 TTL Gate and CL(100pF)
- Input Pulse Rise and Fall Times : 10ns Max.
- Input Pulse Levels : 0.6V and 2.4V
- Timing Measurement Reference Level : Input 1V and 2V ; Output 0.8V and 2.0V

TIMING WAVEFORMS (PROGRAM)

● PROGRAM OPERATION 1. ($V_{PP}=21V \pm 0.5V$)



● PROGRAM OPERATION 2. ($V_{PP}=21V \pm 0.5V$)



- Note : 1. V_{CC} must be applied simultaneously or before V_{PP} and cut off simultaneously or after V_{PP} .
2. Removing the device from socket and setting the device in socket with $V_{PP}=21V$ may cause permanent damage to the device.
3. The V_{PP} supply voltage is permitted up to 22V for program operation, so the voltage over 22V should not be applied to the V_{PP} terminal.
When the switching pulse voltage is applied to the V_{PP} terminal, the overshoot voltage of its pulse should not be exceeded 22V.

TMM27128DI-15, TMM27128DI-20 TMM27128DI-25

ERASURE CHARACTERISTICS

The TMM27128DI's erasure is achieved by applying shortwave ultraviolet light which has a wavelength of 2537Å (Angstroms) to the chip through the transparent window.

Then integrated does (Ultraviolet light intensity $[w/cm^2] \times \text{exposure time [sec.]}$) for erasure should be a minimum of 15 $[W \cdot \text{sec}/cm^2]$.

When the Toshiba sterilizing lamp GL-15 is used and the device is exposed at a distance of 1cm from the lamp surface, the erasure will be achieved within 60 minutes.

And using commercial lamps whose ultraviolet

light intensity is a 12000 $[\mu w/cm^2]$ will reduce the exposure time to about 20 minutes. (In this case, the integrated dose is $12000 [\mu W/cm^2] \times (20 \times 60) [\text{sec}] \approx 15 [w \cdot \text{sec}/cm^2]$.)

The TMM27128DI's erasure begins to occur when exposed to light with wavelength shorter than 4000Å. The sunlight and the fluorescent lamps will include 3000~4000Å wavelength components. Therefore when used under such lighting for extended periods of time, the opeque seals-Toshiba EPROM Protect Seal AC901 are available.

OPERATION INFORMATION

The TMM27128DI's six operation modes are listed in the following table.

Mode selection can be achieved by applying TTL level signal to all inputs.

In the read operation mode, a single 5V power supply is required and the levels required for all inputs are TTL.

| MODE | | PIN NAMES (NUMBER) | PGM (27) | \overline{CE} (20) | \overline{OE} (22) | V_{PP} (1) | V_{CC} (28) | $O_0 \sim O_7$ (11~13, 15~19) | POWER |
|--|-----------------|--------------------|-------------|-------------------------|-------------------------|-----------------|------------------|----------------------------------|---------|
| READ OPERATION ($T_a = -40 \sim 85^\circ\text{C}$) | Read | | H | L | L | 5 V | 5V | Data Out | Active |
| | Output Deselect | | * | * | H | | | High Impedance | Active |
| | Standby | | * | H | * | | | High Impedance | Standby |
| PROGRAM OPERATION ($T_a = 25 \pm 5^\circ\text{C}$) | Program | | L | L | * | 21V | 5V | Data In | Active |
| | Program Inhibit | | * | H | * | | | High Impedance | Active |
| | Program Verify | | H | L | L | | | Data Out | Active |

Note H : V_{IH} , L : V_{IL} , * : V_{IH} or V_{IL}

READ MODE

The TMM27128DI has three control functions. The chip enable (\overline{CE}) controls the operation power and should be used for device selection.

The output enable (\overline{OE}) and the program control (\overline{PGM}) control the output buffers, independent of device selection.

Assuming that $\overline{CE} = \overline{OE} = V_{IL}$ and $\overline{PGM} = V_{IH}$, the output data is valid at the output after address access time from stabilizing of all addresses.

The \overline{CE} to output valid (t_{CE}) is equal to the address access time (t_{ACC}).

Assuming that $\overline{CE} = V_{IL}$, $\overline{PGM} = V_{IH}$ and all addresses are valid, the output data is valid at the outputs after t_{OE} from the falling edge of \overline{OE} .

And assuming that $\overline{CE} = \overline{OE} = V_{IL}$ and all addresses are valid, the output data is valid at the outputs after t_{PGM} from the rising edge of \overline{PGM} .

OUTPUT DESELECT MODE

Assuming that $\overline{CE} = V_{IH}$ or $\overline{OE} = V_{IH}$, the outputs will be in a high impedance state.

So two or more TMM27128DI can be connected

together on a common bus line.

When \overline{CE} is decoded for device selection, all deselected devices are in low power standby mode.

TMM27128DI-15, TMM27128DI-20 TMM27128DI-25

STANDBY MODE

The TMM27128DI has a low power standby mode controlled by the \overline{CE} signal.

By applying a TTL high level to the \overline{CE} input, the TMM27128DI is placed in the standby mode which

PROGRAM MODE

Initially, when received by customers, all bits of the TMM27128DI are in the "1" state which is erased state.

Therefore the program operation is to introduce "0's" data into the desired bit locations by electrically programming.

The TMM27128DI is set up in the program operation mode when applied the program voltage (+21V) to the V_{PP} terminal under $\overline{CE} = \overline{PGM} = \overline{OE} = V_{IH}$.

The program operation occurs during the overlap of the \overline{CE} low and the \overline{PGM} low.

Then the programming is achieved by applying a

PROGRAM VERIFY MODE

The verify mode is to check that the desired data is correctly programmed on the programmed bits.

PROGRAM INHIBIT MODE

Under the condition that the program voltage (+21V) is applied to V_{PP} terminal, a high level \overline{CE} or \overline{PGM} input inhibits the TMM27128DI from being programmed.

Programming of two or more TMM27128DIs in parallel with different data is easily accomplished.

HIGH SPEED PROGRAMMING MODE (2 TYPES)

The program time can be greatly decreased by using this high speed programming mode.

The device is set up in the high speed programming mode when the programming voltage (+21V) is applied to the V_{PP} terminal with $V_{CC} = 6V$ and $\overline{PGM} = V_{IH}$.

The programming is achieved by applying a single TTL low level 1ms pulse the \overline{PGM} input after addresses and data are stable. Then the programmed data is verified by using Program Verify Mode.

If the programmed data is not correct, another program pulse of 1ms is applied and then pro-

grammed data is verified. This should be repeated until the program operates correctly (max. A times).

After correctly programming the selected address, one additional program pulse with pulse width B times that needed for programming is applied.

When programming has been completed, the data in all addresses should be verified with $V_{CC} = V_{PP} = 5V$.

50ms (t_{PW}) active low program pulse to the \overline{CE} or the \overline{PGM} input after the addresses and data are stable.

This program pulse should be a single pulse with 50ms pulse width per address word, and its maximum value is 55ms.

The levels required for all inputs are TTL.

The TMM27128DI can be programmed any location at anytime—either individually, sequentially, or at random.

The TMM27128DI should not be programmed with D.C. signal applied to both \overline{CE} and \overline{PGM} inputs.

The verify is accomplished with \overline{OE} and \overline{CE} at V_{IL} and \overline{PGM} at V_{IH} .

That is, all inputs except for \overline{CE} or \overline{PGM} may be commonly connected, and a TTL low level program pulse is applied to the \overline{CE} and \overline{PGM} of the desired device only and TTL high level signal is applied to the other devices.

grammed data is verified. This should be repeated until the program operates correctly (max. A times).

After correctly programming the selected address, one additional program pulse with pulse width B times that needed for programming is applied.

When programming has been completed, the data in all addresses should be verified with $V_{CC} = V_{PP} = 5V$.

TYPE 1 : A=15, B=4

TYPE 2 : A=20, B=1

TMM27128DI-15, TMM27128DI-20 TMM27128DI-25

HIGH SPEED PROGRAM OPERATION

D. C. RECOMMENDED OPERATING CONDITIONS

| SYMBOL | PARAMETER | MIN. | TYP. | MAX. | UNIT |
|----------|-------------------------------|------|------|----------------|------|
| V_{IH} | Input High Voltage | 2.2 | — | $V_{CC} + 1.0$ | V |
| V_{IL} | Input Low Voltage | -0.3 | — | 0.8 | V |
| V_{CC} | V_{CC} Power Supply Voltage | 4.75 | 5.0 | 5.25 | V |
| V_{PP} | V_{PP} Power Supply Voltage | 20.5 | 21.0 | 21.5 | V |

D. C. and OPERATING CHARACTERISTICS (Ta = 25 ± 5°C, VCC = 6V ± 0.25V, VPP = 21V ± 0.5V)

| SYMBOL | PARAMETER | TEST CONDITION | MIN. | TYP. | MAX. | UNIT |
|-----------|-------------------------|---------------------------|------|------|------|------|
| I_{LI} | Input Current | $V_{IN} = 0 \sim V_{CC}$ | — | — | ±10 | μA |
| V_{OH} | Output High Voltage | $I_{OH} = -400 \mu A$ | 2.4 | — | — | V |
| V_{OL} | Output Low Voltage | $I_{OL} = 2.1 \text{ mA}$ | — | — | 0.4 | V |
| I_{CC} | V_{CC} Supply Current | — | — | — | 100 | mA |
| I_{PP2} | V_{PP} Supply Current | $V_{PP} = 21.5 \text{ V}$ | — | — | 30 | mA |

A. C. PROGRAMMING CHARACTERISTICS (Ta = 25 ± 5°C, VCC = 6V ± 0.25V, VPP = 21V ± 0.5V)

| SYMBOL | PARAMETER | TEST CONDITION | MIN. | TYP. | MAX. | UNIT |
|-----------|-------------------------------------|--------------------------|------|------|------|------|
| t_{AS} | Address Setup Time | — | 2 | — | — | μs |
| t_{AH} | Address Hold Time | — | 2 | — | — | μs |
| t_{CES} | \overline{CE} Setup Time | — | 2 | — | — | μs |
| t_{CEH} | \overline{CE} Hold Time | — | 2 | — | — | μs |
| t_{DS} | Data Setup Time | — | 2 | — | — | μs |
| t_{DH} | Data Hold Time | — | 2 | — | — | μs |
| t_{VS} | V_{PP} Setup Time | — | 2 | — | — | μs |
| t_{PW} | Program Pulse Width | — | 0.95 | 1.0 | 1.05 | ms |
| t_{OPW} | Additional Program Pulse Width | Note 1 | A | — | B | ms |
| t_{PRT} | Program Pulse Rise Time | — | 5 | — | — | ns |
| t_{PFT} | Program Pulse Fall Time | — | 5 | — | — | ns |
| t_{OE} | \overline{OE} to Output Valid | — | — | — | 100 | ns |
| t_{OF2} | \overline{OE} to Output in High Z | $\overline{CE} = V_{IL}$ | — | — | 90 | ns |

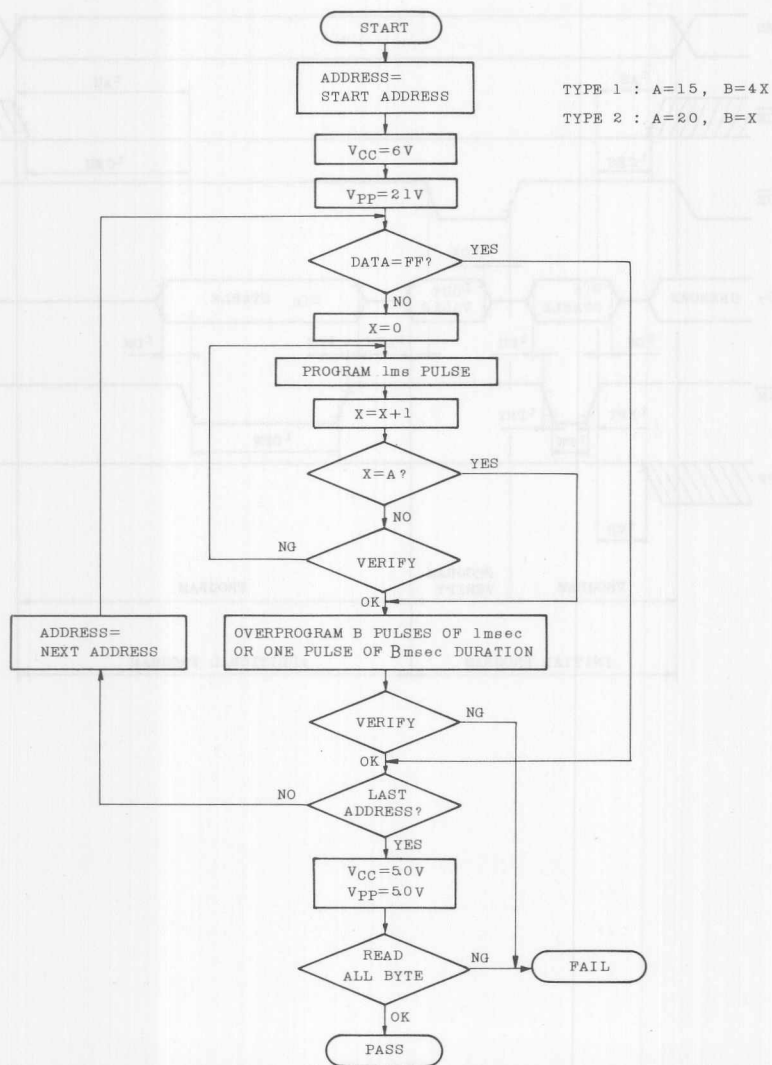
A. C. Test Conditions

- Output Load : 1 TTL Gate and $C_L(100\text{pF})$
- Input Pulse Rise and Fall Time : 10ns Max.
- Input Pulse Levels : 0.6V and 2.4V
- Timing Measurement Reference Level : Input 1V and 2V : Output 0.8V and 2.0V

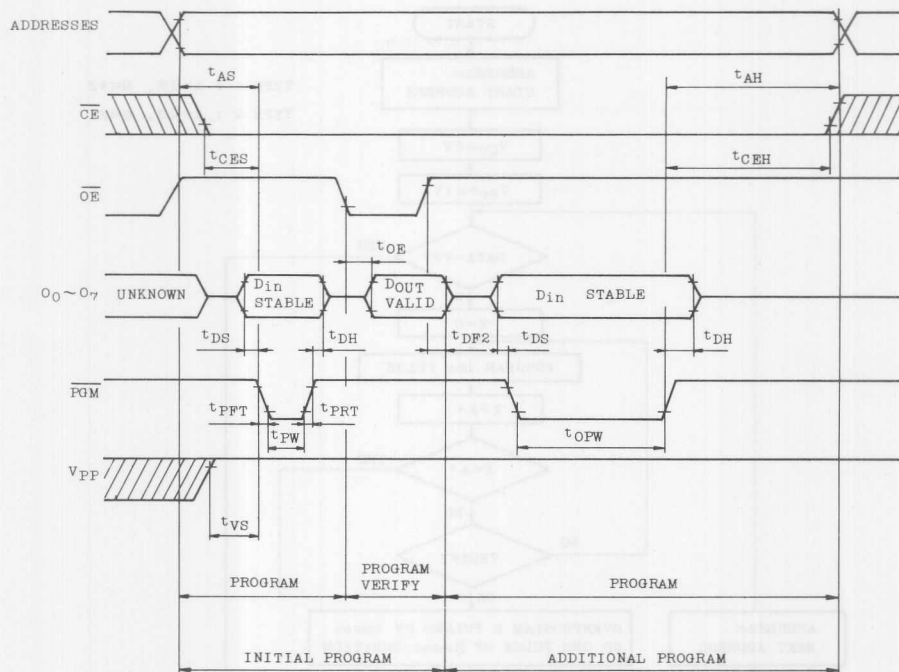
Note :

1. t_{OPW} depends on the program pulse width which is required in the initial Program.
(TYPE 1 : A=3.8, B=63, TYPE 2 : A=0.95, B=21)

HIGH SPEED PROGRAM MODE FLOW CHART

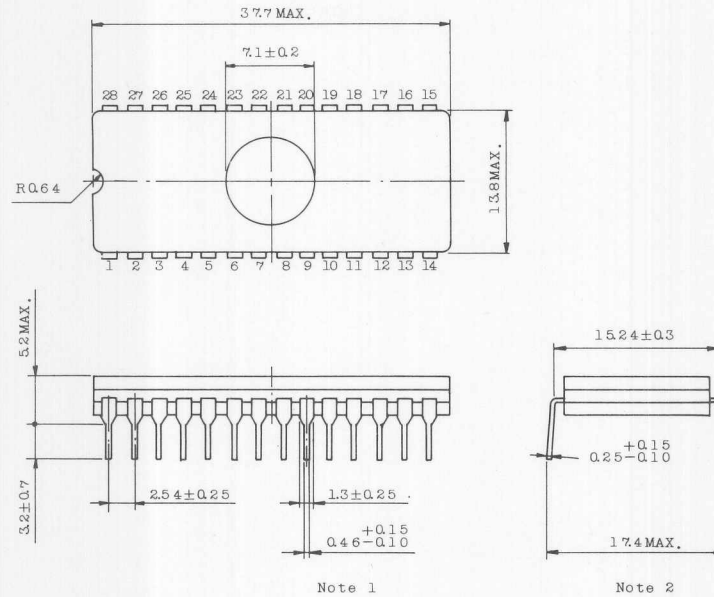


TIMING WAVEFORM (HIGH SPEED PROGRAM)



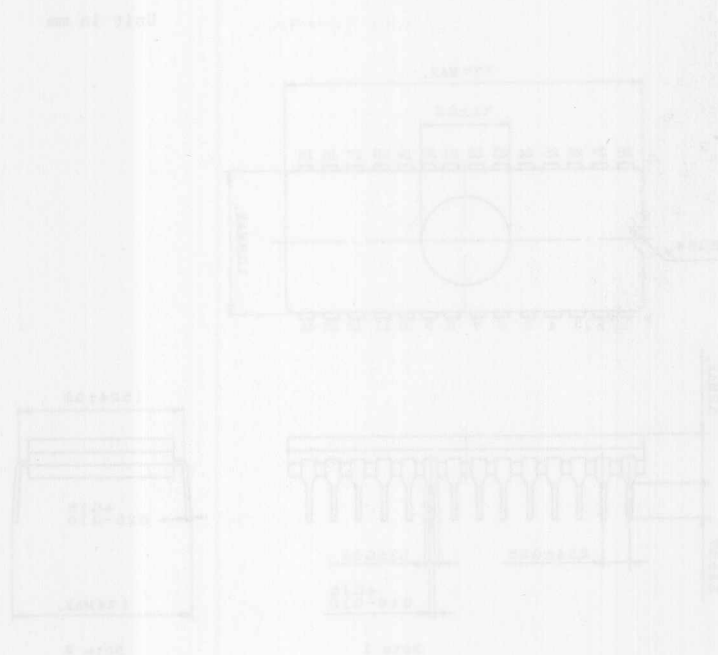
OUTLINE DRAWINGS

Unit in mm



- Note: 1. Each lead pitch is 2.54mm. All leads are located within 0.25mm of their true longitudinal position with respect No.1 and No.28 leads.
2. This value is measured at the end of leads.
3. All dimensions are in millimeters.

TMM27128DI-15, TMM27128DI-20 TMM27128DI-25



Note: 1. Each lead pitch is 0.25mm. All leads are located within 0.1mm of the topological position.
2. The value is measured in the end of the lead.
3. All dimensions are in millimeters.

Note: Toshiba does not assume any responsibility for use of any circuitry described; no circuit patent licenses are implied, and Toshiba reserves the right, at any time without notice, to change said circuitry.
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TOSHIBA MOS MEMORY PRODUCTS

32,768 WORD × 8 BIT N-MOS UV ERASABLE AND
ELECTRICALLY PROGRAMMABLE READ ONLY MEMORY
SILICON STACKED GATE MOS

TMM27256D-15 TMM27256D-20

DESCRIPTION

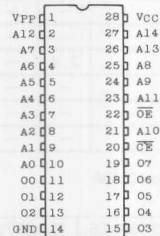
The TMM27256D is a 32,768 word×8 bit ultraviolet light erasable and electrically programmable read only memory.

For read operation, the TMM27256D's access time is 150ns/200ns, and the TMM27256D operates from a single 5-volt power supply and has low power standby mode which reduces the power dissipation without increasing access time. The standby mode is achieved by applying a TTL-high level signal to the \overline{CE} input.

FEATURES

- Fast access time TMM27256D-15 150ns
TMM27256D-20 200ns
- Low power dissipation
Active : 100mA
Standby : 25mA
- Single 5V power supply

PIN CONNECTION (TOP VIEW)



PIN NAMES

| | |
|-------------------|-------------------------------|
| $A_0 \sim A_{14}$ | Address Inputs |
| $O_0 \sim O_7$ | Outputs (Inputs) |
| \overline{CE} | Chip Enable Input |
| \overline{OE} | Output Enable Input |
| V_{PP} | Program Supply Voltage |
| V_{CC} | V_{CC} Supply Voltage (+5V) |
| GND | Ground |

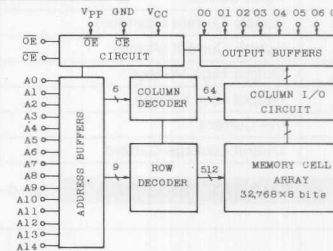
For program operation, the programming is achieved by using the high speed programming mode. Program supply voltage is 21V which is the same voltage as TMM2764D, TMM27128D and TC57256D.

The programming of TMM27256D is accomplished within about one and a half minutes (typ.).

The TMM27256D is fabricated with the N-channel silicon double layer gate MOS technology.

- Full static operation
- High speed programming mode
- Inputs and outputs TTL compatible
- Pin compatible with ROM TC53257P and TMM23256P and CMOS EPROM TC57256D.
- Standard 28 pin DIP cerdip package

BLOCK DIAGRAM



MODE SELECTION

| MODE | PIN | \overline{CE} (20) | \overline{OE} (22) | V_{PP} (1) | V_{CC} (28) | $O_0 \sim O_7$ (11~13, 15~19) | POWER |
|-----------------|-----|----------------------|----------------------|--------------|---------------|-------------------------------|--------|
| Read | | L | L | | | Data Out | Active |
| Output Deselect | | * | H | 5V | 5V | High Impedance | |
| Standby | | H | * | | | High Impedance | |
| Program | | L | H | | | Data In | Active |
| Program Inhibit | | H | * | 21V | 6V | High Impedance | |
| Program Verify | | L | L | | | Data Out | |

Note * : H or L

TMM27256D-15

TMM27256D-20

MAXIMUM RATINGS

| SYMBOL | ITEM | RATING | UNIT |
|---------------------|--------------------------------------|-----------|--------|
| V _{CC} | V _{CC} Power Supply Voltage | -0.6~7.0 | V |
| V _{PP} | Program Supply Voltage | -0.6~22.0 | V |
| V _{IN} | Input Voltage | -0.6~7.0 | V |
| V _{I/O} | Input/Output Voltage | -0.6~7.0 | V |
| P _D | Power Dissipation | 1.5 | W |
| T _{SOLDER} | Soldering Temperature • Time | 260 • 10 | °C•sec |
| T _{STG.} | Storage Temperature | -65~125 | °C |
| T _{OPR.} | Operating Temperature | 0~70 | °C |

READ OPERATION

D. C. RECOMMENDED OPERATING CONDITIONS

| SYMBOL | PARAMETER | MIN. | TYP. | MAX. | UNIT |
|-----------------|--------------------------------------|------|-----------------|----------------------|------|
| V _{IH} | Input High Voltage | 2.0 | — | V _{CC} +1.0 | V |
| V _{IL} | Input Low Voltage | -0.3 | — | 0.8 | V |
| V _{CC} | V _{CC} Power Supply Voltage | 4.75 | 5.00 | 5.25 | V |
| V _{PP} | V _{PP} Power Supply Voltage | 2.0 | V _{CC} | V _{CC} +0.6 | V |

D. C. and OPERATING CHARACTERISTICS (Ta=0~70°C, V_{CC}=5V±5%)

| SYMBOL | PARAMETER | TEST CONDITION | MIN. | TYP. | MAX. | UNIT |
|------------------|--------------------------|---|------|------|------|------|
| I _{LI} | Input Current | V _{IN} =0~V _{CC} | — | — | ±10 | μA |
| I _{CC1} | Supply Current (Standby) | $\overline{CE}=V_{IH}$ | — | — | 25 | mA |
| I _{CC2} | Supply Current (Active) | $\overline{CE}=V_{IL}$ | — | — | 100 | mA |
| V _{OH} | Output High Voltage | I _{OH} =-400μA | 2.4 | — | — | V |
| V _{OL} | Output Low Voltage | I _{OL} =2.1mA | — | — | 0.4 | V |
| I _{PP1} | V _{PP} Current | V _{PP} =0~V _{CC} +0.6 | — | — | ±10 | μA |
| I _{LO} | Output Leakage Current | V _{OUT} =0.4~V _{CC} | — | — | ±10 | μA |

A. C. CHARACTERISTICS (Ta=0~70°C, V_{CC}=5V±5%, V_{PP}=2.0V~V_{CC}+0.6V)

| SYMBOL | PARAMETER | TEST CONDITION | TMM27256D-15 | | TMM27256D-20 | | UNIT |
|------------------|-------------------------------------|--------------------------------------|--------------|------|--------------|------|------|
| | | | MIN. | MAX. | MIN. | MAX. | |
| t _{ACC} | Address Access Time | $\overline{CE}=\overline{OE}=V_{IL}$ | — | 150 | — | 200 | ns |
| t _{CE} | \overline{CE} to Output Valid | $\overline{OE}=V_{IL}$ | — | 150 | — | 200 | ns |
| t _{OE} | \overline{OE} to Output Valid | $\overline{CE}=V_{IL}$ | — | 70 | — | 70 | ns |
| t _{DF1} | \overline{CE} to Output in High-Z | $\overline{OE}=V_{IL}$ | 0 | 60 | 0 | 60 | ns |
| t _{DF2} | \overline{OE} to Output in High-Z | $\overline{CE}=V_{IL}$ | 0 | 60 | 0 | 60 | ns |
| t _{OH} | Output Data Hold Time | $\overline{CE}=\overline{OE}=V_{IL}$ | 0 | — | 0 | — | ns |

A. C. Test Conditions

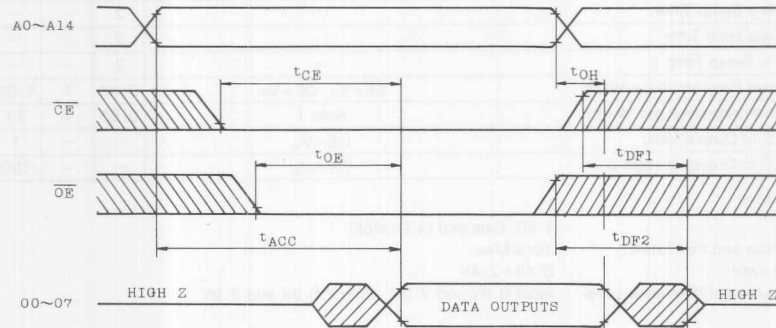
- Output Load : 1 TTL Gate and C_L=100pF
- Input Pulse Rise and Fall Times : 10ns Max.
- Input Pulse Levels : 0.45V~2.4V
- Timing Measurement Reference Level : Inputs 0.8V and 2.0V, Outputs 0.8V and 2.0V

CAPACITANCE * (Ta=25°C, f=1MHz)

| SYMBOL | PARAMETER | TEST CONDITION | MIN. | TYP. | MAX. | UNIT |
|------------------|--------------------|----------------------|------|------|------|------|
| C _{IN} | Input Capacitance | V _{IN} =0V | — | 4 | 6 | pF |
| C _{OUT} | Output Capacitance | V _{OUT} =0V | — | 8 | 12 | pF |

* This paramater is periodically sampled and is not 100% tested.

TIMING WAVEFORMS (READ)



PROGRAM OPERATION

D. C. RECOMMENDED OPERATING CONDITIONS

| SYMBOL | PARAMETER | MIN. | TYP. | MAX. | UNIT |
|-----------------|--------------------------------------|------|------|----------------------|------|
| V _{IH} | Input High Voltage | 2.0 | — | V _{CC} +1.0 | V |
| V _{IL} | Input Low Voltage | -0.3 | — | 0.8 | V |
| V _{CC} | V _{CC} Power Supply Voltage | 5.75 | 6.0 | 6.25 | V |
| V _{PP} | V _{PP} Power Supply Voltage | 20.5 | 21.0 | 21.5 | V |

D. C. and OPERATING CHARACTERISTICS (Ta=25±5°C, V_{CC}=6V±0.25V, V_{PP}=21V±0.5V)

| SYMBOL | PARAMETER | TEST CONDITION | MIN. | TYP. | MAX. | UNIT |
|------------------|--------------------------------|------------------------------------|------|------|------|------|
| I _{LI} | Input Current | V _{IN} =0~V _{CC} | — | — | ±10 | μA |
| V _{OH} | Output High Voltage | I _{OH} =-400μA | 2.4 | — | — | V |
| V _{OL} | Output Low Voltage | I _{OL} =2.1mA | — | — | 0.4 | V |
| I _{CC} | V _{CC} Supply Current | — | — | — | 100 | mA |
| I _{PP2} | V _{PP} Supply Current | V _{PP} =21.5V | — | — | 30 | mA |

TMM27256D-15

TMM27256D-20

A. C. PROGRAMMING CHARACTERISTICS (Ta=25±5°C, Vcc=6V±0.25V, Vpp=21V±0.5V)

| SYMBOL | PARAMETER | TEST CONDITION | MIN. | TYP. | MAX. | UNIT |
|--------|-----------------------------|--------------------|------|------|------|------|
| tAS | Address Setup Time | — | 2 | — | — | μs |
| tAH | Address Hold Time | — | 2 | — | — | μs |
| tCES | CE Setup Time | — | 2 | — | — | μs |
| tCEH | CE Hold Time | — | 2 | — | — | μs |
| tOES | OE Setup Time | — | 2 | — | — | μs |
| tOEH | OE Hold Time | — | 2 | — | — | μs |
| tDS | Data Setup Time | — | 2 | — | — | μs |
| tDH | Data Hold Time | — | 2 | — | — | μs |
| tVS | VPP Setup Time | — | 2 | — | — | μs |
| tpw | Initial Program Pulse Width | CE = VIL, OE = VIH | 0.95 | 1 | 1.05 | ns |
| topw | Overprogram Pulse Width | Note 1 | 0.95 | 1 | 21 | ms |
| tdv | CE to Output Valid | OE = VIL | — | — | 1 | μs |
| tdf1 | CE to Output in High-Z | OE = VIL | — | — | 150 | ns |

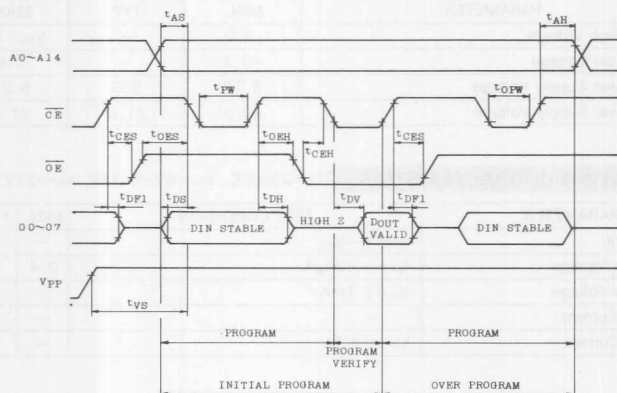
A. C. Test Conditions

- Output Load : 1 TTL Gate and CL (100pF)
- Input Pulse Rise and Fall Times : 10ns Max.
- Input Pulse Levels : 0.45~2.4V
- Timing Measurement Reference Level : Input 0.8V and 2.0V, Output 0.8V and 2.0V

Note : 1. The length of the overprogram pulse may vary as a function of the counter value X.

TIMING WAVEFORMS (PROGRAM)

- (Vcc=6V±0.25V, Vpp=21V±0.5V)



- Note : 1. Vcc must be applied simultaneously or before Vpp and cut off simultaneously or after Vpp.
2. Removing the device from socket and setting the device in socket with Vpp=21V may cause permanent damage to the device.
3. The Vpp supply voltage is permitted up to 22V for program operation, so the voltage over 22V should not be applied to the Vpp terminal. When the switching pulse voltage is applied to the Vpp terminal, the overshoot voltage of its pulse should not be exceeded 22V.

ERASURE CHARACTERISTICS

The TMM27256D's erasure is achieved by applying shortwave ultraviolet light which has a wavelength of 2537Å (Angstroms) to the chip through the transparent window.

Then integrated dose (ultraviolet light intensity [W/cm^2] \times exposure time [sec.]) for erasure should be a minimum of 15 [$\text{W}\cdot\text{sec}/\text{cm}^2$].

When the Toshiba sterilizing lamp GL-15 is used and the device is exposed at a distance of 1cm from the lamp surface, the erasure will be achieved within 60 minutes. And using commercial lamps whose

ultraviolet light intensity is a 12000 [$\mu\text{W}/\text{cm}^2$] will reduce the exposure time to about 20 minutes. (In this case, the integrated dose is 12000 [$\mu\text{W}/\text{cm}^2$] \times (20 \times 60) [sec] \cong 15 [$\text{W}\cdot\text{sec}/\text{cm}^2$].)

The TMM27256D's erasure begins to occur when exposed to light with wavelength shorter than 4000Å. The sunlight and the fluorescent lamps will include 3000~4000Å wavelength components. Therefore when used under such lighting for extended periods of time, the opaque seals-Toshiba EPROM Protect Seal AC901-are available.

OPERATION INFORMATION

The TMM27256D's six operation modes are listed in the following table. Mode selection can be

achieved by applying TTL level signal to all inputs.

| PIN NAMES(NUMBER) | | $\overline{\text{CE}}$ (20) | $\overline{\text{OE}}$ (22) | V_{PP} (1) | V_{CC} (28) | $O_0\sim O_7$ (11~13, 15~19) | POWER |
|--|-----------------|--------------------------------|--------------------------------|------------------------|-------------------------|---------------------------------|---------|
| Read Operation ($T_a=0\sim 70^\circ\text{C}$) | Read | L | L | 5 V | 5V | Data Out | Active |
| | Output Deselect | * | H | | | High Impedance | Active |
| | Standby | H | * | | | High Impedance | Standby |
| Program Operation ($T_a=25\pm 5^\circ\text{C}$) | Program | L | H | 21V | 6V | Data In | Active |
| | Program Inhibit | H | * | | | High Impedance | Active |
| | Program Verify | L | L | | | Data Out | Active |

Note H : V_{IH} , L : V_{IL} , * : V_{IH} or V_{IL}

READ MODE

The TMM27256D has two control functions. The chip enable ($\overline{\text{CE}}$) controls the operation power and should be used for device selection.

The output enable ($\overline{\text{OE}}$) control the output buffers, independent of device selection.

Assuming that $\overline{\text{CE}}=\overline{\text{OE}}=V_{\text{IL}}$, the output data is valid at the outputs after address access time from

OUTPUT DESELECT MODE

Assuming that $\overline{\text{CE}}=V_{\text{IH}}$ or $\overline{\text{OE}}=V_{\text{IH}}$, the outputs will be in a high impedance state.

So two or more TMM27256Ds can be con-

stabilizing of all addresses.

The $\overline{\text{CE}}$ to output valid (t_{CE}) is equal to the address access time (t_{ACC}).

Assuming that $\overline{\text{CE}}=V_{\text{IL}}$ and all addresses are valid, the output data is valid at the outputs after t_{OE} from the falling edge of $\overline{\text{OE}}$.

nected together on a common bus line.

When $\overline{\text{CE}}$ is decoded for device selection, all deselected devices are in low power standby mode.

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STANDBY MODE

The TMM27256D has a low power standby mode controlled by the \overline{CE} signal.

By applying a high level to the \overline{CE} input, the TMM27256D is placed in the standby mode which

PROGRAM MODE

Initially, when received by customers, all bits of the TMM27256D are in the "1" state which is erased state.

Therefore the program operation is to introduce "0s" data into the desired bit locations by electrically programming.

PROGRAM VERIFY MODE

The verify mode is to check that desired data is correctly programmed on the programmed bits.

PROGRAM INHIBIT MODE

Under the condition that the program voltage (+21V) is applied to V_{PP} terminal, a high level \overline{CE} input inhibits the TMM27256D from being programmed.

Programming of two or more TMM27256Ds in parallel with different data is easily accomplished.

HIGH SPEED PROGRAMMING MODE

The program time can be greatly decreased by using this high speed programming mode. The device is set up in the high speed programming mode when the programming voltage (+21V) is applied to the V_{PP} terminal with $V_{CC}=6V$.

The programming is achieved by applying a single TTL low level 1ms pulse to the \overline{CE} input after addresses and data are stable. Then the programmed data is verified by using Program Verify Mode.

If the programmed data is not correct, another program pulse of 1ms is applied and then the programmed data is verified. This should be repeated

until the program operates correctly (max. 20 times).

After correctly programming the selected address, the additional program pulse with width equal to that needed for initial programming is applied.

The TMM27256D is in the programming mode when the V_{PP} input is at 21V and \overline{CE} is at TTL-Low under $\overline{OE}=V_{IH}$.

The TMM27256D can be programmed any location at anytime either individually, sequentially, or at random.

The verify is accomplished with \overline{OE} and \overline{CE} at V_{IL} .

That is, all inputs except for \overline{CE} may be commonly connected, and a TTL low level program pulse is applied to the \overline{CE} of the desired device only and TTL high level signal is applied to the other devices.

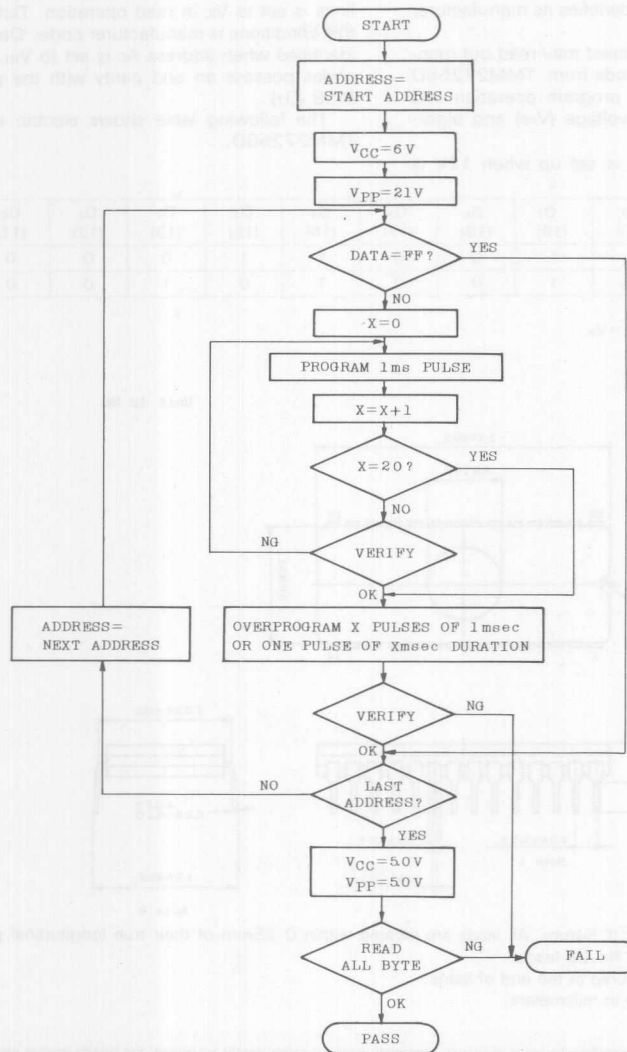
until the program operates correctly (max. 20 times).

After correctly programming the selected address, the additional program pulse with width equal to that needed for initial programming is applied.

When programming has been completed, the data in all addresses should be verified with $V_{CC}=V_{PP}=5V$.

This high speed program algorithm allows the programming of the TMM27256D to be accomplished within one and a half minutes (typ.).

HIGH SPEED PROGRAM MODE FLOW CHART



TMM27256D-15

TMM27256D-20

ELECTRIC SIGNATURE MODE

Electric signature mode allows to read out a code from TMM27256D which identifies its manufacturer and device type.

The programming equipment may read out manufacturer code and device code from TMM27256D by using this mode before program operation and automatically set program voltage (V_{PP}) and algorithm.

Electric Signature mode is set up when 12V is

applied to address line A_9 and the rest of address lines is set to V_{IL} in read operation. Data output in this conditions is manufacturer code. Device code is identified when address A_0 is set to V_{IH} . These two codes possess an odd parity with the parity bit of MSB (O_7).

The following table shows electric signature of TMM27256D.

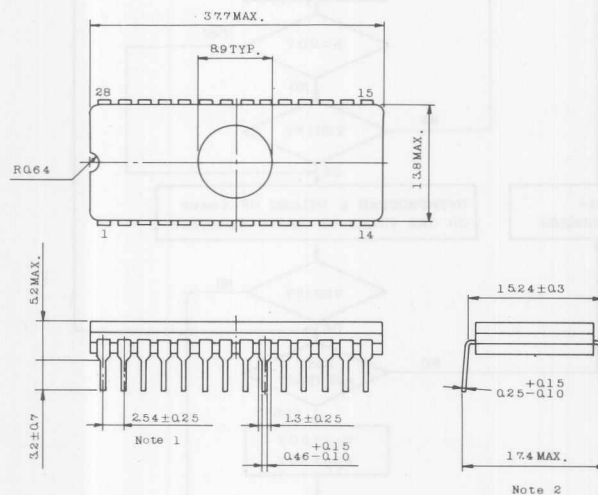
| SIGNATURE | PINS | A_0 (10) | O_7 (19) | O_6 (18) | O_5 (17) | O_4 (16) | O_3 (15) | O_2 (13) | O_1 (12) | O_0 (11) | HEX. DATA |
|------------------|----------|---------------|---------------|---------------|---------------|---------------|---------------|---------------|---------------|---------------|--------------|
| Manufacture Code | V_{IL} | 1 | 0 | 0 | 1 | 1 | 0 | 0 | 0 | 0 | 98 |
| Device Code | V_{IH} | 1 | 0 | 0 | 1 | 0 | 1 | 0 | 0 | 0 | 94 |

Notes: $A_9 = 12V \pm 0.5V$

$A_1-A_8, A_{10}-A_{14}, \overline{CE}, \overline{OE} = V_{IL}$

OUTLINE DRAWINGS

Unit in mm



Note: 1. Each lead pitch is 2.54mm. All leads are located within 0.25mm of their true longitudinal position with respect No. 1 and No.28 leads.

2. This value is measured at the end of leads.

3. All dimensions are in millimeters.

Note: Toshiba does not assume any responsibility for use of any circuitry described; no circuit patent licenses are implied, and Toshiba reserves the right, at any time without notice, to change said circuitry.

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TOSHIBA MOS MEMORY PRODUCTS

32,768 WORD × 8 BIT NMOS UV ERASABLE AND
ELECTRICALLY PROGRAMMABLE READ ONLY MEMORY
SILICON STACKED GATE MOS

TMM27256DI-15 TMM27256DI-20

DESCRIPTION

The TMM27256DI is a 32,768 word×8 bit ultraviolet light erasable and electrically programmable read only memory.

For read operation, the TMM27256DI's access time is 150ns/200ns, and the TMM27256DI operates from a single 5-volt power supply and has low power standby mode which reduces the power dissipation without increasing access time. The standby mode is achieved by applying a TTL-high level signal to the \overline{CE} input.

FEATURES

- Wide operating temperature range : $-40 \sim 85^{\circ}\text{C}$
- Fast access time : TMM27256DI-15 150ns
TMM27256DI-20 200ns
- Low power dissipation
Active : 120mA
Standby : 25mA
- Single 5V power supply

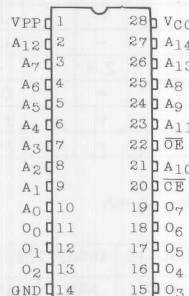
For program operation, the programming is achieved by using the high speed programming mode. Program supply voltage is 21V which is the same voltage as TMM2764D, TMM27128D and TC57256D.

The programming of TMM27256DI is accomplished within about one and a half minutes (typ.).

The TMM27256DI is fabricated with the N-channel silicon double layer gate MOS technology.

- Full static operation
- High speed programming mode
- Inputs and outputs TTL compatible
- Pin compatible with ROM TC53257P and TMM23256P and CMOS EPROM TC57256D.
- Standard 28 pin DIP cerdip package

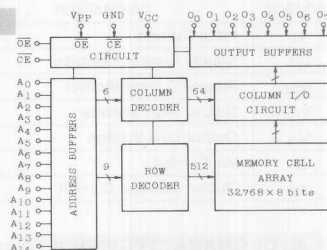
PIN CONNECTION (TOP VIEW)



PIN NAMES

| | |
|-------------------|-------------------------------|
| $A_0 \sim A_{14}$ | Address Inputs |
| $O_0 \sim O_7$ | Outputs (Inputs) |
| \overline{CE} | Chip Enable Input |
| \overline{OE} | Output Enable Input |
| V_{PP} | Program Supply Voltage |
| V_{CC} | V_{CC} Supply Voltage (+5V) |
| GND | Ground |

BLOCK DIAGRAM



MODE SELECTION

| PIN | \overline{CE} (20) | \overline{OE} (22) | V_{PP} (1) | V_{CC} (28) | $O_0 \sim O_7$ (11 ~ 13, 15 ~ 19) | POWER |
|-----------------|----------------------|----------------------|--------------|---------------|-----------------------------------|---------|
| Read | L | L | | | Data Out | Active |
| Output Deselect | * | H | 5V | 5V | High Impedance | |
| Standby | H | * | | | High Impedance | Standby |
| Program | L | H | | | Data In | Active |
| Program Inhibit | H | * | 21V | 6V | High Impedance | |
| Program Verify | L | L | | | Data Out | |

Note * : H or L

TMM27256DI-15

TMM27256DI-20

MAXIMUM RATINGS

| SYMBOL | ITEM | RATING | UNIT |
|--------------|-------------------------------|------------------|-------------------------------------|
| V_{CC} | V_{CC} Power Supply Voltage | $-0.6 \sim 7.0$ | V |
| V_{PP} | Program Supply Voltage | $-0.6 \sim 22.0$ | V |
| V_{IN} | Input Voltage | $-0.6 \sim 7.0$ | V |
| $V_{I/O}$ | Input/Output Voltage | $-0.6 \sim 7.0$ | V |
| P_D | Power Dissipation | 1.5 | W |
| T_{SOLDER} | Soldering Temperature · Time | $260 \cdot 10$ | $^{\circ}\text{C} \cdot \text{sec}$ |
| T_{STG} | Storage Temperature | $-65 \sim 125$ | $^{\circ}\text{C}$ |
| T_{OPR} | Operating Temperature | $-40 \sim 85$ | $^{\circ}\text{C}$ |

READ OPERATION

D. C. RECOMMENDED OPERATING CONDITIONS

| SYMBOL | PARAMETER | MIN. | TYP. | MAX. | UNIT |
|----------|-------------------------------|------|----------|----------------|------|
| V_{IH} | Input High Voltage | 2.2 | — | $V_{CC} + 1.0$ | V |
| V_{IL} | Input Low Voltage | -0.3 | — | 0.8 | V |
| V_{CC} | V_{CC} Power Supply Voltage | 4.75 | 5.00 | 5.25 | V |
| V_{PP} | V_{PP} Power Supply Voltage | 2.2 | V_{CC} | $V_{CC} + 0.6$ | V |

D. C. and OPERATING CHARACTERISTICS (Ta = -40~85°C, VCC = 5V ± 5%)

| SYMBOL | PARAMETER | TEST CONDITION | MIN. | TYP. | MAX. | UNIT |
|-----------|--------------------------|--------------------------------|------|------|------|---------------|
| I_{LI} | Input Current | $V_{IN} = 0 \sim V_{CC}$ | — | — | ±10 | μA |
| I_{CC1} | Supply Current (Standby) | $\overline{CE} = V_{IH}$ | — | — | 25 | mA |
| I_{CC2} | Supply Current (Active) | $\overline{CE} = V_{IL}$ | — | — | 120 | mA |
| V_{OH} | Output High Voltage | $I_{OH} = -400 \mu\text{A}$ | 2.4 | — | — | V |
| V_{OL} | Output Low Voltage | $I_{OL} = 2.1 \text{ mA}$ | — | — | 0.4 | V |
| I_{PP1} | V_{PP} Current | $V_{PP} = 0 \sim V_{CC} + 0.6$ | — | — | ±10 | μA |
| I_{LO} | Output Leakage Current | $V_{OUT} = 0.4 \sim V_{CC}$ | — | — | ±10 | μA |

A. C. CHARACTERISTICS (Ta = -40~85°C, VCC = 5V ± 5%, VPP = 2.2V ~ VCC + 0.6V)

| SYMBOL | PARAMETER | TEST CONDITION | TMM27256DI-15 | | TMM27256DI-20 | | UNIT |
|-----------|-------------------------------------|--|---------------|------|---------------|------|------|
| | | | MIN. | MAX. | MIN. | MAX. | |
| t_{ACC} | Address Access Time | $\overline{CE} = \overline{OE} = V_{IL}$ | — | 150 | — | 200 | ns |
| t_{CE} | \overline{CE} to Output Valid | $\overline{OE} = V_{IL}$ | — | 150 | — | 200 | ns |
| t_{OE} | \overline{OE} to Output Valid | $\overline{CE} = V_{IL}$ | — | 70 | — | 70 | ns |
| t_{DF1} | \overline{CE} to Output in High-Z | $\overline{OE} = V_{IL}$ | 0 | 60 | 0 | 60 | ns |
| t_{DF2} | \overline{OE} to Output in High-Z | $\overline{CE} = V_{IL}$ | 0 | 60 | 0 | 60 | ns |
| t_{OH} | Output Data Hold Time | $\overline{CE} = \overline{OE} = V_{IL}$ | 0 | — | 0 | — | ns |

A. C. TEST CONDITIONS

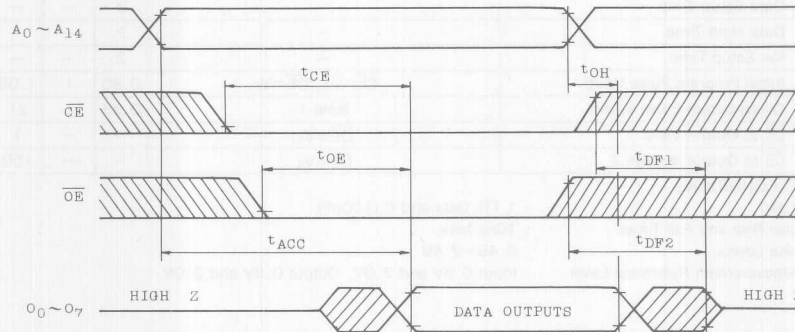
- Output Load : 1 TTL Gate and $C_L = 100\text{pF}$
- Input Pulse Rise and Fall Times : 10ns Max.
- Input Pulse Levels : 0.45V ~ 2.4V
- Timing Measurement Reference Level : Inputs 0.8V and 2.0V, Outputs 0.8V and 2.0V

CAPACITANCE * (Ta=25°C, f=1MHz)

| SYMBOL | PARAMETER | TEST CONDITION | MIN. | TYP. | MAX. | UNIT |
|------------------|--------------------|----------------------|------|------|------|------|
| C _{IN} | Input Capacitance | V _{IN} =0V | — | 4 | 6 | pF |
| C _{OUT} | Output Capacitance | V _{OUT} =0V | — | 8 | 12 | pF |

* This parameter is periodically sampled and is not 100% tested.

TIMING WAVEFORMS (READ)



PROGRAM OPERATION

D. C. and RECOMMENDED OPERATING CONDITIONS

| SYMBOL | PARAMETER | MIN. | TYP. | MAX. | UNIT |
|-----------------|--------------------------------------|------|------|----------------------|------|
| V _{IH} | Input High Voltage | 2.2 | — | V _{CC} +1.0 | V |
| V _{IL} | Input Low Voltage | -0.3 | — | 0.8 | V |
| V _{CC} | V _{CC} Power Supply Voltage | 5.75 | 6.0 | 6.25 | V |
| V _{PP} | V _{PP} Power Supply Voltage | 20.5 | 21.0 | 21.5 | V |

D. C. and OPERATING CHARACTERISTICS (Ta=25±5°C, V_{CC}=6V±0.25, V_{PP}=21V±0.5V)

| SYMBOL | PARAMETER | TEST CONDITION | MIN. | TYP. | MAX. | UNIT |
|------------------|--------------------------------|------------------------------------|------|------|------|------|
| I _{LI} | Input Current | V _{IN} =0~V _{CC} | — | — | ±10 | μA |
| V _{OH} | Output High Voltage | I _{OH} =-400μA | 2.4 | — | — | V |
| V _{OL} | Output Low Voltage | I _{OL} =2.1mA | — | — | 0.4 | V |
| I _{CC} | V _{CC} Supply Current | — | — | — | 120 | mA |
| I _{PP2} | V _{PP} Supply Current | V _{PP} =21.5V | — | — | 30 | mA |

TMM27256DI-15

TMM27256DI-20

A. C. PROGRAMMING CHARACTERISTICS

($T_a = 25 \pm 5^\circ\text{C}$, $V_{CC} = 6V \pm 0.25V$, $V_{PP} = 21V \pm 0.5V$)

| SYMBOL | PARAMETER | TEST CONDITION | MIN. | TYP. | MAX. | UNIT |
|-----------|-------------------------------------|---|------|------|------|---------------|
| t_{AS} | Address Setup Time | — | 2 | — | — | μS |
| t_{AH} | Address Hold Time | — | 2 | — | — | μS |
| t_{CES} | CE Setup Time | — | 2 | — | — | μS |
| t_{CEH} | CE Hold Time | — | 2 | — | — | μS |
| t_{OES} | OE Setup Time | — | 2 | — | — | μS |
| t_{OEH} | OE Hold Time | — | 2 | — | — | μS |
| t_{DS} | Data Setup Time | — | 2 | — | — | μS |
| t_{DH} | Data Hold Time | — | 2 | — | — | μS |
| t_{VS} | V_{PP} Setup Time | — | 2 | — | — | μS |
| t_{PW} | Initial Program Pulse Width | $\overline{CE} = V_{IL}$, $\overline{OE} = V_{IH}$ | 0.95 | 1 | 1.05 | ms |
| t_{OPW} | Overprogram Pulse Width | Note 1 | 0.95 | 1 | 21 | ms |
| t_{DV} | CE to Output Valid | $\overline{OE} = V_{IL}$ | — | — | 1 | μS |
| t_{DF1} | \overline{CE} to Output in High-Z | $\overline{OE} = V_{IL}$ | — | — | 150 | ns |

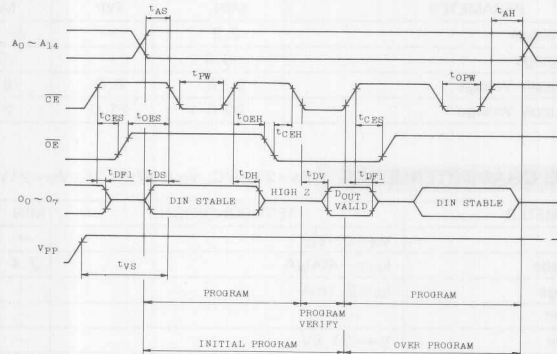
A. C. TEST CONDITIONS

- Output Load : 1 TTL Gate and $C_L(100\text{pF})$
- Input Pulse Rise and Fall Times : 10ns Max.
- Input Pulse Levels : 0.45~2.4V
- Timing Measurement Reference Level : Input 0.8V and 2.0V, Output 0.8V and 2.0V

Note : The length of the overprogram pulse may vary as a function of the counter value X.

TIMING WAVEFORMS (PROGRAM)

- ($V_{CC} = 6V \pm 0.25V$, $V_{PP} = 21V \pm 0.5V$)



- Note :
1. V_{CC} must be applied simultaneously or before V_{PP} and cut off simultaneously or after V_{PP} .
 2. Removing the device from socket and setting the device in socket with $V_{PP} = 21V$ may cause permanent damage to the device.
 3. The V_{PP} supply voltage is permitted up to 22V for program operation, so the voltage over 22V should not be applied to the V_{PP} terminal.
When the switching pulse voltage is applied to the V_{PP} terminal, the overshoot voltage of its pulse should not be exceeded 22V.

ERASURE CHARACTERISTICS

The TMM27256DI's erasure is achieved by applying shortwave ultraviolet light which has a wavelength of 2537Å (Angstroms) to the chip through the transparent window.

Then integrated dose (ultraviolet light intensity [w/cm²] × exposure time [sec.]) for erasure should be a minimum of 15 [w·sec/cm²]

When the Toshiba sterilizing lamp GL-15 is used and the device is exposed at a distance of 1 cm from the lamp surface, the erasure will be achieved within 60 minutes. And using commercial lamps whose

ultraviolet light intensity is a 12000 [μw/cm²] will reduce the exposure time to about 20 minutes. (In this case, the integrated dose is 12000 [μw/cm²] × (20×60) [sec] ≅ 15 [w·sec/cm²] .)

The TMM27256DI's erasure begins to occur when exposed to light with wavelength shorter than 4000Å. The sunlight and the fluorescent lamps will include 3000~4000Å (wavelength components.)

Therefore when used under such lighting for extended periods of time, the opeque seals-Toshiba EPROM Protect Seal AC901-are available.

OPERATION INFORMATION

The TMM27256DI's six operation modes are listed in the following table.

Mode selection can be achieved by applying TTL level signal to all inputs.

| MODE \ PIN NAMES(NUMBER) | | CE (20) | OE (22) | V _{PP} (1) | V _{CC} (28) | O ₀ ~O ₇ (11~13, 15~19) | POWER |
|--|-----------------|------------|------------|------------------------|-------------------------|--|---------|
| Read operation (T _a =40~85°C) | Read | L | L | 5V | 5V | Data Out | Active |
| | Output Deselect | * | H | | | High Impedance | Active |
| | Standby | H | * | | | High Impedance | Standby |
| Program Operation (T _a =25±5°C) | Program | L | H | 21V | 6V | Data In | Active |
| | Program Inhibit | H | * | | | High Impedance | Active |
| | Program Verify | L | L | | | Data Out | Active |

Note H : V_{IH}, L : V_{IL}, * : V_{IH} or V_{IL}

READ MODE

The TMM27256DI has two control functions. The chip enable (CE) controls the operation power and should be used for device selection.

The output enable (OE) control the output buffers, independent of device selection. Assuming that CE = OE = V_{IL}, the output data is valid at the outputs after

address access time from stabilizing of all addresses.

The CE to output valid (t_{CE}) is equal to the address access time (t_{ACC}).

Assuming that CE = V_{IL} and all addresses are valid, the output data is valid at the outputs after t_{CE} from the falling edge of OE.

OUTPUT Deselect MODE

Assuming that CE = V_{IH} or OE = V_{IH}, the outputs will be in a high impedance state. So two or more TMM27256DIs can be connected together on a

common bus line.

When CE is decoded for device selection, all deselected devices are in low power standby mode.

STANDBY MODE

The TMM27256DI has a low power standby mode controlled by the CE signal.

By applying a high level to the CE input, the TMM27256DI is placed in the standby mode which

reduce the operating current to 25mA from 120mA (about 80% reduction) by applying MOS-high level (V_{CC}) and then the outputs are in a high impedance state, independent of the OE inputs.

TMM27256DI-15

TMM27256DI-20

PROGRAM MODE

Initially, when received by customers, all bits of the TMM27256DI are in the "1" state which is erased state.

Therefore the program operation is to introduce "0s" data into the desired bit locations by electrically programming.

PROGRAM VERIFY MODE

The verify mode is to check that desired data is correctly programmed on the programmed bits.

PROGRAM INHIBIT MODE

Under the condition that the program voltage (+21V) is applied to V_{PP} terminal, a high level \overline{CE} input inhibits the TMM 27256DI from being programmed.

Programming of two or more TMM27256DIs in parallel with different data is easily accomplished.

HIGH SPEED PROGRAMMING MODE

The Program time can be greatly decreased by using this high speed programming mode.

The device is set up in the high speed programming mode when the programming voltage (+21V) is applied to the V_{PP} terminal with $V_{CC}=6V$.

The programming is achieved by applying a single TTL low level 1ms pulse to the \overline{CE} input after addresses and data are stable. Then the programmed data is verified by using Program Verify Mode.

If the programmed data is not correct, another program pulse of 1ms is applied and then the programmed data is verified. This should be repeated

The TMM 27256DI is in the programming mode when the V_{PP} input is at 21V and \overline{CE} is at TTL-Low under $\overline{OE}=V_{IH}$.

The TMM27256DI can be programmed any location at anytime either individually, sequentially, or at random.

The verify is accomplished with \overline{OE} and \overline{CE} at V_{IL} .

That is, all inputs except for \overline{CE} may be commonly connected, and a TTL low level program pulse is applied to the \overline{CE} of the desired device only and TTL high level signal is applied to the other devices.

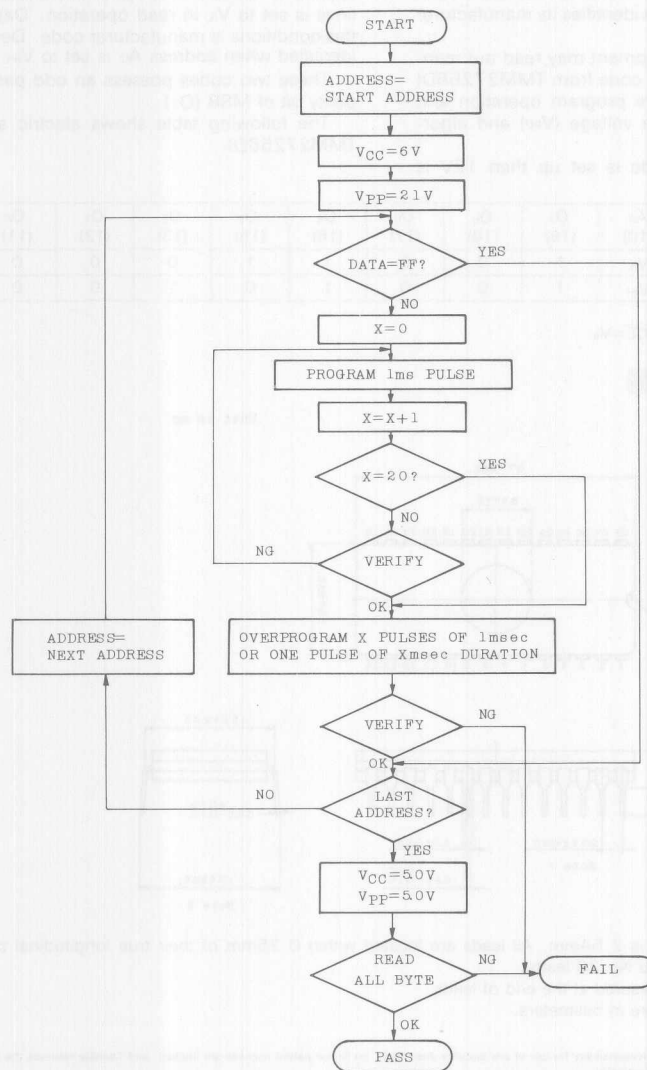
until the program operates correctly (max. 20 tims).

After correctly programming the selected address, the additional program pulse with width equal to that needed for initial programming is applied.

When programming has been completed, the data in all addresses should be verified with $V_{CC}=V_{PP}=5V$.

This high speed program algorithm allows the programming of the TMM27256DI to be accomplished within one and a half minutes (typ.).

HIGH SPEED PROGRAM MODE FLOW CHART



TMM27256DI-15

TMM27256DI-20

ELECTRIC SIGNATURE MODE

Electric signature mode allows to read out a code from TMM27256DI which identifies its manufacturer and device type.

The programming equipment may read out manufacturer code and device code from TMM27256DI by using this mode before program operation and automatically set program voltage (V_{PP}) and algorithm.

Electric Signature mode is set up then 12V is

applied to address line A_9 and the rest of address lines is set to V_{IL} in read operation. Data output in this conditions is manufacturer code. Device code is identified when address A_0 is set to V_{IH} .

These two codes possess an odd parity with the parity bit of MSB (O_7).

The following table shows electric signature of TMM27256DI.

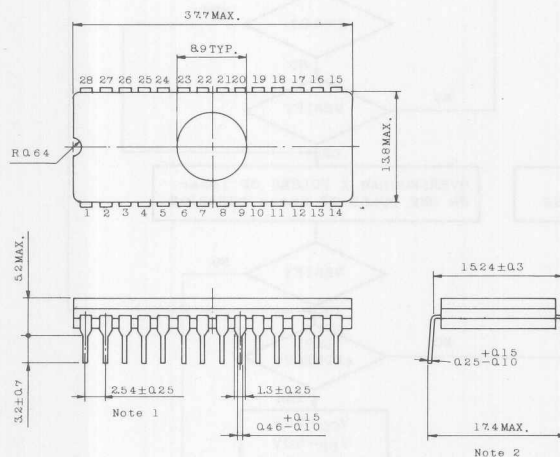
| SIGNATURE \ PINS | A_0 (10) | O_7 (19) | O_6 (18) | O_5 (17) | O_4 (16) | O_3 (15) | O_2 (13) | O_1 (12) | O_0 (11) | HEX. DATA |
|-------------------|---------------|---------------|---------------|---------------|---------------|---------------|---------------|---------------|---------------|--------------|
| Manufacturer Code | V_{IL} | 1 | 0 | 0 | 1 | 1 | 0 | 0 | 0 | 98 |
| Device Code | V_{IH} | 1 | 0 | 0 | 1 | 0 | 1 | 0 | 0 | 94 |

Notes: $A_9 = 12V \pm 0.5V$

$A_1-A_8, A_{10}-A_{14}, \overline{CE}, \overline{OE} = V_{IL}$

OUTLINE DRAWINGS

Unit in mm



- Note : 1. Each lead pitch is 2.54mm. All leads are located within 0.25mm of their true longitudinal position with respect No.1 and No.28 leads.
 2. This value is measured at the end of leads.
 3. All dimensions are in millimeters.

Note : Toshiba does not assume any responsibility for use of any circuitry described ; no circuit patent licenses are implied, and Toshiba reserves the right, at any time without notice, to change said circuitry.

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CHILD PROSECUTION: A CHALLENGE FOR THE FUTURE

TOSHIBA MOS MEMORY PRODUCTS

32,768 WORD X 8 BIT CMOS UV ERASABLE AND
ELECTRICALLY PROGRAMMABLE READ ONLY
MEMORY

TC57256D-20 TC57256D-25

SILICON STACKED GATE MOS

DESCRIPTION

The TC57256D is a 32,768 word x 8 bit CMOS ultraviolet light erasable and electrically programmable read only memory. For read operation, the TC57256D's access time is 200ns, and the TC57256D operates from a single 5-volt power supply and has low power standby mode which reduces the power dissipation without increasing access time. The standby mode is achieved by applying a TTL-high level signal to the \overline{CE} input. Advanced CMOS technology reduces the maximum active current to 30

mA/5MHz and standby current to 100 μ A.

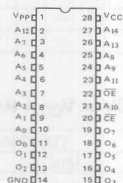
For program operation, the programming is achieved by using the high speed programming mode. Program supply voltage is 21V which is the same voltage as TMM2764D and TMM27128D. The programming of TC57256D is accomplished within about one and a half minutes (typ.) TC57256D is fabricated with the CMOS technology and the N-channel silicon double layer gate MOS technology.

FEATURES

- Peripheral circuit: CMOS
Memory cell : N-MOS
- Low power dissipation
30mA/5MHZ (active)
100 μ A (standby)
- Fast access time TC57256D-20 200 ns
TC57256D-25 250 ns

- Single 5V power supply
- Full static operation
- High speed programming mode
- Inputs and outputs TTL compatible
- Pin compatible with ROM TC53257P and TMM23256P
- Standard 28 pin DIP cerdip Package

PIN CONNECTION (TOP VIEW)



PIN NAMES

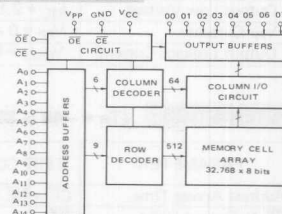
| | |
|-------------------|-------------------------------|
| $A_0 \sim A_{14}$ | Address Inputs |
| $O_0 \sim O_7$ | Outputs (Inputs) |
| \overline{CE} | Chip Enable Input |
| \overline{OE} | Output Enable Input |
| V_{PP} | Program Supply Voltage |
| V_{CC} | V_{CC} Supply Voltage (+5V) |
| GND | Ground |

MODE SELECTION

| PIN | \overline{CE} (20) | \overline{OE} (22) | V_{PP} (1) | V_{CC} (28) | $O_0 \sim O_7$ (11 ~ 13, 15 ~ 19) | POWER |
|-----------------|-------------------------|-------------------------|-----------------|------------------|--------------------------------------|--------|
| Read | L | L | 5V | 5V | Data Out | Active |
| Output Deselect | * | H | | 5V | High Impedance | |
| Standby | H | * | | 5V | High Impedance | |
| Program | L | H | 21V | 6V | Data In | Active |
| Program Inhibit | H | * | | | High Impedance | |
| Program Verify | L | L | | | Data Out | |

* : H or L

BLOCK DIAGRAM



TC57256D-20

TC57256D-25

MAXIMUM RATINGS

| SYMBOL | ITEM | RATING | UNIT |
|--------------|-------------------------------|--------------------------|-------------------------------------|
| V_{CC} | V_{CC} Power Supply Voltage | $-0.6 \sim 7.0$ | V |
| V_{PP} | Program Supply Voltage | $-0.6 \sim 22.0$ | V |
| V_{IN} | Input Voltage | $-0.6 \sim 7.0$ | V |
| $V_{I/O}$ | Input/Output Voltage | $-0.6 \sim V_{CC} + 0.5$ | V |
| P_D | Power Dissipation | 1.5 | W |
| T_{SOLDER} | Soldering Temperature Time | $260 \cdot 10$ | $^{\circ}\text{C} \cdot \text{sec}$ |
| T_{STRG} | Storage Temperature | $-65 \sim 125$ | $^{\circ}\text{C}$ |
| T_{OPR} | Operating Temperature | $-40 \sim 85$ | $^{\circ}\text{C}$ |

READ OPERATION

D. C. RECOMMENDED OPERATING CONDITIONS

| SYMBOL | PARAMETER | MIN. | TYP. | MAX. | UNIT |
|----------|-------------------------------|------|----------|----------------|------|
| V_{IH} | Input High Voltage | 2.2 | — | $V_{CC} + 0.3$ | V |
| V_{IL} | Input Low Voltage | -0.3 | — | 0.8 | V |
| V_{CC} | V_{CC} Power Supply Voltage | 4.75 | 5.00 | 5.25 | V |
| V_{PP} | V_{PP} Power Supply Voltage | 2.0 | V_{CC} | $V_{CC} + 0.3$ | V |

D. C. and OPERATING CHARACTERISTICS ($T_a = -40 \sim 85^{\circ}\text{C}$, $V_{CC} = 5\text{V} \pm 5\%$)

| SYMBOL | PARAMETER | TEST CONDITION | MIN. | TYP. | MAX. | UNIT |
|------------|------------------------|--|------|------|----------|---------------|
| I_{LI} | Input current | $V_{IN} = 0 \sim V_{CC}$ | — | — | ± 10 | μA |
| I_{CC01} | Operating Current | $\overline{CE} = 0$ | — | — | 30 | mA |
| I_{CC02} | | $f = 5\text{MHz}$ | — | — | 10 | mA |
| I_{CCS1} | Standby Current | $\overline{CE} = V_{IH}$ | — | — | 1 | mA |
| I_{CCS2} | | $\overline{CE} = V_{CC} - 0.2\text{V}$ | — | — | 100 | μA |
| V_{OH} | Output High Voltage | $I_{OH} = -400\mu\text{A}$ | 2.4 | — | — | V |
| V_{OL} | Output Low Voltage | $I_{OL} = 2.1\text{mA}$ | — | — | 0.4 | V |
| I_{PP1} | V_{PP} Current | $V_{PP} = 0 \sim V_{CC} + 0.3\text{V}$ | — | — | ± 10 | μA |
| I_{LO} | Output Leakage Current | $V_{OUT} = 0.4\text{V} \sim V_{CC}$ | — | — | ± 10 | μA |

A. C. CHARACTERISTICS ($T_a = -40 \sim 85^{\circ}\text{C}$, $V_{CC} = 5\text{V} \pm 5\%$, $V_{PP} = 2.0\text{V} \sim V_{CC} + 0.3\text{V}$)

| SYMBOL | PARAMETER | TEST CONDITION | TC57256D-20 | | TC57256D-25 | | UNIT |
|-----------|-------------------------------------|--|-------------|------|-------------|------|------|
| | | | MIN. | MAX. | MIN. | MAX. | |
| t_{ACC} | Address Access Time | $\overline{CE} = \overline{OE} = V_{IL}$ | — | 200 | — | 250 | ns |
| t_{CE} | \overline{CE} to Output Valid | $\overline{OE} = V_{IL}$ | — | 200 | — | 250 | ns |
| t_{OE} | \overline{OE} to Output Valid | $\overline{CE} = V_{IL}$ | — | 70 | — | 100 | ns |
| t_{DF1} | \overline{CE} to Output in High-Z | $\overline{OE} = V_{IL}$ | 0 | 60 | 0 | 90 | ns |
| t_{DF2} | \overline{OE} to Output in High-Z | $\overline{CE} = V_{IL}$ | 0 | 60 | 0 | 90 | ns |
| t_{OH} | Output Data Hold Time | $\overline{CE} = \overline{OE} = V_{IL}$ | 0 | — | 0 | — | ns |

A. C. TEST CONDITIONS

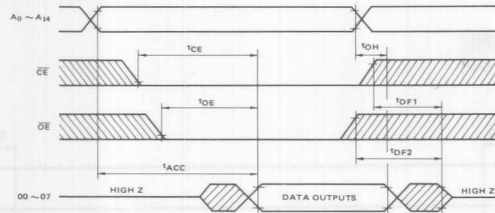
Output Load : 1 TTL Gate and $C_L = 100\text{pF}$
 Input Pulse Rise and Fall Times : 10 ns Max.
 Input Pulse Levels : 0.45 ~ 2.4V
 Timing Measurement Reference Level : Inputs 0.8V and 2.0V, Outputs 0.8V and 2.0V

CAPACITANCE * ($T_a = 25^\circ\text{C}$, $f = 1\text{MHz}$)

| SYMBOL | PARAMETER | TEST CONDITION | MIN. | TYP. | MAX. | UNIT |
|-----------|--------------------|-----------------------|------|------|------|------|
| C_{IN} | Input Capacitance | $V_{IN} = 0\text{V}$ | — | 4 | 6 | pF |
| C_{OUT} | Output Capacitance | $V_{OUT} = 0\text{V}$ | — | 8 | 12 | pF |

*This parameter is periodically sampled and is not 100% tested.

TIMING WAVEFORMS (READ)



PROGRAM OPERATION

D.C. RECOMMENDED OPERATING CONDITIONS

| SYMBOL | PARAMETER | MIN. | TYP. | MAX. | UNIT |
|----------|-------------------------------|------|------|----------------|------|
| V_{IH} | Input High Voltage | 2.2 | — | $V_{CC} + 0.3$ | V |
| V_{IL} | Input Low Voltage | -0.3 | — | 0.8 | V |
| V_{CC} | V_{CC} Power Supply Voltage | 5.75 | 6.0 | 6.25 | V |
| V_{PP} | V_{PP} Power Supply Voltage | 20.5 | 21.0 | 21.5 | V |

D.C. and OPERATING CHARACTERISTICS ($T_a = 25 \pm 5^\circ\text{C}$, $V_{CC} = 6\text{V} \pm 0.25\text{V}$, $V_{PP} = 21\text{V} \pm 0.5$)

| SYMBOL | PARAMETER | TEST CONDITION | MIN. | TYP. | MAX. | UNIT |
|-----------|-------------------------|----------------------------|------|------|----------|---------------|
| I_{LI} | Input Current | $V_{IN} = 0 \sim V_{CC}$ | — | — | ± 10 | μA |
| V_{OH} | Output High Voltage | $I_{OH} = -400\mu\text{A}$ | 2.4 | — | — | V |
| V_{OL} | Output Low Voltage | $I_{OL} = 2.1\text{mA}$ | — | — | 0.4 | V |
| I_{CC} | V_{CC} Supply Current | — | — | — | 30 | mA |
| I_{PP2} | V_{PP} Supply Current | $V_{PP} = 21.5\text{V}$ | — | — | 30 | mA |

A.C. PROGRAMMING CHARACTERISTICS ($T_a = 25 \pm 5^\circ\text{C}$, $V_{CC} = 6\text{V} \pm 0.25\text{V}$, $V_{PP} = 21\text{V} \pm 0.5$)

| SYMBOL | PARAMETER | TEST CONDITION | MIN. | TYP. | MAX. | UNIT |
|-----------|-----------------------------|---|------|------|------|---------------|
| t_{AS} | Address Setup Time | — | 2 | — | — | μs |
| t_{AH} | Address Hold Time | — | 2 | — | — | μs |
| t_{CES} | CE Setup Time | — | 2 | — | — | μs |
| t_{CEH} | CE Hold Time | — | 2 | — | — | μs |
| t_{OES} | OE Setup Time | — | 2 | — | — | μs |
| t_{OEH} | OE Hold Time | — | 2 | — | — | μs |
| t_{DS} | Data Setup Time | — | 2 | — | — | μs |
| t_{DH} | Data Hold Time | — | 2 | — | — | μs |
| t_{VS} | V_{PP} Setup Time | — | 2 | — | — | μs |
| t_{PW} | Initial Program Pulse Width | $\overline{CE} = V_{IL}$, $\overline{OE} = V_{IH}$ | 0.95 | 1 | 1.05 | ms |
| t_{OPW} | Overprogram Pulse Width | Note 1 | 0.95 | 1 | 21 | ms |
| t_{DV} | CE to Output Valid | $\overline{OE} = V_{IL}$ | — | — | 1 | μs |
| t_{DF1} | CE to Output in High-Z | $\overline{OE} = V_{IL}$ | — | — | 150 | ns |

TC57256D-20 TC57256D-25

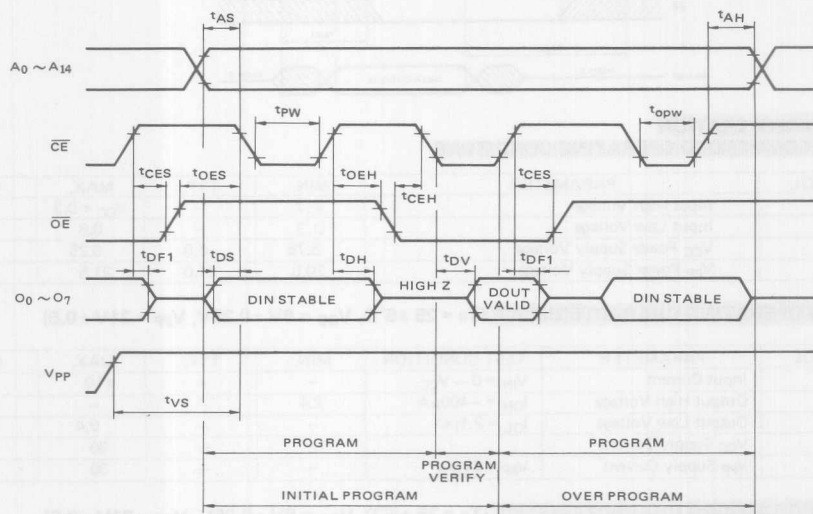
A. C. TEST CONDITIONS

| | |
|------------------------------------|---|
| Output Load | : 1 TTL Gate and C_L (100pF) |
| Input Pulse Rise and Fall Times | : 10 ns Max. |
| Input Pulse Levels | : 0.45 ~ 2.4V |
| Timing Measurement Reference Level | : Input 0.8V and 2.0V, Output 0.8V and 2.0V |

Note 1: The length of the overprogram pulse may vary as function of the counter value X.

TIMING WAVEFORMS (PROGRAM)

($V_{CC} = 6V \pm 0.25V$, $V_{PP} = 21V \pm 0.5V$)



- Note:
- (1) V_{CC} must be applied simultaneously or before V_{PP} and cut off simultaneously or after V_{PP} .
 - (2) Removing the device from socket and setting the device in socket with $V_{PP} = 21V$ may cause permanent damage to the device.
 - (3) The V_{PP} supply voltage is permitted up to 22V for program operation, so the voltage over 22V should not be applied to the V_{PP} terminal. When the switching pulse voltage is applied to the V_{PP} terminal, the overshoot voltage of its pluse should not be exceeded 22V.

ERASURE CHARACTERISTICS

The TC57256D's erasure is achieved by applying shortwave ultraviolet light which has a wavelength of 2537Å (Angstroms) to the chip through the transparent window.

Then integrated does (ultraviolet light intensity [w/cm^2] \times exposure time [sec.]) for erasure should be a minimum of 15 [$\text{w}\cdot\text{sec}/\text{cm}^2$].

When the Toshiba sterilizing lamp GL-15 is used and the device is exposed at a distance of 1cm from the lamp surface, the erasure will be achieved within 60 minutes. And using commercial lamps whose

ultraviolet light intensity is a 12000 [$\mu\text{w}/\text{cm}^2$] will reduce the exposure time to about 20 minutes. (In this case, the integrated does is 12000 [$\mu\text{w}/\text{cm}^2$] \times (20 \times 60) [sec.] \approx 15 [$\text{w}\cdot\text{sec}/\text{cm}^2$].)

The TC57256D's erasure begins to occur when exposed to light with wavelength shorter than 4000Å. The sunlight and the fluorescent lamps will include 3000 ~ 4000Å wavelength components. Therefore when used under such lighting for extended periods of time, the opaque seal Toshiba EPROM Protect Seal AC901 is available.

OPERATION INFORMATION

The TC57256D's six operation modes are listed in the following table. Mode selection can be achieved

by applying TTL level signal to all inputs.

| PIN NAMES (NUMBER) | | CE (20) | OE (22) | V _{PP} (1) | V _{CC} (28) | O ₀ ~ O ₇ (11 ~ 13, 15 ~ 19) | POWER |
|--|-----------------|------------|------------|------------------------|-------------------------|---|---------|
| Read Operation (T _a = -40 ~ 85°C) | Read | L | L | 5V | 5V | Data Out | Active |
| | Output Deselect | * | H | | | High Impedance | Active |
| | Standby | H | * | | | High Impedance | Standby |
| Program Operation (T _a = 25 ± 5°C) | Program | L | H | 21V | 6V | Data In | Active |
| | Program Inhibit | H | * | | | High Impedance | Active |
| | Program Verify | L | L | | | Data Out | Active |

Note: H: V_{IH}, L: V_{IL}, *: V_{IH} or V_{IL}

READ MODE

The TC57256D has two control functions. The chip enable (CE) controls the operation power and should be used for device selection.

The output enable (OE) control the output buffers, independent of device selection. Assuming that CE = OE = V_{IL}, the output data is valid at the outputs after address access time from stabilizing of

all addresses.

The CE to output valid (t_{CE}) is equal to the address access time (t_{ACC}).

Assuming that CE = V_{IL} and all addresses are valid, the output data is valid at the outputs after t_{OE} from the falling edge of OE.

TC57256D-20

TC57256D-25

OUTPUT DESELECT MODE

Assuming that $\overline{CE} = V_{IH}$ or $\overline{OE} = V_{IH}$, the outputs will be in a high impedance state. So two or more TC57256D's can be connected together on a common

STANDBY MODE

The TC57256D has a low power standby mode controlled by the \overline{CE} signal. By applying a high level to the \overline{CE} input, the TC57256D is placed in the standby mode which reduce the operating current

PROGRAM MODE

Initially, when received by customers, all bits of the TC57256D are in the "1" state which is erased state.

Therefore the program operation is to introduce "0's" data into the desired bit locations by electrically programming.

PROGRAM VERIFY MODE

The verify mode is to check that desired data is correctly programmed on the programmed bits.

PROGRAM INHIBIT MODE

Under the condition that the program voltage (+21V) is applied to V_{pp} terminal, a high level \overline{CE} input inhibits the TC57256D from being programmed.

Programming of two or more TC57256Ds in parallel with different data is easily accomplished.

HIGH SPEED PROGRAMMING MODE

The program time can be greatly decreased by using this high speed programming mode. The device is set up in the high speed programming mode when the programming voltage (+21V) is applied to the V_{pp} terminal with $V_{CC} = 6V$.

The programming is achieved by applying a single TTL low level 1ms pulse to the \overline{CE} input after addresses and data are stable. Then the programmed data is verified by using Program Verify Mode.

If the programmed data is not correct, another program pulse of 1ms is applied and the programmed

bus line. When \overline{CE} is decoded for device selection, all deselected devices are in low power standby mode.

to 100 μ A by applying MOS-high level (V_{CC}) and then the outputs are in a high impedance state, independent of the \overline{OE} inputs.

The TC57256D is in the programming mode when the V_{pp} input is at 21V and \overline{CE} is at TTL-Low under $\overline{OE} = V_{IH}$.

The TC57256D can be programmed any location at anytime either individually, sequentially, or at random.

The verify is accomplished with \overline{OE} and \overline{CE} at V_{IL} .

That is, all inputs except for \overline{CE} may be commonly connected, and a TTL low level program pulse is applied to the \overline{CE} of the desired device only and TTL high level signal is applied to the other devices.

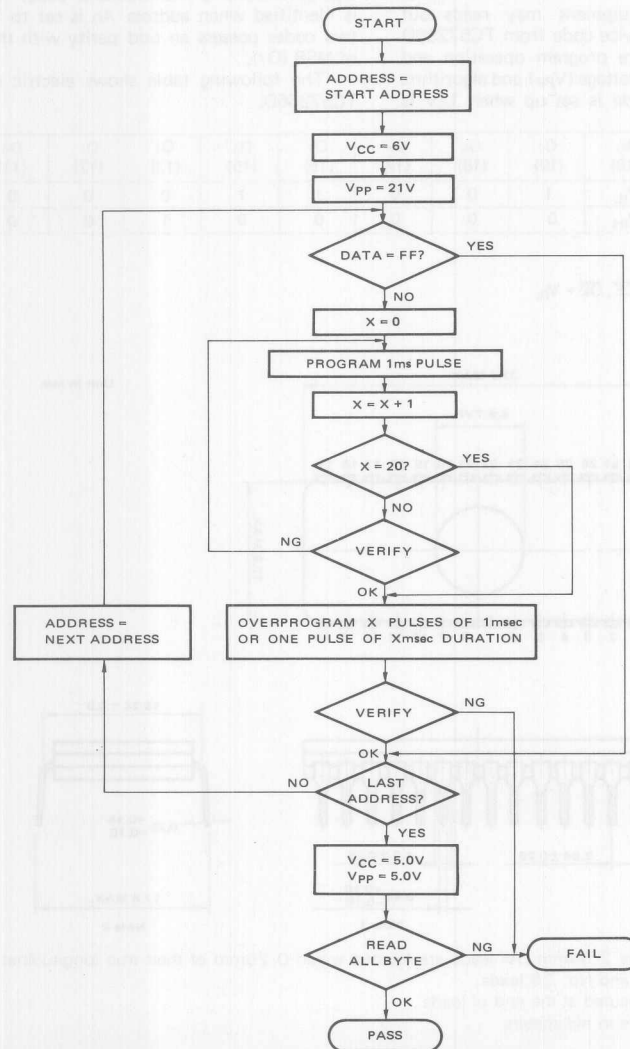
data is verified. This should be repeated until the program operates correctly (max. 20 times).

After correctly programming the selected address, the additional program pulse with width equal to that needed for initial programming is applied.

When programming has been completed, the data in all addresses should be verified with $V_{CC} = V_{pp} = 5V$.

This high speed program algorithm allows the programming of the TC57256D to be accomplished within one and a half minutes (typ.).

HIGH SPEED PROGRAM MODE FLOW CHART



TC57256D-20 TC57256D-25

ELECTRIC SIGNATURE MODE

Electric signature mode allows to read out a code from TC57256D which identifies its manufacturer and device type.

The programming equipment may reads out manufacturer code and device code from TC57256D by using this mode before program operation and automatically set program voltage (V_{pp}) and algorithm.

Electric Signature mode is set up when 12V is

applied to address line A_9 and the rest of address lines is set to V_{IL} in read operation. Data output in this conditions is manufacturer code. Device code is identified when address A_0 is set to V_{IH} . These two codes possess an odd parity with the parity bit of MSB (O_7).

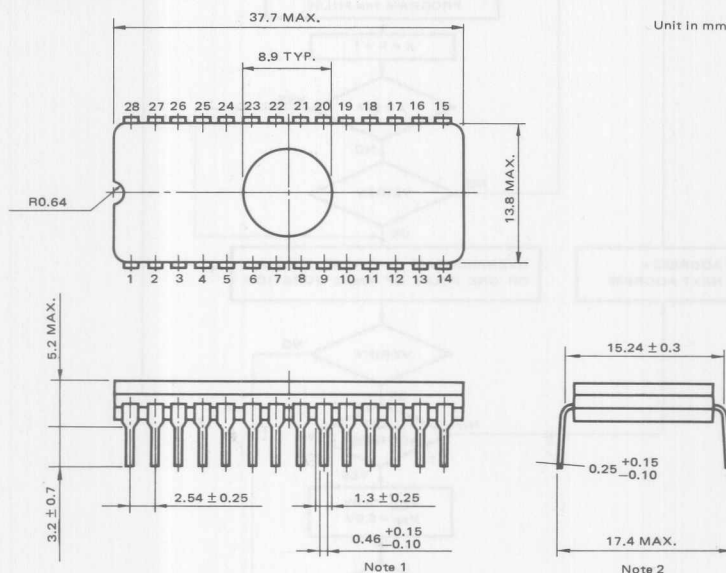
The following table shows electric signature of TC57256D.

| SIGNATURE | PINS | A_0 (10) | O_7 (19) | O_6 (18) | O_5 (17) | O_4 (16) | O_3 (15) | O_2 (13) | O_1 (12) | O_0 (11) | HEX. DATA |
|-------------------|----------|---------------|---------------|---------------|---------------|---------------|---------------|---------------|---------------|---------------|--------------|
| Manufacturer Code | V_{IL} | 1 | 0 | 0 | 1 | 1 | 0 | 0 | 0 | 0 | 98 |
| Device Code | V_{IH} | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 0 | 0 | 04 |

Notes: $A_9 = 12V \pm 0.5V$

$A_1 - A_8, A_{10} - A_{14}, \overline{CE}, \overline{OE} = V_{IL}$

OUTLINE DRAWINGS



- Note: 1. Each lead pitch is 2.54mm. All leads are located within 0.25mm of their true longitudinal position with respect to No. 1 and No. 28 leads.
2. This value is measured at the end of leads.
3. All dimensions are in millimeters.

NMOS Mask Read Only Memories

WINDY WALK BEACH ONLY WINDY WALK

TOSHIBA MOS MEMORY PRODUCTS

64K BIT (8K WORD × 8 BIT) MASK ROM
N-CHANNEL SILICON GATE

TMM2365P

DESCRIPTION

The TMM2365P is a 65536 bit fully static read only memory organized as 8192 words by 8 bits with a low bit cost, thus being most suitable for use in programming of production apparatus using micro-processor.

The TMM2365P is fully compatible with a 64 K bits EPROM TMM2764D, so completely replace EPROM socket.

The TMM2365P also features an automatic stand-by power mode. When deselected by Chip Enable

($CE_1 \sim \overline{3}/\overline{CE_1} \sim \overline{3}$), the operating current is reduced from 100mA (MAX) to 25mA(MAX). Output Enable (\overline{OE}) is effective in preventing data confliction of a common bus line.

The TMM2365P is fabricated with ion implanted N-channel silicon gate technology. This technology allows a production of high performance.

The TMM2365P is moulded in a 28 pin standard plastic package, 0.6 inch in width.

FEATURES

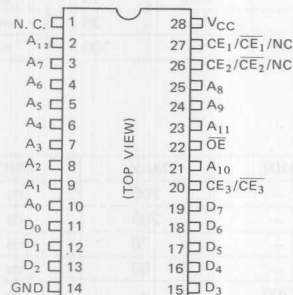
- Single 5V power Supply
- Access Time: 200ns max.
- Power Dissipation
 - Average Current: 100mA max.
 - Standby Current: 25mA max.
- Input and Output: TTL Compatible

- Three State Outputs: Wired OR Capability
- Output Buffer Control: \overline{OE}
- Programmable Chip Enable: $CE_1/\overline{CE_1}$, $CE_2/\overline{CE_2}$, $CE_3/\overline{CE_3}$

Easy Memory Expansion

- Compatible with 64K EPROM TMM2764D

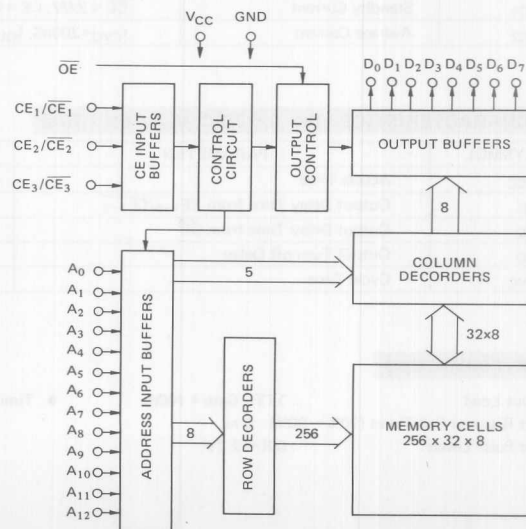
PIN CONNECTION



PIN NAMES

| | |
|--|-----------------------|
| $A_0 \sim A_{12}$ | Address inputs |
| $D_0 \sim D_7$ | Data outputs |
| \overline{OE} | Output enable input |
| $CE_1/\overline{CE_1}$, $CE_2/\overline{CE_2}$, $CE_3/\overline{CE_3}$ | Chip enable inputs |
| N. C. | No connection |
| V_{CC} | Power supply terminal |
| GND | Ground |

BLOCK DIAGRAM



TMM2365P

MAXIMUM RATINGS

| SYMBOL | ITEM | RATING | UNIT |
|-------------------|--|------------|----------|
| V_{CC} | Power Supply Voltage | -0.5 ~ 7.0 | V |
| V_{IN}, V_{OUT} | Input and Output Voltage | -0.5 ~ 7.0 | V |
| T_{OPR} | Operating Temperature | 0 ~ 70 | °C |
| T_{STG} | Storage Temperature | -55 ~ 150 | °C |
| T_{SD} | Soldering Temperature • Time | 260 • 10 | °C • sec |
| P_D | Power Dissipation ($T_a = 70^\circ\text{C}$) | 1.0 | W |

D.C. OPERATING CONDITIONS ($T_a = 0 \sim 70^\circ\text{C}$)

| SYMBOL | PARAMETER | CONDITIONS | MIN. | TYP. | MAX. | UNIT |
|----------|----------------------|------------|------|------|------------|------|
| V_{IH} | Input High Voltage | — | 2.0 | — | $V_{CC}+1$ | V |
| V_{IL} | Input Low Voltage | — | -0.5 | — | 0.8 | V |
| V_{CC} | Power Supply Voltage | — | 4.5 | 5.0 | 5.5 | V |

D.C. and OPERATING CHARACTERISTICS ($T_a = 0 \sim 70^\circ\text{C}$)

| SYMBOL | PARAMETER | CONDITIONS | MIN. | MAX. | UNIT |
|-----------|------------------------|---|------|------|---------------|
| I_{IH} | Input High Current | $V_{IN} = 5.5\text{V}$ | — | 10 | μA |
| I_{IL} | Input Low Current | $V_{IN} = \text{GND}$ | — | -10 | μA |
| V_{OH} | Output High Voltage | $I_{OH} = -400\mu\text{A}$ | 2.4 | — | V |
| V_{OL} | Output Low Voltage | $I_{OL} = 3.2\text{mA}$ | — | 0.4 | V |
| I_{LO} | Output Leakage Current | $0\text{V} \leq V_{OUT} \leq V_{CC}$ | -10 | 10 | μA |
| I_{CC1} | Standby Current | $\overline{CE} = 2.0\text{V}, CE = 0.8\text{V}$ | — | 25 | mA |
| I_{CC2} | Average Current | $t_{CYC} = 200\text{nS}, I_{OUT} = 0\text{mA}$ | — | 100 | mA |

A.C. CHARACTERISTICS ($T_a = 0 \sim 70^\circ\text{C}, V_{CC} = 5\text{V} \pm 10\%$)

| SYMBOL | PARAMETER | MIN. | MAX. | UNIT |
|-----------|---|------|------|------|
| t_{ACC} | Access Time | — | 200 | ns |
| t_{CE} | Output Delay Time from $\overline{CE}_{1-3}/CE_{1-3}$ | — | 200 | ns |
| t_{OE} | Output Delay Time from \overline{OE} | — | 70 | ns |
| t_{OD} | Output Turn off Delay | — | 60 | ns |
| t_{CYC} | Cycle Time | 200 | — | ns |

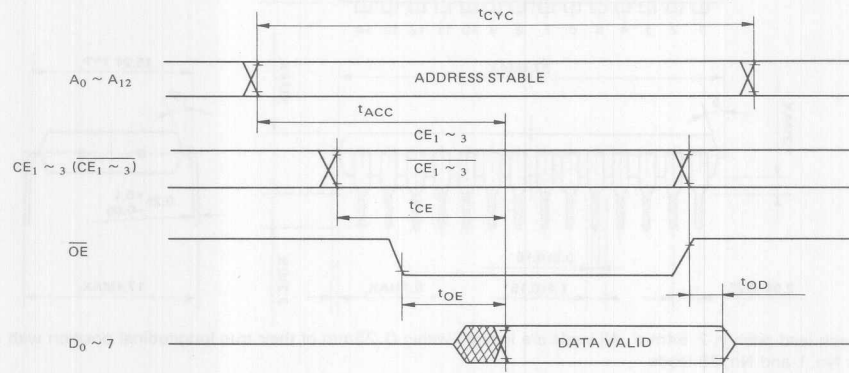
A.C. TEST CONDITIONS

- Output Load : 1TTL Gate + 100pF
- Input Rise and Fall Times (10% ~ 90%) : 5 ns
- Input Pulse Levels : 0.8 ~ 2.2V
- Timing Measurement Reference Levels :
 - Input : 1V and 2.0V
 - Output: 0.8V and 2.0V

CAPACITANCE ($T_a = 25^\circ\text{C}$, $f = 1\text{MHz}$)

| SYMBOL | PARAMETER | CONDITIONS | MIN. | MAX. | UNIT |
|-----------|--------------------|-----------------------------|------|------|------|
| C_{IN} | Input Capacitance | $V_{IN} = \text{A.C. GND}$ | — | 8 | pF |
| C_{OUT} | Output Capacitance | $V_{OUT} = \text{A.C. GND}$ | — | 10 | pF |

Note: This parameter is periodically sampled and is not 100% tested.

TIMING WAVEFORMS

Note: t_{OD} is specified from \overline{OE} or $\overline{CE}/\overline{CE}$, whichever occurs first.

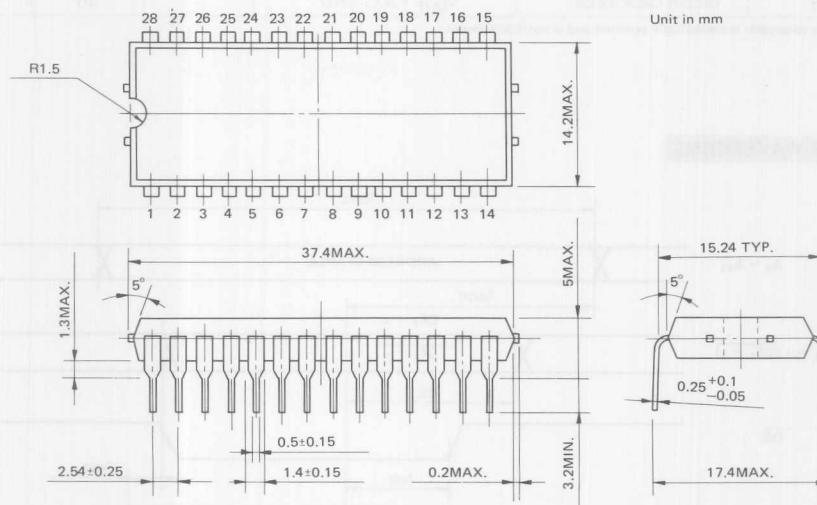
POWER ON

The TMM2365 has self substrate-bias generator internally. So a minimum $100\mu\text{s}$ time delay is

required after the application of V_{CC} ($4.5 \sim 5.5\text{V}$) before proper device operation is achieved.

TMM2365P

OUTLINE DRAWINGS



Note : Each lead pitch is 2.54mm. All leads are located within 0.25mm of their true longitudinal position with respect to No.1 and No.28 leads.

Note: Toshiba does not assume any responsibility for use of any circuitry described; no circuit patent licenses are implied, and Toshiba reserves the right, at any time without notice, to change said circuitry.
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TOSHIBA MOS MEMORY PRODUCTS

64K BIT (8K WORD \times 8 BIT) MASK ROM
N-CHANNEL SILICON GATE MOS

TMM2366P

DESCRIPTION

The TMM2366P is a 65536 bit fully static read only memory organized as 8192 words by 8 bits with a low bit cost, thus being most suitable for use in programming of production apparatus using micro-processor.
The TMM2366P also features an automatic standby power mode. When deselected by Chip Enable (CE/ $\overline{\text{CE}}$), the operating current is reduced from 100mA (MAX) to 25mA (MAX).

FEATURES

- Single 5V power Supply
- Access Time: 200ns max.
- Power Dissipation
Average Current: 100mA max.
Standby Current: 25mA max.

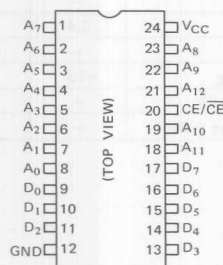
The TMM2366P is fabricated with ion implanted N-channel silicon gate technology.

This technology allows a production of high performance.

The TMM2366P is moulded in a 24 pin standard plastic package, 0.6 inch in width.

- Input and Output: TTL Compatible
- Three State Outputs: Wired OR Capability
- Programmable Chip Enable: CE/ $\overline{\text{CE}}$
- Compatible with TMS4764

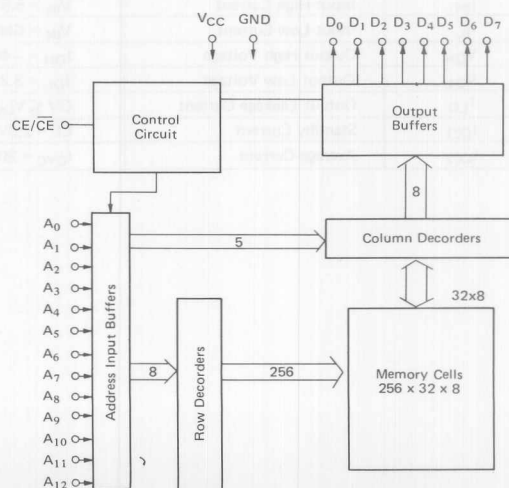
PIN CONNECTION



PIN NAMES

| | |
|----------------------------|-----------------------|
| $A_0 \sim A_{12}$ | Address inputs |
| $D_0 \sim D_7$ | Data outputs |
| CE/ $\overline{\text{CE}}$ | Chip enable input |
| V_{CC} | Power supply terminal |
| GND | Ground |

BLOCK DIAGRAM



TMM2366P

MAXIMUM RATINGS

| SYMBOL | ITEM | RATING | UNIT |
|-------------------|--|------------|----------|
| V_{CC} | Power Supply Voltage | -0.5 ~ 7.0 | V |
| V_{IN}, V_{OUT} | Input and Output Voltage | -0.5 ~ 7.0 | V |
| T_{OPR} | Operating Temperature | 0 ~ 70 | °C |
| T_{STRG} | Storage Temperature | -55 ~ 150 | °C |
| T_{SD} | Soldering Temperature Time | 260 • 10 | °C • sec |
| P_D | Power Dissipation ($T_a = 70^{\circ}\text{C}$) | 1.0 | W |

D.C. OPERATING CONDITIONS ($T_a = 0 \sim 70^{\circ}\text{C}$)

| SYMBOL | PARAMETER | CONDITIONS | MIN. | TYP. | MAX. | UNIT |
|----------|----------------------|------------|------|------|------------|------|
| V_{IH} | Input High Voltage | — | 2.0 | — | $V_{CC}+1$ | V |
| V_{IL} | Input Low Voltage | — | -0.5 | — | 0.8 | V |
| V_{CC} | Power Supply Voltage | — | 4.5 | 5.0 | 5.5 | V |

D.C. and OPERATING CHARACTERISTICS ($T_a = 0 \sim 70^{\circ}\text{C}$)

| SYMBOL | PARAMETER | CONDITIONS | MIN. | MAX. | UNIT |
|-----------|------------------------|---|------|------|---------------|
| I_{IH} | Input High Current | $V_{IN} = 5.5\text{V}$ | — | 10 | μA |
| I_{IL} | Input Low Current | $V_{IN} = \text{GND}$ | — | -10 | μA |
| V_{OH} | Output High Voltage | $I_{OH} = -400\mu\text{A}$ | 2.4 | — | V |
| V_{OL} | Output Low Voltage | $I_{OL} = 3.2\text{mA}$ | — | 0.4 | V |
| I_{LO} | Output Leakage Current | $0\text{V} \leq V_{OUT} \leq V_{CC}$ | -10 | 10 | μA |
| I_{CC1} | Standby Current | $\overline{\text{CE}} = 2.0\text{V}, \text{CE} = 0.8\text{V}$ | — | 25 | mA |
| I_{CC2} | Average Current | $t_{CYC} = 200\text{ns}, I_{OUT} = 0\text{mA}$ | — | 100 | mA |

A.C. CHARACTERISTICS ($T_a = 0 \sim 70^\circ\text{C}$, $V_{CC} = 5V \pm 10\%$)

| SYMBOL | PARAMETER | MIN. | MAX. | UNIT |
|-----------|---|------|------|------|
| t_{ACC} | Access Time | — | 200 | ns |
| t_{CE} | Output Delay Time from CE/\overline{CE} | — | 200 | ns |
| t_{OD} | Output Turn off Delay | — | 60 | ns |
| t_{CYC} | Cycle Time | 200 | — | ns |

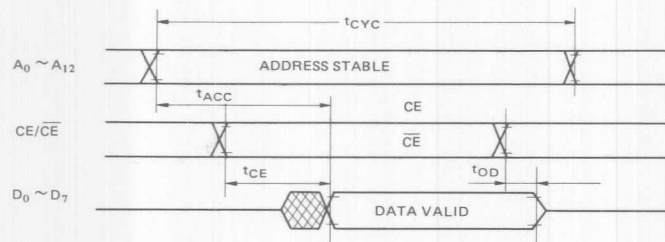
A.C. TEST CONDITIONS

- Output Load : 1TTL Gate + 100pF
- Input Rise and Fall Times (10% ~ 90%) : 5 ns
- Input Pulse Levels : 0.8 ~ 2.2V
- Timing Measurement Reference Levels : Input; 1V and 2.0V
Output; 0.8V and 2.0V

CAPACITANCE ($T_a = 25^\circ\text{C}$, $f = 1\text{MHz}$)

| SYMBOL | PARAMETER | CONDITIONS | MIN. | MAX. | UNIT |
|-----------|--------------------|-----------------------------|------|------|------|
| C_{IN} | Input Capacitance | $V_{IN} = \text{A.C. GND}$ | — | 8 | pF |
| C_{OUT} | Output Capacitance | $V_{OUT} = \text{A.C. GND}$ | — | 10 | pF |

Note: This parameter is periodically sampled and is not 100% tested.

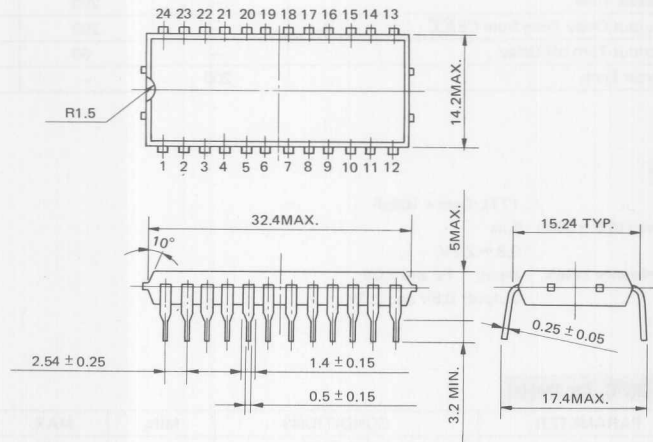
TIMING WAVEFORMS**POWER ON**

The TMM2366 has a self substrate-bias generator internally. So a minimum 100 μs time delay is

required after the application of V_{CC} (4.5 ~ 5.5V) before proper device operation is achieved.

TMM2366P

OUTLINE DRAWING



Note : Each lead pitch is 2.54mm. All leads are located within 0.25mm of their true longitudinal position with respect to No.1 and No.24 leads.

Note: Toshiba does not assume any responsibility for use of any circuitry described; no circuit patent licenses are implied, and Toshiba reserves the right, at any time without notice, to change said circuitry.
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TOSHIBA MOS MEMORY PRODUCTS

128K BIT (16K WORD × 8 BIT) MASK ROM
N-CHANNEL SILICON GATE

TMM23128P

DESCRIPTION

The TMM23128P is a 131,072 bit read only memory organized as 16,384 words by 8 bits with low bit cost, thus being suitable for use in program memory for microprocessor and character generator.

The TMM23128P is fully compatible with a 128K bits EPROM TMM27128D, so completely replace EPROM socket.

The TMM23128P also features an automatic

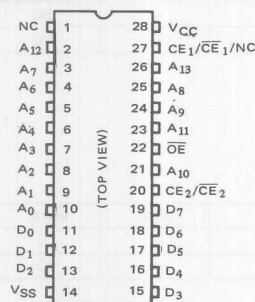
standby power mode. When deselected by Chip Enable (CE_1 , $2/\overline{CE}_1$, 2), the operating current is reduced from 80mA (Max.) to 20mA (Max.). Output Enable (\overline{OE}) is effective in preventing data confliction of a common bus line. The TMM23128P is fabricated with ion implanted N-channel silicon gate technology. The TMM23128P is moulded in a 28 pin standard plastic package, 0.6 inch in width.

FEATURES

- Fully Static Operation
- 16,384 word x 8 bit Structure
- Single 5V Power Supply
- $t_{ACC} = 200ns$ Max.
- $T_{opr} = 0 \sim 70^\circ C$
- $I_{CC\ ope} = 80mA$ Max.
- $I_{CC\ sby} = 20mA$ Max.

- Input and Output TTL Compatible
- Three State Outputs
- Programmable Chip Enable
- Pin Compatible with EPROM TMM27128D
- 28 pin 600 mil. width DIP Plastic Package

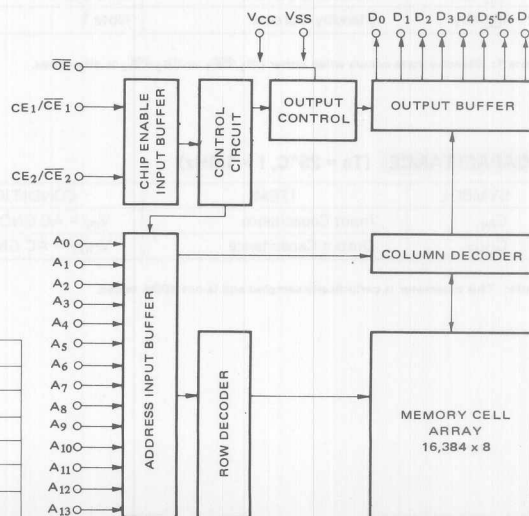
PIN CONNECTION



PIN NAMES

| | |
|--|---------------------|
| A ₀ ~ A ₁₃ | Address Inputs |
| D ₀ ~ D ₇ | Data Outputs |
| CE ₁ ~ 2/ \overline{CE}_1 ~ 2 | Chip Enable Inputs |
| \overline{OE} | Output Enable Input |
| NC | No Connection |
| V _{CC} | 5V Power Supply |
| V _{SS} | Ground |

BLOCK DIAGRAM



TMM23128P

MAXIMUM RATINGS

| SYMBOL | ITEM | RATING | UNIT |
|------------------------------------|-------------------------------|------------|----------|
| V _{CC} | Power Supply Voltage | -0.5 ~ 7.0 | V |
| V _{IN} , V _{OUT} | Input and Output Voltage | -0.5 ~ 7.0 | V |
| P _D | Power Dissipation (Ta = 70°C) | 1.0 | W |
| T _{OPR} | Operating Temperature | 0 ~ 70 | °C |
| T _{STG} | Storage Temperature | -55 ~ 150 | °C |
| T _{SOLDER} | Soldering Temperature · Time | 260 · 10 | °C · sec |

D.C. OPERATING CONDITIONS (Ta = 0 ~ 70°C)

| SYMBOL | ITEM | MIN. | MAX. | UNIT |
|-----------------|----------------------|------|---------------------|------|
| V _{CC} | Power Supply Voltage | 4.5 | 5.5 | V |
| V _{IH} | Input High Voltage | 2.2 | V _{CC} + 1 | V |
| V _{IL} | Input Low Voltage | -0.5 | 0.8 | V |

D.C. AND OPERATING CHARACTERISTICS (Ta = 0 ~ 70°C)

| SYMBOL | ITEM | CONDITIONS | MIN. | MAX. | UNIT |
|---------------------|------------------------|---|------|------|------|
| I _{IN} | Input Current | 0V ≤ V _{IN} ≤ V _{CC} | — | ±10 | μA |
| I _{LO} | Output Leakage Current | 0V ≤ V _{OUT} ≤ V _{CC} | — | ±10 | μA |
| I _{OH} | Output High Current | V _{OH} = 2.4V | -400 | — | μA |
| I _{OL} | Output Low Current | V _{OL} = 0.4V | 3.2 | — | mA |
| I _{CC ope} | Operating Current | Min. Cycle | — | 80 | mA |
| I _{CC sby} | Standby Current | Note 1 | — | 20 | mA |

Note 1: Standby state occurs when either CE₁/CE₁ or CE₂/CE₂ is disabled.

CAPACITANCE (Ta = 25°C, f = 1MHz)

| SYMBOL | ITEM | CONDITIONS | MIN. | MAX. | UNIT |
|------------------|--------------------|---------------------------|------|------|------|
| C _{IN} | Input Capacitance | V _{IN} = AC GND | — | 8 | pF |
| C _{OUT} | Output Capacitance | V _{OUT} = AC GND | — | 10 | pF |

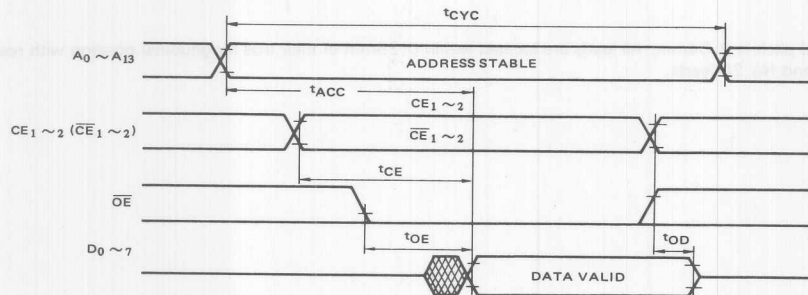
Note: This parameter is periodically sampled and is not 100% tested.

A.C. CHARACTERISTICS ($T_a = 0 \sim 70^\circ\text{C}$, $V_{CC} = 5V \pm 10\%$)

| SYMBOL | ITEM | MIN. | MAX. | UNIT |
|-----------|---|------|------|------|
| t_{ACC} | Access Time | — | 200 | ns |
| t_{CE} | Output Delay Time from $CE_{1\sim 2}/\overline{CE}_{1\sim 2}$ | — | 200 | ns |
| t_{OE} | Output Delay Time from \overline{OE} | — | 70 | ns |
| t_{OD} | Output Turn Off Delay | — | 60 | ns |
| t_{CYC} | Cycle Time | 200 | — | ns |

AC Test Conditions

- Output Load : 1 TTL + 100pF
- Input Rise and Fall Times (10% to 90%) : 5 ns
- Input Pulse Levels : 0.6V to 2.4V
- Timing Measurement Reference Levels : Input : 0.8V and 2.2V
Output : 0.8V and 2.0V

TIMING WAVEFORMS

Note:

- 1) t_{CE} specifies the time interval of $CE_{1\sim 2}$ ($\overline{CE}_{1\sim 2}$) to become active until it is actually being output.
- 2) t_{OD} is specified from \overline{OE} or CE , whichever occurs first.

APPLICATION INFORMATION

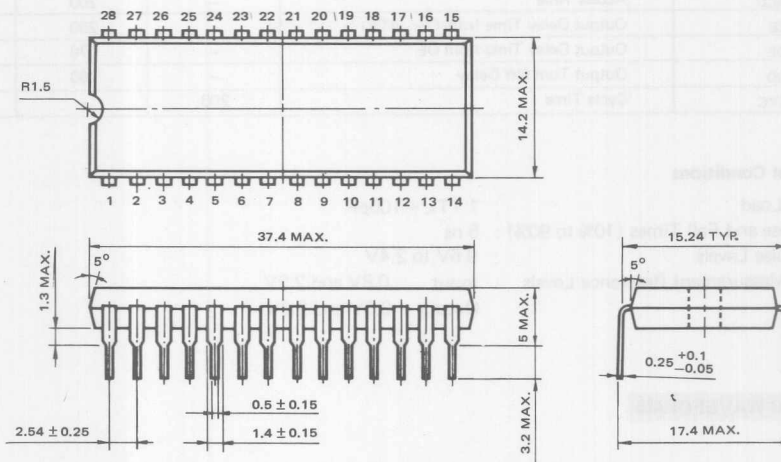
TMM23128P has self substrate-bias generator internally. So a minimum 100 μ s time delay is

required after the application of V_{CC} (4.5V to 5.5V) before proper device operation is achieved.

TMM23128P

OUTLINE DRAWINGS

Unit in mm



Note : Each lead pitch is 2.54mm. All leads are located within 0.25mm of their true longitudinal position with respect to No.1 and No.28 leads.

Note: Toshiba does not assume any responsibility for use of any circuitry described; no circuit patent licenses are implied, and Toshiba reserves the right, at any time without notice, to change said circuitry.

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TOSHIBA MOS MEMORY PRODUCTS

256K BIT (32K WORD × 8 BIT) MASK ROM
N-CHANNEL SILICON GATE

TMM23256P

DESCRIPTION

The TMM23256P is a 262,144 bit read only memory organized as 32,768 words by 8 bits with a low bit cost, thus being most suitable for use in character generator.

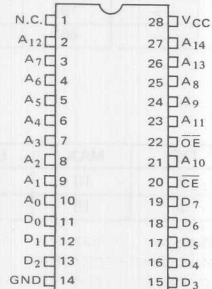
Consisting of static memory cells and clocked peripheral circuitry, the TMM23256P provides a high speed and low power dissipation (access time 150ns, operating current 40mA).

The TMM23256P also features an automatic standby power mode. When deselected by Chip Enable (\overline{CE}), the operating current is reduced from 40mA to

FEATURES

- Single 5V Power Supply
- Fast Access Time : 150ns (Max.)
- Low Power Dissipation
 - Average Current : 40mA (Max.)
 - Standby Current : 10mA (Max.)
- Inputs protected : All Inputs have Protection Against Static Charge

PIN CONNECTION



PIN NAMES

| | |
|----------------------------------|-----------------------|
| A ₀ ~ A ₁₄ | Address Inputs |
| D ₀ ~ D ₇ | Data Outputs |
| \overline{OE} | Output Enable Input |
| \overline{CE} | Chip Enable Input |
| N.C. | No Connection |
| V _{CC} | Power Supply Terminal |
| GND | Ground |

10mA. Output Enable (\overline{OE}) is effective in preventing data confliction on a common bus line.

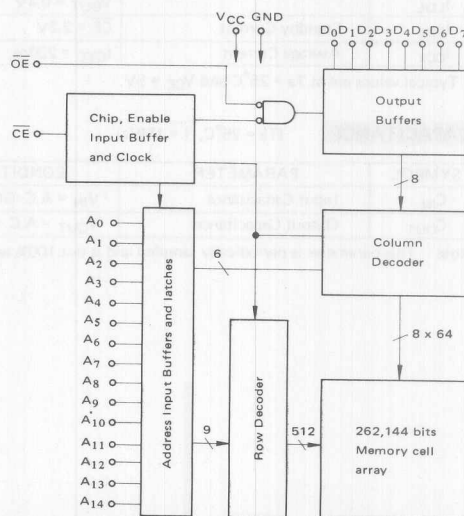
The TMM23256P uses the address latch system that the falling edge of \overline{CE} latches all inputs except for \overline{OE} , thus can be easily connected to a system where address and data buses are commonly used.

The TMM23256P is fabricated with ion implanted N-channel silicon gate technology. This technology allows a production on high performance.

The TMM23256P is moulded in a 28 pin standard plastic package, 0.6 inch in width.

- Edge Enabled Operation : \overline{CE}
- Output Buffer Control : \overline{OE}
- Input and Output : TTL Compatible
- Three State Outputs : Wired OR Capability
- 28 pin Standard Plastic DIP

BLOCK DIAGRAM



TMM23256P

MAXIMUM RATINGS

| SYMBOL | ITEM | RATING | UNIT |
|------------------------------------|-------------------------------|------------|----------|
| V _{CC} | Power Supply Voltage | -0.5 ~ 7.0 | V |
| V _{IN} , V _{OUT} | Input and Output Voltage | -0.5 ~ 7.0 | V |
| T _{OPR} | Operating Temperature | 0 ~ 70 | °C |
| T _{STRG} | Storage Temperature | -55 ~ 150 | °C |
| T _{SOLDER} | Soldering Temperature - Time | 260 · 10 | °C · sec |
| P _D | Power Dissipation (Ta = 70°C) | 1.0 | W |

D.C. OPERATING CONDITIONS (Ta = 0 ~ 70°C)

| SYMBOL | PARAMETER | CONDITIONS | MIN. | TYP. | MAX. | UNIT |
|-----------------|----------------------|------------|------|------|---------------------|------|
| V _{IH} | Input High Voltage | — | 2.2 | — | V _{CC} + 1 | V |
| V _{IL} | Input Low Voltage | — | -0.5 | — | 0.8 | V |
| V _{CC} | Power Supply Voltage | — | 4.5 | 5.0 | 5.5 | V |

D.C. and OPERATING CHARACTERISTICS (Ta = 0 ~ 70°C)

| SYMBOL | PARAMETER | CONDITIONS | MIN. | TYP. | MAX. | UNIT |
|------------------|------------------------|--|------|-------|------|------|
| I _{IH} | Input High Current | V _{IN} = 5.5V | — | 0.05 | 10 | μA |
| I _{IL} | Input Low Current | V _{IN} = GND | — | -0.05 | -10 | μA |
| V _{OH} | Output High Voltage | I _{OH} = -400 μA | 2.4 | 3.3 | — | V |
| V _{OL} | Output Low Voltage | I _{OL} = 3.2mA | — | 0.3 | 0.4 | V |
| I _{LOH} | Output Leakage Current | V _{OUT} = 5.5V CE = 2.2V or | — | 0.05 | 10 | μA |
| I _{LOL} | | V _{OUT} = 0.4V OE = 2.2V | — | -0.1 | -20 | μA |
| I _{CC1} | Standby Current | CE = 2.2V | — | — | 10 | mA |
| I _{CC2} | Average Current | t _{CYC} = 230ns, I _{OUT} = 0mA | — | — | 40 | mA |

- Typical values are at Ta = 25°C and V_{CC} = 5V.

CAPACITANCE (Ta = 25°C, f = 1MHz)

| SYMBOL | PARAMETER | CONDITIONS | MIN. | TYP. | MAX. | UNIT |
|------------------|--------------------|-----------------------------|------|------|------|------|
| C _{IN} | Input Capacitance | V _{IN} = A.C. GND | — | 5 | 10 | pF |
| C _{OUT} | Output Capacitance | V _{OUT} = A.C. GND | — | 8 | 15 | pF |

Note : This parameter is periodically sampled and is not 100% tested.

A.C. CHARACTERISTICS

($T_a = 0 \sim 70^\circ\text{C}$, $V_{CC} = 5V \pm 10\%$)

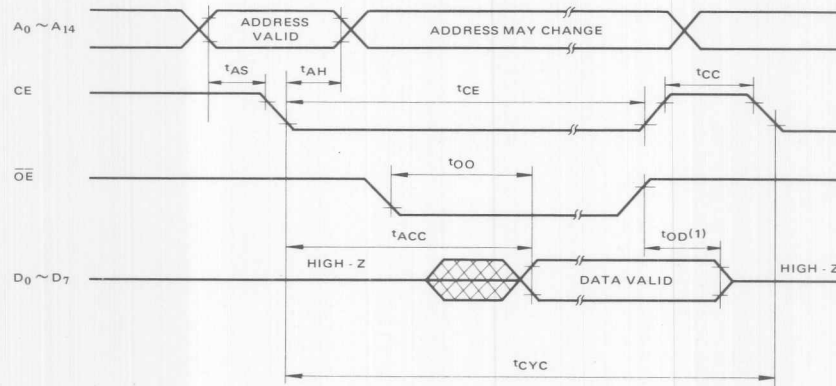
| SYMBOL | PARAMETER | CONDITIONS | MIN. | TYP. | MAX. | UNIT |
|-----------|--|--|------|------|------|------|
| t_{CE} | \overline{CE} pulse width | — | 150 | — | — | ns |
| t_{AS} | Address Setup Time | — | 0 | — | — | ns |
| t_{AH} | Address Hold Time | — | 30 | — | — | ns |
| t_{ACC} | Access Time | — | — | — | 150 | ns |
| t_{OO} | Output Delay Time form \overline{OE} | — | — | — | 70 | ns |
| t_{OD} | Output Turn off Delay | — | — | — | 70 | ns |
| t_{CC} | \overline{CE} off Time | — | 70 | — | — | ns |
| t_{CYC} | Cycle Time | $t_{AS} = 0\text{ns}$, t_r , $t_f = 5\text{ns}$ | 230 | — | — | ns |

- Typical values are at $T_a = 25^\circ\text{C}$ and $V_{CC} = 5V$.

A.C. TEST CONDITIONS

- Output Load : 1TTL Gate + 100pF
- Input Rise and Fall Times (10% ~ 90%) : 5ns
- Input Pulse Levels : 0.8 ~ 2.4V
- Timing Measurement Reference Levels : Input ; 1V and 2.2V
Output ; 0.8V and 2.0V

TIMING WAVEFORMS



Note (1) t_{OD} is specified from \overline{OE} or \overline{CE} , whichever occurs first.

TMM23256P


OPERATION INFORMATION

The TMM23256P has two control functions.

The chip enable (\overline{CE}) controls the operation power and should be used for device selection. The falling edge of the \overline{CE} will activate the device and latch the addresses. The output enable (\overline{OE}) control the out-

put buffers, independent of device selection. Assuming that $\overline{OE} = V_{IL}$, the output data is valid at the outputs after t_{ACC} (150ns) from the falling edge of the \overline{CE} .

The operation modes of the TMM23256P are listed in the following table.

| MODE | \overline{CE} | ADDRESS | \overline{OE} | OUTPUT | POWER |
|-----------------|---|---------|-----------------|----------------|---------|
| Standby | H | * | * | High Impedance | Standby |
| Latch |  | Valid | * | High Impedance | — |
| Read | L | ** | L | Data Out | Active |
| Output Deselect | L | * | H | High Impedance | Active |

Note * : Don't care

** : Address may change after t_{AH} .



APPLICATION INFORMATION

1. POWER SUPPLY DECOUPLING

The operating current I_{CC} waveforms for TMM 23256P are shown in Fig. 1, 2.

The TMM23256P is a clocked device, so the transient current peaks are produced on the \overline{CE} transition and \overline{CE} active level.

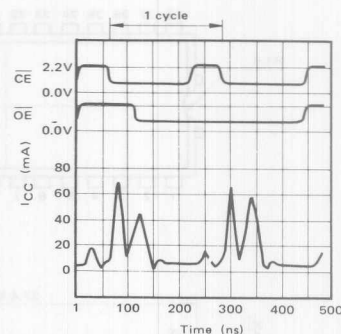
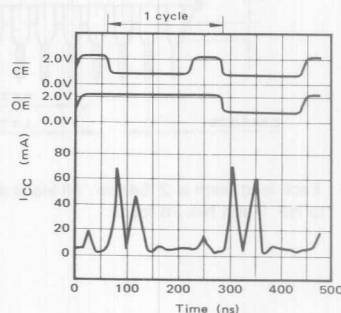
The I_{CC} current transients require adequate decoupling of V_{CC} power supply.

2. POWER ON

The TMM23256P requires initialization prior to normal operation. Two initialization methods are as follows:

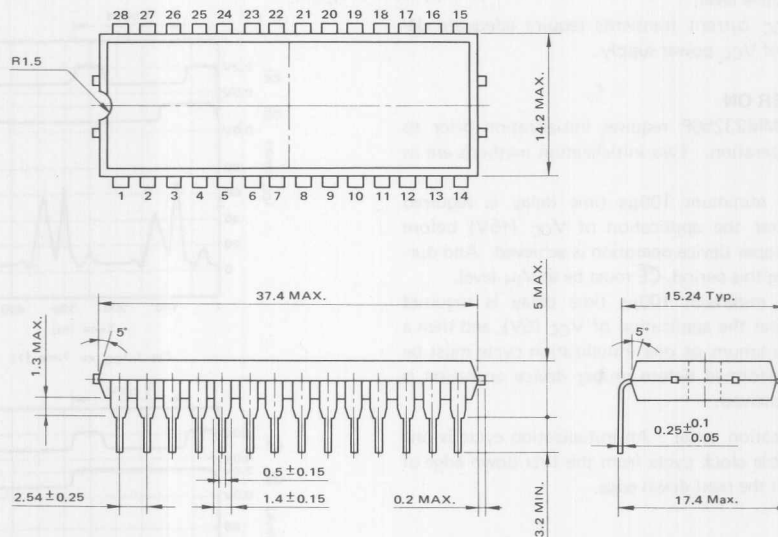
- (1) A minimum $100\mu s$ time delay is required after the application of V_{CC} (+5V) before proper device operation is achieved. And during this period, \overline{CE} must be at V_{IH} level.
- (2) A minimum $100\mu s$ time delay is required after the application of V_{CC} (5V), and then a minimum of one initialization cycle must be performed before proper device operation is achieved.

Initialization cycle : An initialization cycle is one Chip Enable clock cycle from the first down edge of the \overline{CE} till the next down edge.

Fig. 1 I_{CC} vs. Time (1)Fig. 2 I_{CC} vs. Time (2)

TMM23256P

Unit : mm



Note : Each lead pitch is 2.54mm. All leads are located within 0.25mm of their true longitudinal position with respect to No.1 and No.28 leads.

Note: Toshiba does not assume any responsibility for use of any circuitry described; no circuit patent licenses are implied, and Toshiba reserves the right, at any time without notice, to change said circuitry.

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CMOS Mask Read Only Memories

SAUNDERS WHO HAS BEEN SIGNED

TOSHIBA MOS MEMORY PRODUCTS

64K BIT (8K WORD × 8 BIT) CMOS MASK ROM
SILICON GATE CMOS

TC5364P

DESCRIPTION

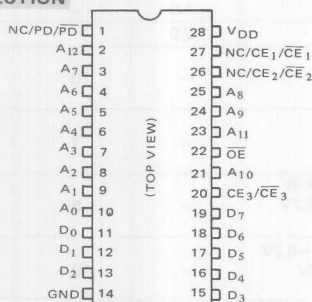
The TC5364P is a 65,536 bit read only memory organized as 8,192 words by 8 bits with a low bit cost, thus being suitable for use in program memory of microprocessor and character generator. The TC5364P using CMOS technology is most suitable for low power applications such as battery operated system.

The TC5364P is asynchronous type ROM which is consisting of address latch circuit, static memory

FEATURES

- Single Power Supply: 5V
- Access Time: 250 ns
- Low Power Dissipation
 - Operating Current: 7mA (Max.)
 - Standby Current: 20μA (Max.)
- Wide Operating Temperature Range: -40 ~ 85°C
- Pin Compatible with 64K EPROM TMM2764 and NMOS ROM TMM2364/2365

PIN CONNECTION



PIN NAMES

| | |
|-------------------|---------------------|
| $A_0 \sim A_{12}$ | Address inputs |
| $D_0 \sim D_7$ | Data outputs |
| $CE_1 \sim CE_3$ | Chip enable inputs |
| P_D | Power down input |
| OE | Output enable input |
| NC | No connection |
| V_{DD} | Power Supply |
| GND | Ground |

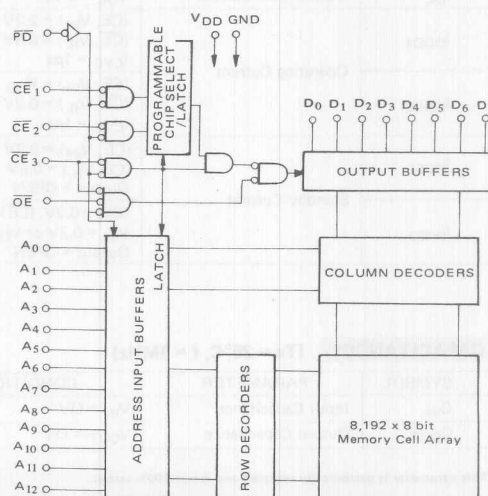
cells and clocked peripheral circuitry. The falling edge of \overline{CE}_3 (or rising edge of CE_3) latches all inputs except for OE and P_D/P_D .

The TC5364P has a P_D/P_D (optional) input for device power saving, and also has three programmable chip enable inputs ($CE_1 \sim 3/\overline{CE}_1 \sim 3$) and one output enable input (OE) for fast memory access and output control.

The TC5364P is moulded in a 28 pin standard plastic package.

- Edge Enable Operation: CE_3/\overline{CE}_3
- Address Latch Type
- Programmable Power Saving Input P_D/P_D /NC
- Programmable Chip Select: CE_1 , CE_2 , CE_3 , Easy Memory Expansion
- All Inputs and Outputs: TTL Compatible
- Three State Outputs

BLOCK DIAGRAM



TC5364P

MAXIMUM RATINGS

| SYMBOL | ITEM | RATING | UNIT |
|-------------|------------------------------|-----------------|-------------------------------------|
| V_{DD} | Power Supply Voltage | $-0.5 \sim 7.0$ | V |
| V_{IN} | Input Voltage | $-0.5 \sim 7.0$ | V |
| V_{OUT} | Output Voltage | $0 \sim V_{DD}$ | V |
| P_D | Power Dissipation | 1.0 | W |
| T_{opr} | Operating Temperature | $-40 \sim 85$ | $^{\circ}\text{C}$ |
| T_{stg} | Storage Temperature | $-55 \sim 150$ | $^{\circ}\text{C}$ |
| T_{SOLDR} | Soldering Temperature - Time | $260 \cdot 10$ | $^{\circ}\text{C} \cdot \text{sec}$ |

D.C. OPERATING CONDITIONS ($T_a = -40 \sim 85^{\circ}\text{C}$)

| SYMBOL | PARAMETER | MIN. | MAX. | UNIT |
|----------|----------------------|------|----------------|------|
| V_{DD} | Power Supply Voltage | 4.5 | 5.5 | V |
| V_{IH} | Input High Voltage | 2.2 | $V_{DD} + 0.3$ | V |
| V_{IL} | Input Low Voltage | -0.3 | 0.8 | V |

D.C. and OPERATING CHARACTERISTICS ($T_a = -40 \sim 85^{\circ}\text{C}$, $V_{DD} = 5\text{V} \pm 10\%$)

| SYMBOL | PARAMETER | CONDITION | MIN. | MAX. | UNIT |
|------------|------------------------|---|------|-----------|---------------|
| I_{IN} | Input Leakage Current | $0\text{V} \leq V_{IN} \leq V_{DD}$ | — | ± 1.0 | μA |
| I_{LO} | Output Leakage Current | $0\text{V} \leq V_{OUT} \leq V_{DD}$ | — | ± 5.0 | μA |
| I_{OH} | Output High Current | $V_{OH} = 2.4\text{V}$ | -1.0 | — | mA |
| I_{OL} | Output Low Current | $V_{OL} = 0.4\text{V}$ | 2.0 | — | mA |
| I_{DDO1} | Operating Current | $(\text{CE}, V_{IH}) = 2.2\text{V}$ $(\text{CE}, V_{IL}) = 0.8\text{V}$ $t_{CYC} = 1\mu\text{s}$ | — | 10 | mA |
| I_{DDO2} | | $(\text{CE}, V_{IH}) = V_{DD} - 0.2\text{V}$ $(\text{CE}, V_{IL}) = 0.2\text{V}$ $t_{CYC} = 1\mu\text{s}$ | — | 7 | mA |
| I_{DDS1} | Standby Current | $(\text{CE}, V_{IH}) = 2.2\text{V}$ $\text{CE} = 0.8\text{V}$ $(\text{CE}, V_{IL}) = 0.8\text{V}$ $\text{CE} = 2.2\text{V}$ Output = OPEN | — | 5 | mA |
| I_{DDS2} | | $(\text{CE}) = 0.2\text{V}$, $(\text{CE}) = V_{DD} - 0.2\text{V}$ $V_{IN} = 0.2\text{V}$ or $V_{DD} - 0.2\text{V}$ Output = OPEN | — | 20 | μA |

CAPACITANCE* ($T_a = 25^{\circ}\text{C}$, $f = 1\text{MHz}$)

| SYMBOL | PARAMETER | CONDITIONS | MAX. | UNIT |
|-----------|--------------------|-----------------------|------|------|
| C_{IN} | Input Capacitance | $V_{IN} = 0\text{V}$ | 8 | pF |
| C_{OUT} | Output Capacitance | $V_{OUT} = 0\text{V}$ | 10 | pF |

* This parameter is periodically sampled and is not 100% tested.

A.C. CHARACTERISTICS (Ta = -40~85°C, VDD = 5V ± 10%)

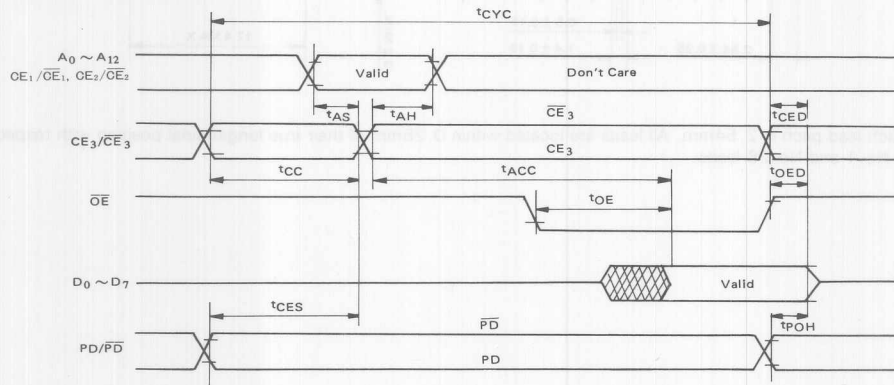
| SYMBOL | PARAMETER | MIN. | MAX. | UNIT |
|------------------|--|------|------|------|
| t _{ACC} | Chip Enable Access Time | — | 250 | ns |
| t _{OE} | Output Enable Access Time | — | 100 | ns |
| t _{AS} | Address Set up Time | 0 | — | ns |
| t _{AH} | Address Hold Time | 50 | — | ns |
| t _{CC} | Chip Enable Off Time | 90 | — | ns |
| t _{CES} | Chip Enable Setup Time from PD/ \overline{PD} | 90 | — | ns |
| t _{OED} | Output Disable Time from \overline{OE} | — | 90 | ns |
| t _{CED} | Output Disable Time from CE ₃ / \overline{CE}_3 | — | 90 | ns |
| t _{POH} | Output Hold Time from PD/ \overline{PD} | — | 90 | ns |
| t _{CYC} | Cycle Time | 350 | — | ns |

Note 1: Assumes that \overline{OE} delay time to CE₃/ \overline{CE}_3 ≥ t_{ACC} - t_{OE}

A.C. TEST CONDITIONS

- Output Load: 100pF + 1 TTL Gate
- Input Levels: V_{IL} = 0.6V, V_{IH} = 2.4V
- Timing Measurement Reference Levels
 - Input: 0.8V, 2.2V
 - Output: 0.8V, 2.2V
- Input Rise and Fall Time: 5 ns

TIMING WAVE FORMS



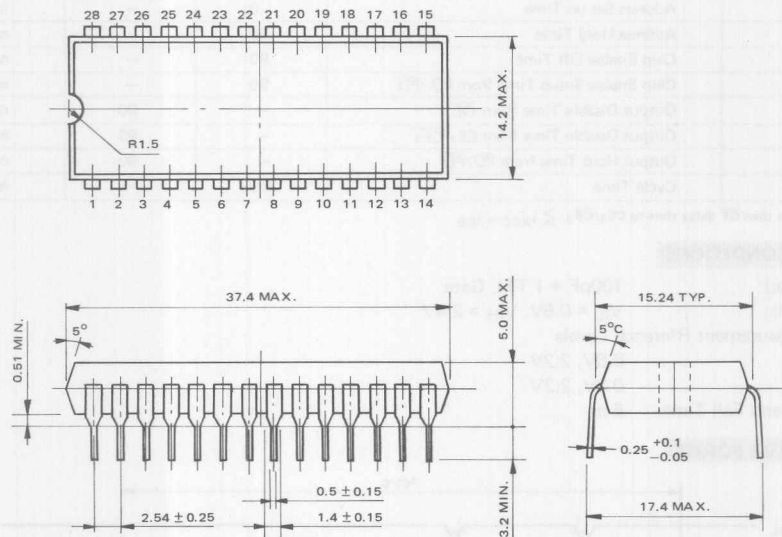
OPERATION MODE

| MODE | PD (\overline{PD}) | CE ₁ (\overline{CE}_1) | CE ₂ (\overline{CE}_2) | CE ₃ (\overline{CE}_3) | \overline{OE} | Outputs |
|-----------------|------------------------|---------------------------------------|---------------------------------------|---------------------------------------|-----------------|---------|
| Read | L(H) | H(L) | H(L) | H \overline{f} (L \overline{f}) | L | Valid |
| | H(L) | * | * | * | * | |
| Output Deselect | * | L(H) | * | * | * | High-Z |
| | * | * | L(H) | * | * | |
| | * | * | * | L(H) | * | |
| | * | * | * | * | H | |

Note: H: V_{IH}, L: V_{IL}, *: V_{IH} or V_{IL}

OUTLINE DRAWING

Unit: mm



Note : Each lead pitch is 2.54mm. All leads are located within 0.25mm of their true longitudinal position with respect to No.1 and No.28 leads.

Note: Toshiba does not assume any responsibility for use of any circuitry described; no circuit patent licenses are implied, and Toshiba reserves the right, at any time without notice, to change said circuitry.
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TOSHIBA MOS MEMORY PRODUCTS

64K BIT (8K WORD × 8 BIT) CMOS MASK ROM
SILICON GATE MOS

TC5365P
TC5365F

DESCRIPTION

The TC5365P/F is a 65,536 bit read only memory organized as 8,192 words by 8 bit with a low bit cost, thus being suitable for use in program memory of microprocessor, and in character generator. The TC5365P/F using CMOS technology is most suitable for low power applications where battery operation is

required.

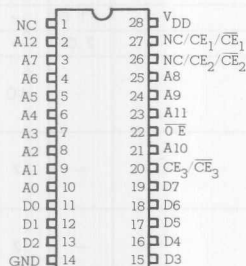
The TC5365P/F has three programmable chip enable input $\overline{CE}_1 \sim \overline{CE}_3 / \overline{CE}_1 \sim \overline{CE}_3$, for device selection and one output enable input (\overline{OE}) for fast memory access and output control.

FEATURES

- single 5V Power Supply
- Access Time : 250ns(Max.)
- Power Dissipation
Operating Current : 7mA(Max.)
Standby Current : 20 μ A(Max.)
- Pin Compatible with 64K EPROM TMM 2764D
- Full Static Operation

- Programmable Chip Enable
- All Inputs and Outputs : TTL Compatible
- Three State Outputs
- Package
Plastic DIP : TC5365P
Plastic FP : TC5365F

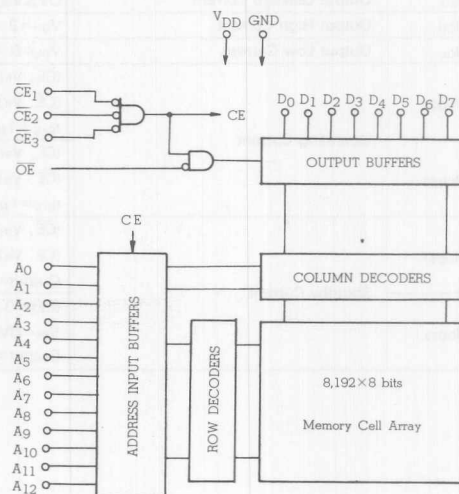
PIN CONNECTION (TOP VIEW)



PIN NAMES

| | |
|---|---------------------|
| $A_0 \sim A_{12}$ | Address Inputs |
| $D_0 \sim D_7$ | Data Outputs |
| NC | No connection |
| $\overline{CE}_1 \sim \overline{CE}_3 / \overline{CE}_1 \sim \overline{CE}_3$ | Chip enable inputs |
| \overline{OE} | Output enable input |
| V_{DD} | Power supply |
| GND | Ground |

BLOCK DIAGRAM



TC5365P TC5365F

MAXIMUM RATINGS

| SYMBOL | ITEM | RATING | UNITS |
|---------------------|----------------------------|-------------------|--------|
| V _{DD} | Power Supply Voltage | -0.5~7.0 | V |
| V _{IN} | Input Voltage | -0.5~7.0 | V |
| V _{OUT} | Output Voltage | 0~V _{DD} | V |
| P _D | Power Dissipation | 1.0/0.6* | W |
| T _{OPR} | Operating Temperature | -40~85 | °C |
| T _{STG} | Storage Temperature | -55~150 | °C |
| T _{SOLDER} | Soldering Temperature·Time | 260·10 | °C·sec |

NOTE : * Plastic FP

D. C. OPERATING CONDITIONS

(Ta = -40~85°C)

| SYMBOL | PARAMETER | MIN. | MAX. | UNIT |
|-----------------|----------------------|------|----------------------|------|
| V _{DD} | Power Supply Voltage | 4.5 | 5.5 | V |
| V _{IH} | Input High Voltage | 2.2 | V _{DD} +0.3 | V |
| V _{IL} | Input Low Voltage | -0.3 | 0.8 | V |

D. C. and OPERATING CHARACTERISTICS

(Ta = -40~85°C, V_{DD} = 5V ± 10%)

| SYMBOL | PARAMETER | CONDITIONS | MIN. | MAX. | UNIT |
|-------------------|------------------------|---|------|------|------|
| I _{IN} | Input Leakage Current | 0V ≤ V _{IN} ≤ V _{DD} | — | ±1.0 | μA |
| I _{LO} | Output Leakage Current | 0V ≤ V _{OUT} ≤ V _{DD} | — | ±5.0 | μA |
| I _{OH} | Output High Current | V _{OH} = 2.4V | -1.0 | — | mA |
| I _{OL} | Output Low Current | V _{OL} = 0.4V | 2.0 | — | mA |
| I _{DD01} | Operating Current | (CE, V _{IH}) = 2.2V (\overline{CE} , V _{IL}) = 0.8V t _{CYC} = 1μs | — | 10 | mA |
| I _{DD02} | | (CE, V _{IH}) = V _{DD} - 0.2V (\overline{CE} , V _{IL}) = 0.2V t _{CYC} = 1μs | — | 7 | mA |
| I _{DDS1} | Standby Current | (\overline{CE} , V _{IH}) = 2.2V (CE, V _{IL}) = 0.8V Output = OPEN | — | 2 | mA |
| I _{DDS2} | | (CE) = 0.2V, (\overline{CE}) = V _{DD} - 0.2V V _{IN} = 0V ~ V _{DD} Output = OPEN | — | 20 | μA |

A. C. CHARACTERISTICS

($T_a = -40 \sim 85^\circ\text{C}$, $V_{DD} = 5V \pm 10\%$)

| SYMBOL | PARAMETER | MIN. | MAX. | UNIT |
|-----------|---|------|------|------|
| t_{ACC} | Access Time | — | 250 | ns |
| t_{CE} | Chip Enable Access Time | — | 250 | ns |
| t_{OE} | Output Enable Access Time | — | 100 | ns |
| t_{CED} | Output Disable Time from $\overline{CE_1} \sim \overline{CE_3}$ | 0 | 90 | ns |
| t_{OED} | Output Disable Time from \overline{OE} | 0 | 90 | ns |
| t_{OH} | Output Hold Time | 0 | — | ns |
| t_{CYC} | Cycle Time | 250 | — | ns |

Note 1: Assumes that \overline{OE} delay to $\overline{CE_1} \sim \overline{CE_3} \geq t_{ACC} - t_{OE}$

Note 2: Output disable time (t_{CED} , t_{OED}) is specified from $\overline{CE_1} \sim \overline{CE_3}$, \overline{OE} whichever occurs first.

A. C. TEST CONDITIONS

Output Load

: 100pF + 1TTL

Input Levels

: $V_{IL} = 0.6V$, $V_{IH} = 2.4V$

Timing Measurement Reference Levels

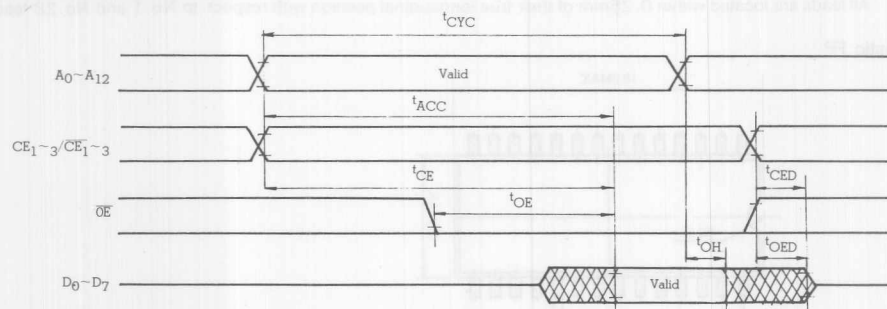
Input : 0.8V, 2.2V

Output : 0.8V, 2.2V

Input Rise and Fall Time

: 5ns

TIMING WAVEFORMS



CAPACITANCE

($T_a = 25^\circ\text{C}$, $f = 1\text{MHz}$)

| SYMBOL | PARAMETER | CONDITIONS | MAX. | UNIT |
|-----------|--------------------|----------------|------|------|
| C_{IN} | Input Capacitance | $V_{IN} = 0V$ | 8 | pF |
| C_{OUT} | Output Capacitance | $V_{OUT} = 0V$ | 10 | pF |

OPERATION MODE

H : V_{IH} , L : V_{IL} , * : V_{IH} or V_{IL}

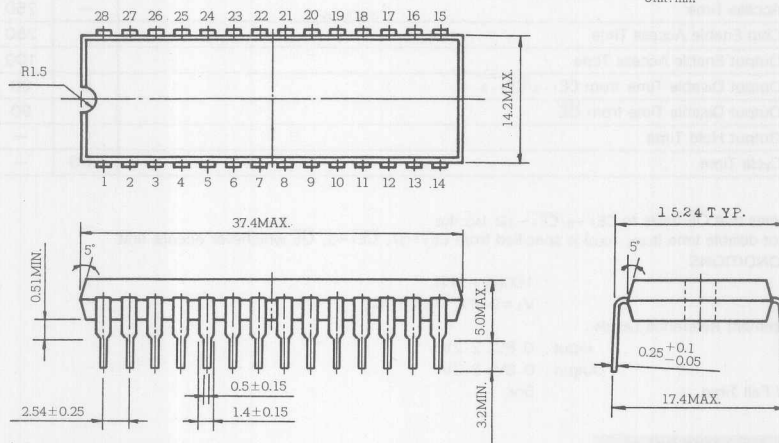
| MODE | $\overline{CE_1}(\overline{CE_1})$ | $\overline{CE_2}(\overline{CE_2})$ | $\overline{CE_3}(\overline{CE_3})$ | \overline{OE} | Outputs |
|---------------------|------------------------------------|------------------------------------|------------------------------------|-----------------|---------|
| Read | H(L) | H(L) | H(L) | L | Valid |
| Outputs Deselect | L(H) | * | * | * | High-Z |
| | * | L(H) | * | * | |
| | * | * | L(H) | * | |
| | * | * | * | H | |

TC5365P TC5365F

OUTLINE DRAWINGS

● Plastic DIP

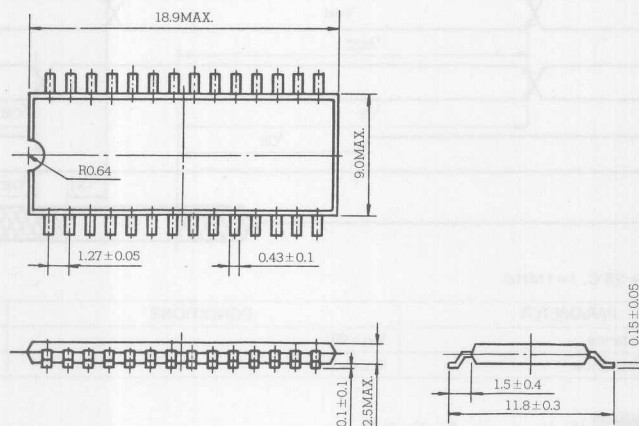
Unit:mm



NOTE : Each lead pitch is 2.54mm.

All leads are located within 0.25mm of their true longitudinal position with respect to No. 1 and No. 28 leads.

● Plastic FP



NOTE : Each lead pitch is 1.27mm.

All leads are located within 0.12mm of their true longitudinal position with respect to No. 1 and No. 28 leads.

Note : Toshiba does not assume any responsibility for use of any circuitry described ; no circuit patent licenses are implied, and Toshiba reserves the right, at any time without notice, to change said circuitry.

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TOSHIBA MOS MEMORY PRODUCTS

64K BIT (8K WORD × 8 BIT) CMOS MASK ROM
SILICON GATE CMOS

TC5366P

DESCRIPTION

The TC5366P is a 65,536 bit read only memory organized as 8,192 words by 8 bits with a low bit cost, thus being suitable for use in program memory of microprocessor and character generator.

The TC5366P using CMOS technology is most suitable for low power applications such as battery

operated system.

The TC5366P is an asynchronous type ROM and has a programmable chip enable input for device selection and device power saving.

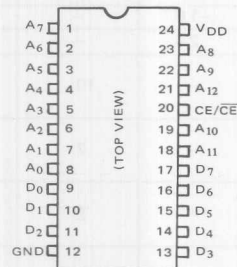
The TC5366P is moulded in a 24 pin standard plastic package.

FEATURES

- Single Power Supply: 5V
- Access Time: 250 ns
- Low Power Dissipation
 - Operating Current: 7mA (Max.)
 - Standby Current: 20μA (Max.)

- Fully Static Operation
- Programmable Chip Enable: CE/ $\overline{\text{CE}}$
- All Inputs and Outputs: TTL Compatible
- Three State Outputs

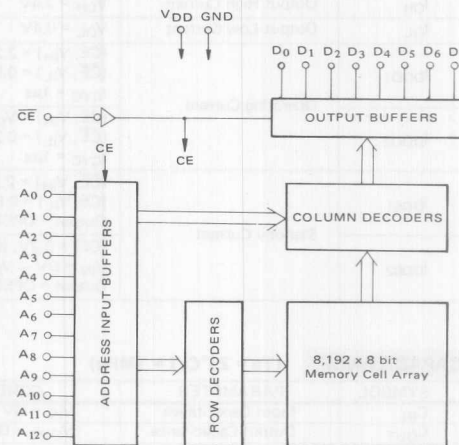
PIN CONNECTION



PIN NAMES

| | |
|----------------------------|-------------------|
| $A_0 \sim A_{12}$ | Address inputs |
| $D_0 \sim D_7$ | Data outputs |
| CE/ $\overline{\text{CE}}$ | Chip enable input |
| V_{DD} | Power supply |
| GND | Ground |

BLOCK DIAGRAM



MAXIMUM RATINGS

| SYMBOL | ITEM | RATING | UNIT |
|--------------|------------------------------|-----------------|-------------------------------------|
| V_{DD} | Power Supply Voltage | $-0.5 \sim 7.0$ | V |
| V_{IN} | Input Voltage | $-0.5 \sim 7.0$ | V |
| V_{OUT} | Output Voltage | $0 \sim V_{DD}$ | V |
| P_D | Power Dissipation | 1.0 | W |
| T_{opr} | Operating Temperature | $-40 \sim 85$ | $^{\circ}\text{C}$ |
| T_{stg} | Storage Temperature | $-55 \sim 150$ | $^{\circ}\text{C}$ |
| T_{SOLDER} | Soldering Temperature · Time | $260 \cdot 10$ | $^{\circ}\text{C} \cdot \text{sec}$ |

D.C. OPERATING CONDITIONS ($T_a = -40 \sim 85^{\circ}\text{C}$)

| SYMBOL | PARAMETER | MIN. | MAX. | UNIT |
|----------|----------------------|------|----------------|------|
| V_{DD} | Power Supply Voltage | 4.5 | 5.5 | V |
| V_{IH} | Input High Voltage | 2.2 | $V_{DD} + 0.3$ | V |
| V_{IL} | Input Low Voltage | -0.3 | 0.8 | V |

D.C. and OPERATING CHARACTERISTICS ($T_a = -40 \sim 85^{\circ}\text{C}$, $V_{DD} = 5V \pm 10\%$)

| SYMBOL | PARAMETER | CONDITIONS | MIN. | MAX. | UNIT |
|------------|------------------------|---|------|-----------|---------------|
| I_{IN} | Input Leakage Current | $0V \leq V_{IN} \leq V_{DD}$ | — | ± 1.0 | μA |
| I_{LO} | Output Leakage Current | $0V \leq V_{OUT} \leq V_{DD}$ | — | ± 0.5 | μA |
| I_{OH} | Output High Current | $V_{OH} = 2.4V$ | -1.0 | — | mA |
| I_{OL} | Output Low Current | $V_{OL} = 0.4V$ | 2.0 | — | mA |
| I_{DD01} | Operating Current | (\overline{CE} , V_{IH}) = 2.2V (\overline{CE} , V_{IL}) = 0.8V $t_{CYC} = 1\mu\text{s}$ | — | 10 | mA |
| I_{DD02} | | (\overline{CE} , V_{IH}) = $V_{DD} - 0.2V$ (\overline{CE} , V_{IL}) = 0.2V $t_{CYC} = 1\mu\text{s}$ | — | 7 | mA |
| I_{DDs1} | Standby Current | (\overline{CE} , V_{IH}) = 2.2V (\overline{CE} , V_{IL}) = 0.8V Output = OPEN | — | 2 | mA |
| I_{DDs2} | | (\overline{CE}) = 0.2V, (\overline{CE}) = $V_{DD} - 0.2V$ $V_{IN} = 0V \sim V_{DD}$ Output = OPEN | — | 20 | μA |

CAPACITANCE* ($T_a = 25^{\circ}\text{C}$, $f = 1\text{MHz}$)

| SYMBOL | PARAMETER | CONDITIONS | MAX. | UNIT |
|-----------|--------------------|----------------|------|------|
| C_{IN} | Input Capacitance | $V_{IN} = 0V$ | 8 | pF |
| C_{OUT} | Output Capacitance | $V_{OUT} = 0V$ | 10 | pF |

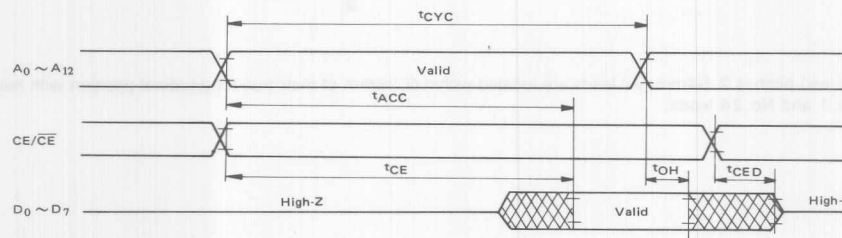
*This parameter is periodically sampled and is not 100% tested.

A.C. CHARACTERISTICS ($T_a = -40 \sim 85^\circ\text{C}$, $V_{DD} = 5V \pm 10\%$)

| SYMBOL | PARAMETER | MIN. | MAX. | UNIT |
|-----------|---|------|------|------|
| t_{ACC} | Access Time | — | 250 | ns |
| t_{CE} | Chip Enable Access Time | — | 250 | ns |
| t_{CED} | Output Disable Time from CE / \overline{CE} | 0 | 90 | ns |
| t_{OH} | Output Hold Time | 0 | — | ns |
| t_{CYC} | Cycle Time | 250 | — | ns |

A.C. TEST CONDITIONS

- Output Load: 100pF + 1 TTL
- Input Levels: $V_{IL} = 0.6V$, $V_{IH} = 2.4V$
- Timing Measurement Reference Levels
 - Input: 0.8V, 2.2V
 - Output: 0.8V, 2.2V
- Input Rise and Fall Time: 5ns

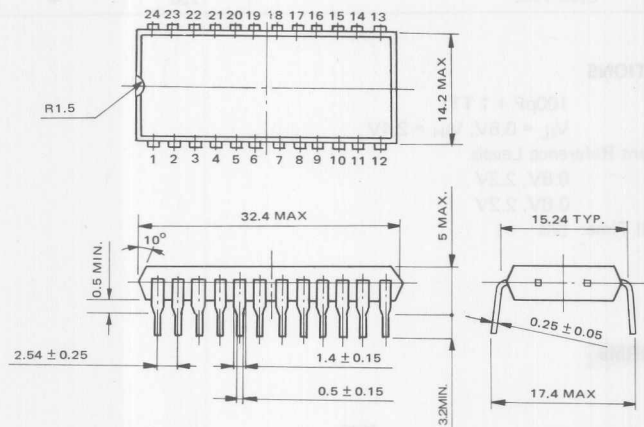
TIMING WAVE FORMS**OPERATION MODE**

| MODE | CE (\overline{CE}) | Output |
|-----------------|------------------------|--------|
| Read | H(L) | Valid |
| Output Deselect | L(H) | High-Z |

Note: H: V_{IH} , L: V_{IL}

TC5366P

OUTLINE DRAWINGS



Note : Each lead pitch is 2.54mm. All leads are located within 0.25mm of their true longitudinal position with respect to No.1 and No.24 leads.

Note: Toshiba does not assume any responsibility for use of any circuitry described; no circuit patent licenses are implied, and Toshiba reserves the right, at any time without notice, to change said circuitry.

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TOSHIBA MOS MEMORY PRODUCTS

256K BIT (32K WORD × 8 BIT) CMOS MASK ROM
SILICON GATE MOS

TC53257P
TC53257F

DESCRIPTION

The TC53257P/F is a 262,144 bit read only memory organized as 32,768 words by 8 bits with a low bit cost, this being suitable for use in program memory of microprocessor, and in character generator. The TC53257P/F using CMOS technology is most suitable for low power applications where bat-

tery operation is required.

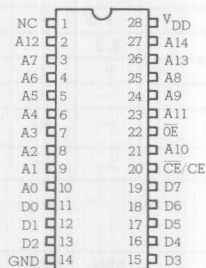
The TC53257P/F has one programmable chip enable input \overline{CE}/CE , for device selection and one output enable input (\overline{OE}) for fast memory access and output control.

FEATURES

- Single 5V Power Supply
- Access Time : 200ns(Max.)
- Power Dissipation
Operating Current : 25mA(Max.)
Standby Current : 20 μ A(Max.)
- Pin Compatible with 256K EPROM TC57256D
- Full Static Operation

- Programmable Chip Enable
- All Inputs and Outputs : TTL Compatible
- Three State Outputs
- Package
Plastic DIP : TC53257P
Plastic FP : TC53257F

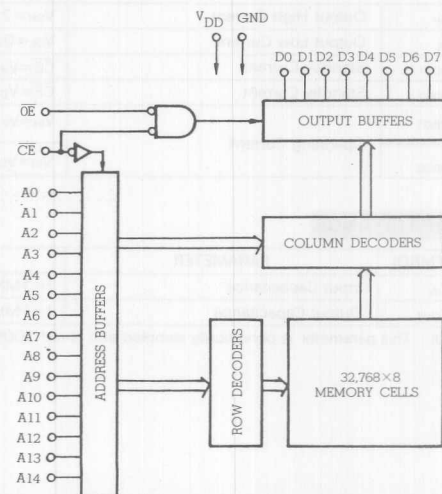
PIN CONNECTION (TOP VIEW)



PIN NAMES

| | |
|---------------------------------|---------------------|
| A ₀ ~A ₁₄ | Address Inputs |
| D ₀ ~D ₇ | Data Outputs |
| NC | No connection |
| \overline{CE}/CE | Chip enable input |
| \overline{OE} | Output enable input |
| V _{DD} | Power supply |
| GND | Ground |

BLOCK DIAGRAM



TC53257P

TC53257F

MAXIMUM RATINGS

| SYMBOL | ITEM | RATING | UNITS |
|--------------|----------------------------|-------------|--------|
| V_{DD} | Power Supply Voltage | -0.5~7.0 | V |
| V_{IN} | Input Voltage | -0.5~7.0 | V |
| V_{OUT} | Output Voltage | 0~ V_{DD} | V |
| P_D | Power Dissipation | 1.0/0.6* | W |
| T_{STG} | Storage Temperature | -55~150 | °C |
| T_{OPR} | Operating Temperature | -40~85 | °C |
| T_{SOLDER} | Soldering Temperature·Time | 260·10 | °C·sec |

Note : *Plastic FP

D. C. OPERATING CONDITINS

($T_a = -40 \sim 85^\circ\text{C}$)

| SYMBOL | PARAMETER | MIN. | TYP. | MAX. | UNIT |
|----------|----------------------|------|------|--------------|------|
| V_{DD} | Power Supply Voltage | 4.5 | 5.0 | 5.5 | V |
| V_{IH} | Input High Voltage | 2.2 | — | $V_{DD}+0.3$ | V |
| V_{IL} | Input Low Voltage | -0.3 | — | 0.8 | V |

D. C. and OPERATING CHARACTERISTICS

($T_a = -40 \sim 85^\circ\text{C}$, $V_{DD} = 5\text{V} \pm 10\%$)

| SYMBOL | PARAMETER | CONDITIONS | MIN. | MAX. | UNIT |
|------------|------------------------|---|------|-----------|---------------|
| I_{IL} | Input Leakage Current | $V_{IN} = 0\text{V} \sim V_{DD}$ | — | ± 1.0 | μA |
| I_{LO} | Output Leakage Current | $\overline{CE} = V_{IH}$ or $\overline{OE} = V_{IH}$ $V_{OUT} = 0\text{V} \sim V_{DD}$ | — | ± 5.0 | μA |
| I_{OH} | Output High Current | $V_{OH} = 2.4\text{V}$ | -1.0 | — | mA |
| I_{OL} | Output Low Current | $V_{OL} = 0.4\text{V}$ | 3.2 | — | mA |
| I_{DDS1} | Standby Current | $\overline{CE} = V_{IH}$ $\overline{CE} = V_{IL}$ | — | 2 | mA |
| I_{DDO1} | Standby Current | $\overline{CE} = V_{DD} - 0.2\text{V}$, $\overline{CE} = 0.2\text{V}$ | — | 20 | μA |
| I_{DDO1} | Operating Current | $V_{IH} = V_{IH}/V_{IL}$, $t_{CYCLE} = 200\text{ns}$ | — | 40 | mA |
| I_{DDO2} | | $V_{IN} = V_{DD} - 0.2\text{V}/0.2\text{V}$, $t_{CYCLE} = 200\text{ns}$ | — | 25 | mA |

CAPACITANCE

| SYMBOL | PARAMETER | CONDITIONS | MIN. | MAX. | UNIT |
|-----------|--------------------|--|------|------|------|
| C_{IN} | Input Capacitance | $f = 1\text{MHz}$, $T_a = 25^\circ\text{C}$ | — | 8 | pF |
| C_{OUT} | Output Capacitance | $f = 1\text{MHz}$, $T_a = 25^\circ\text{C}$ | — | 10 | pF |

Note : This parameter is periodically sampled and is not 100% tested.

A. C. CHARACTERISTICS

(Ta = -40 ~ 85°C, VDD = 5V ± 10%)

| SYMBOL | PARAMETER | MIN. | MAX. | UNIT |
|-------------------------------------|------------------------------------|------|------|------|
| t _{CYC} | Cycle Time | 200 | — | ns |
| t _{ACC} | Access Time | — | 200 | ns |
| t _{CE} | Chip Enable Access Time from CE/CE | — | 200 | ns |
| t _{OE} | Output Enable Access Time from OE | — | 70 | ns |
| t _{CED} , t _{OED} | Output Disable Time from CE/CE, OE | 0 | 60 | ns |
| t _{OH} | Output Hold Time | 0 | — | ns |

A. C. TEST CONDITIONS

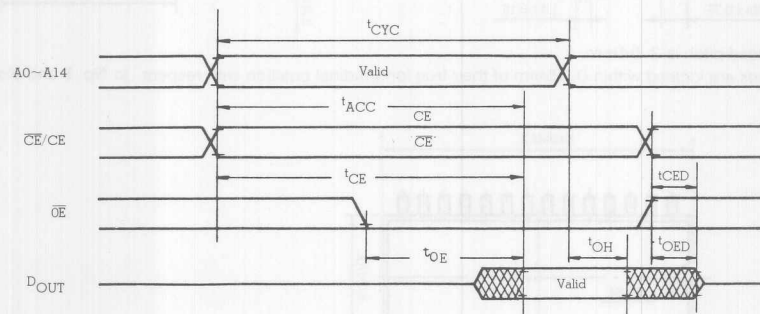
Output Load : 100pF + 1TTL
Input Levels : 0.6V, 2.4V

Timing Measurement Reference Levels

Input : 0.8V, 2.2V
Output : 0.8V, 2.2V

Input Rise and Fall Time : 5ns

TIMING WAVEFORMS



OPERATION MODE

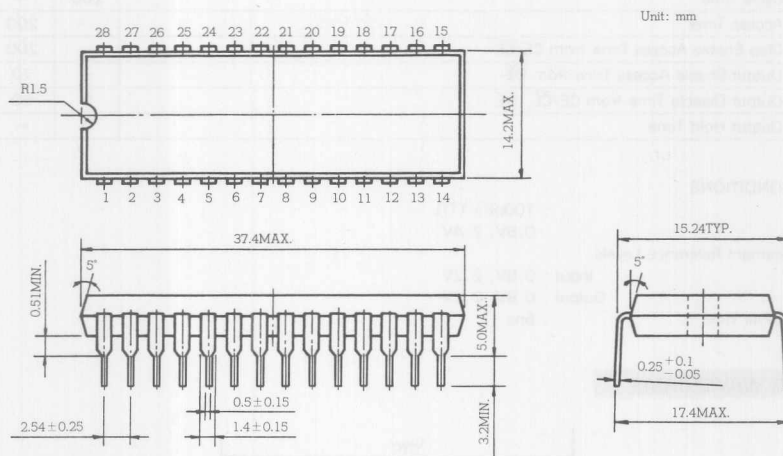
H : V_{IH}, L : V_{IL}, * : V_{IH} or V_{IL}

| MODE | CE(CE) | OE | A ₀ ~14 | Outputs | Power |
|-----------------|--------|----|--------------------|----------|-----------|
| Read | L(H) | L | Valid | Data out | Operating |
| Output Deselect | L(H) | H | * | High-Z | Operating |
| | H(L) | * | * | | Standby |

TC53257P TC53257F

OUTLINE DRAWINGS

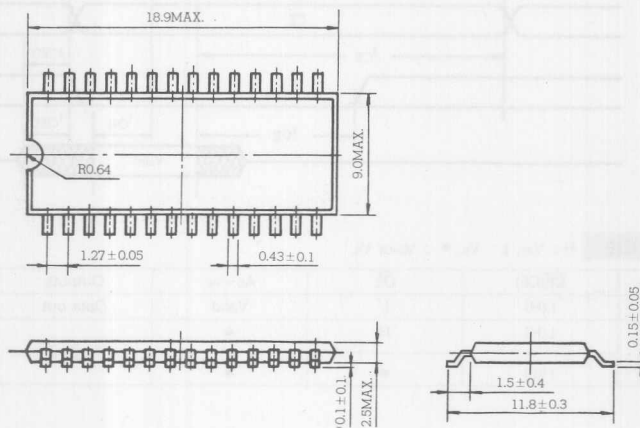
● Plastic DIP



NOTE : Each lead pitch is 2.54mm.

All leads are located within 0.25mm of their true longitudinal position with respect to No. 1 and No. 28 leads.

● Plastic FP



NOTE : Each lead pitch is 1.27mm.

All leads are located within 0.12mm of their true longitudinal position with respect to No. 1 and No. 28 leads.

Note : Toshiba does not assume any responsibility for use of any circuitry described ; no circuit patent licenses are implied, and Toshiba reserves the right, at any time without notice, to change said circuitry.

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DESCRIPTION

The TC531000P is a 1,048,576 bit read only memory organized as 131,072 words by 8 bits with a low bit cost, thus being suitable for use in program memory of microprocessor, especially character generator. The TC531000P using CMOS technology is most suitable for low power applications where

battery operation are required.

The TC531000P has one chip enable input \overline{CE}/CE , programmable for device selection.

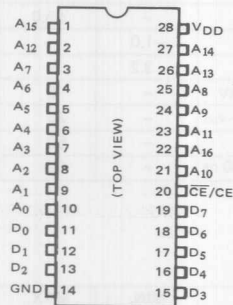
The TC531000P is moulded in a 28 pin standard plastic package, 0.6 inch in width.

FEATURES

- Single 5V Power Supply
- Access Time: 200 ns (Max.)
- Power Dissipation
 - Operating Current: 30mA (Max.)
 - Standby Current: 20 μ A (Max.)

- All Inputs and Outputs: TTL Compatible
- Three State Outputs
- 28 pin 600 mil width DIP Plastic package
- Fully Static Operation
- Programmable Chip Enable

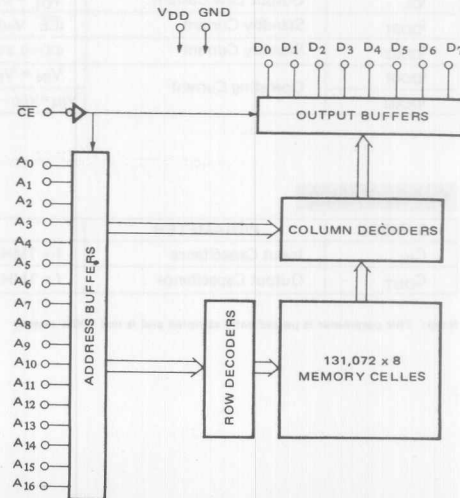
PIN CONNECTION



PIN NAMES

| | |
|--------------------|-------------------|
| $A_0 \sim A_{16}$ | Address inputs |
| $D_0 \sim D_7$ | Data outputs |
| \overline{CE}/CE | Chip enable input |
| V_{DD} | Power supply |
| GND | Ground |

BLOCK DIAGRAM



TC531000P

MAXIMUM RATINGS

| SYMBOL | ITEM | RATING | UNIT |
|--------------|------------------------------|--------------------|-------------------------------------|
| V_{DD} | Power Supply Voltage | $-0.5 \sim 7.0$ | V |
| V_{IN} | Input Voltage | $-0.5 \sim V_{DD}$ | V |
| V_{OUT} | Output Voltage | $0 \sim V_{DD}$ | V |
| P_D | Power Dissipation | 1.0 | W |
| T_{STG} | Storage Temperature | $-55 \sim 150$ | $^{\circ}\text{C}$ |
| T_{OPR} | Operating Temperature | $-40 \sim 85$ | $^{\circ}\text{C}$ |
| T_{SOLDER} | Soldering Temperature · Time | $260 \cdot 10$ | $^{\circ}\text{C} \cdot \text{sec}$ |

D.C. OPERATING CONDITIONS ($T_a = -40 \sim 85^{\circ}\text{C}$)

| SYMBOL | PARAMETER | MIN. | TYP. | MAX. | UNIT |
|----------|----------------------|------|------|----------------|------|
| V_{DD} | Power Supply Voltage | 4.5 | 5.0 | 5.5 | V |
| V_{IH} | Input High Voltage | 2.2 | — | $V_{DD} + 0.3$ | V |
| V_{IL} | Input Low Voltage | -0.3 | — | 0.8 | V |

D.C. and OPERATING CHARACTERISTICS ($T_a = -40 \sim 85^{\circ}\text{C}$, $V_{DD} = 5\text{V} \pm 10\%$)

| SYMBOL | PARAMETER | CONDITIONS | MIN. | MAX. | UNIT |
|------------|------------------------|---|------|-----------|---------------|
| I_{IL} | Input Leakage Current | $V_{IN} = 0 \sim V_{DD}$ | — | ± 1.0 | μA |
| I_{LO} | Output Leakage Current | $\overline{CE} = V_{IH}$, $V_{OUT} = 0\text{V} \sim V_{DD}$ | — | ± 5.0 | μA |
| I_{OH} | Output High Current | $V_{OH} = 2.4\text{V}$ | -1.0 | — | mA |
| I_{OL} | Output Low Current | $V_{OL} = 0.4\text{V}$ | 3.2 | — | mA |
| I_{DDS1} | Standby Current | $(\overline{CE}, V_{IH}) = 2.2\text{V}$, $(\overline{CE}, V_{IL}) = 0.8\text{V}$ | — | 5 | mA |
| I_{DDS2} | Standby Current | $(\overline{CE}) = 0.2\text{V}$, $(\overline{CE}) = V_{DD} - 0.2\text{V}$, $V_{IN} = 0\text{V} \sim V_{DD}$ | — | 20 | μA |
| I_{DD01} | Operating Current | $V_{IN} = V_{IH}/V_{IL}$, $t_{\text{cycle}} = 200\text{ ns}$ | — | 50 | mA |
| I_{DD02} | | $V_{IN} = V_{DD} - 0.2\text{V}/0.2\text{V}$, $t_{\text{cycle}} = 200\text{ ns}$ | — | 30 | mA |

CAPACITANCE

| SYMBOL | PARAMETER | CONDITIONS | MIN. | MAX. | UNIT |
|-----------|--------------------|--|------|------|------|
| C_{IN} | Input Capacitance | $f = 1\text{MHz}$, $T_a = 25^{\circ}\text{C}$ | — | 8 | pF |
| C_{OUT} | Output Capacitance | $f = 1\text{MHz}$, $T_a = 25^{\circ}\text{C}$ | — | 10 | pF |

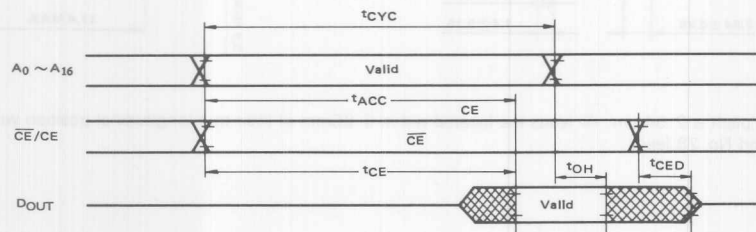
Note: This parameter is periodically sampled and is not 100% tested.

A.C. CHARACTERISTICS ($T_a = -40 \sim 85^\circ\text{C}$, $V_{DD} = 5V \pm 10\%$)

| SYMBOL | PARAMETER | MIN. | MAX. | UNIT |
|-----------|------------------------------------|------|------|------|
| t_{CYC} | Cycle Time | 200 | — | ns |
| t_{ACC} | Access Time | — | 200 | ns |
| t_{CE} | Chip Enable Access Time from CE/CE | — | 200 | ns |
| t_{CED} | Output Disable Time from CE/CE | 0 | 70 | ns |
| t_{OH} | Output Hold Time | 0 | — | ns |

AC TEST CONDITIONS

| | |
|-------------------------------------|----------------|
| Output Load | : 100pF + 1TTL |
| Input Levels | : 0.6V, 2.4V |
| Timing Measurement Reference Levels | |
| Input | : 0.8V, 2.2V |
| Output | : 0.8V, 2.0V |
| Input Rise and Fall Time | : 5ns |

TIMING WAVEFORMS**OPERATION MODE**

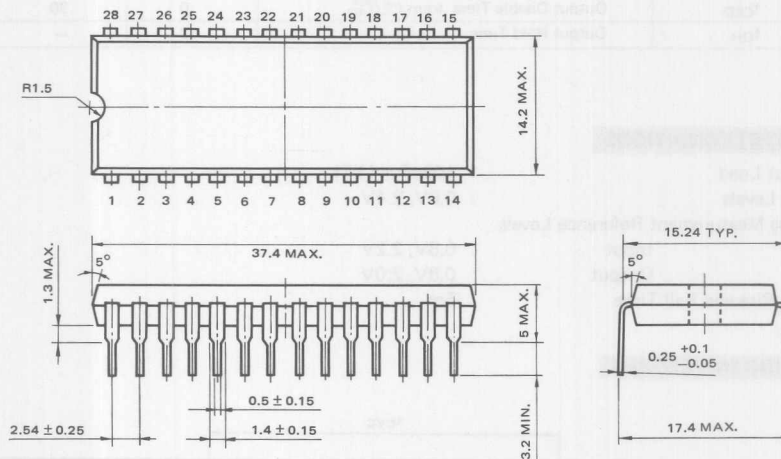
| MODE | \overline{CE} (CE) | $A_0 \sim 16$ | Outputs | Power |
|-----------------|----------------------|---------------|----------|-----------|
| Read | L(H) | Valid | Data out | Operating |
| Output Deselect | H(L) | * | High-Z | Standby |

H: V_{IH} , L: V_{IL} , *: V_{IH} or V_{IL}

TC531000P

OUTLINE DRAWINGS

Unit: mm



Note : Each lead pitch is 2.54mm. All leads are located within 0.25mm of their true longitudinal position with respect to No. 1 and No. 28 leads.

Note: Toshiba does not assume any responsibility for use of any circuitry described; no circuit patent licenses are implied, and Toshiba reserves the right, at any time without notice, to change said circuitry.
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